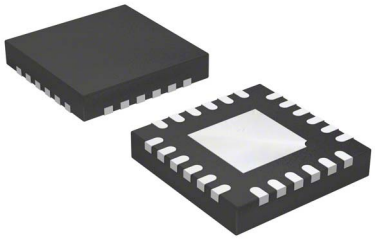
STSPIN820

Advanced 256 microsteps integrated motor driver with step-clock and direction interface

Datasheet - production data



QFN 4 x 4 - 24 lead

Features

- Operating voltage from 7 to 45 V
- Maximum output current 1.5 A_{rms}
- R_{DSon} HS + LS = 1 Ω typ.
- Microstepping up to 1/256th of step
- Current control with programmable OFF time
- Current sensing based on external shunt resistor
- Full protection set
- Non-dissipative overcurrent protection
- Short-circuit protection
- Undervoltage lockout
- Thermal shutdown
- Standby low consumption

Applications

- 3D printers
- Medical equipment
- Industrial 2D printers
- Textile and sewing machines
- CCTV, security and dome cameras
- ATM and cash handling machines
- Office and home automation
- POS
- Robotics

Description

The STSPIN820 is a stepper motor driver which integrates, in a small QFN 4 x 4 mm package, both control logic and a low R_{DSon} power stage.

The integrated controller implements a PWM current control with fixed OFF time and a microstepping resolution up to 1/256th of the step.

The device can be forced into a low consumption state.

The device offers a complete set of protection features including overcurrent, overtemperature and short-circuit protection.

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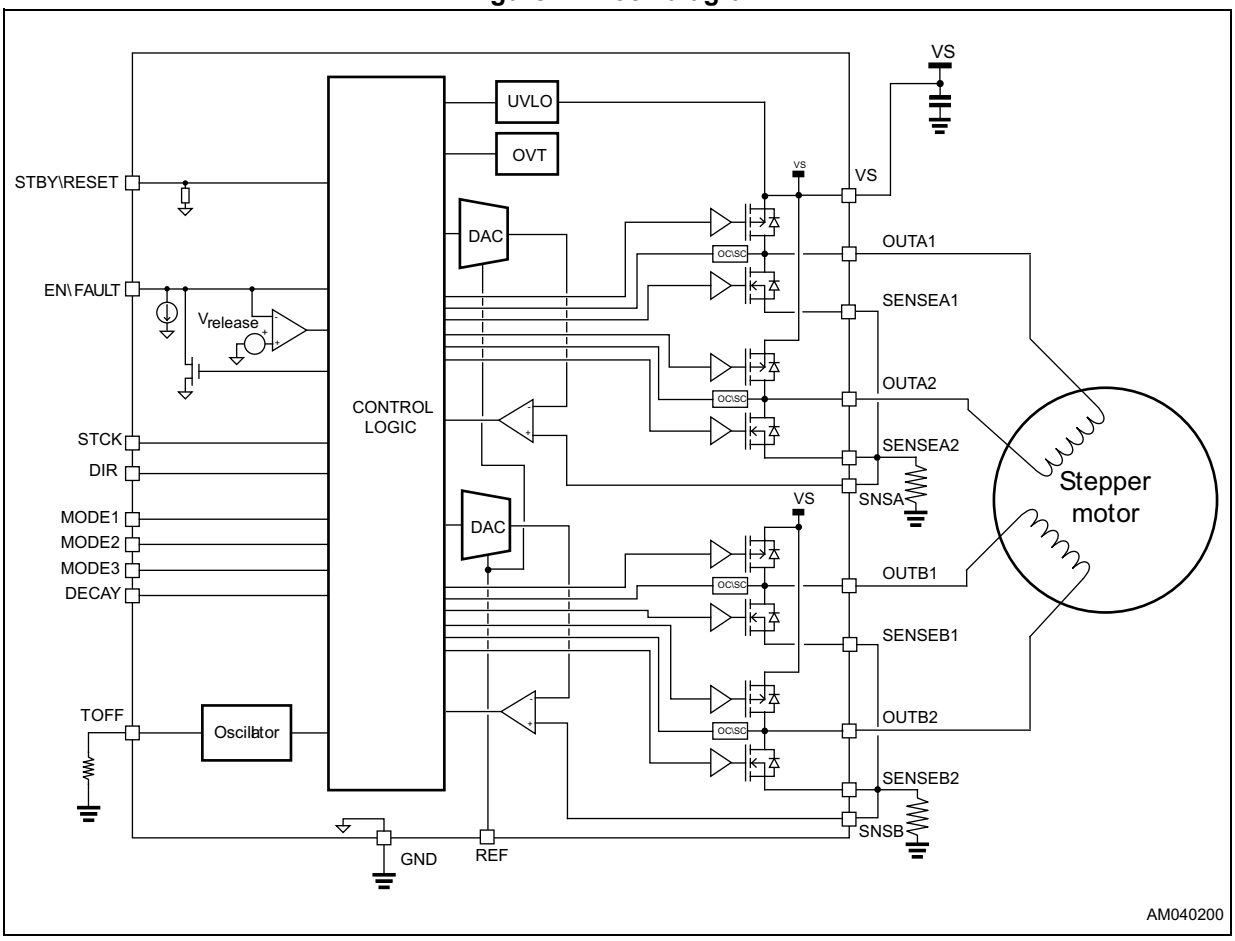
Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_S	Supply voltage	-	-0.3 to 48	V
V_{IN}	Logic input voltage	-	-0.3 to 5.5	V
$V_{OUT,diff}$	Differential voltage between VS, OUTx1, OUTx2 and SENSEx pins	-	up to 48	V
V_{SENSE}	Sense pins voltage	-	-2 to 2	V
V_{REF}	Reference voltage input	-	-0.3 to 2	V
$I_{OUT,RMS}$	Continuous power stage output current (each full-bridge)	-	1.5	A_{rms}
T_j	Junction temperature	-	-40 to 150	°C
T_{STG}	Storage temperature	-	-55 to 150	°C

2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply voltage	7	-	45	V
V_{IN}	Logic input voltage	-	-	5	V
V_{SENSE}	Sense pins voltage	-1	-	+1	V
V_{REF}	Reference voltage input	0.1	-	1	V

2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Conditions	Value	Unit
R_{thJA}	Junction to ambient thermal resistance	Natural convection, according to JESD51-2A(1)	36.5	°C/W
$R_{thJCtop}$	Junction to case thermal resistance (top side)	Cold plate on top package, according to JESD51-12(1)	27.6	°C/W
$R_{thJCbot}$	Junction to case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-12(1)	5.9	°C/W
R_{thJB}	Junction to board thermal resistance	according to JESD51-8(1)	13.6	°C/W
Ψ_{JT}	Junction to top characterization	According to JESD51-2A(1)	1	°C/W
Ψ_{JB}	Junction to board characterization	According to JESD51-2A(1)	13.7	°C/W

1. Simulated on a 76.2 x 114.3 x 1.6 mm, with vias underneath the component, the 2s2p board as per the standard JEDEC (JESD51-7) in natural convection.

2.4 ESD protection ratings

Table 4. ESD protection ratings

Symbol	Parameter	Conditions	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS001	H2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS002 All pins	C2a	500	V
		Conforming to ANSI/ESDA/JEDEC JS002 Corner pins only (1, 6, 7, 12, 13, 18, 19, 24)	-	750	V
MM	Machine model	Conforming to EIA/JESD22-A115-C	NC	200	V

3 Electrical characteristics

Testing conditions: V_S = 36 V, T_j = 25 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General						
$V_{Sth(ON)}$	V_S turn-on threshold	V_S rising from 0 V	-	6.0	6.5	V
$V_{Sth(HYST)}$	V_S turn-off threshold hysteresis	V_S falling from 7 V	-	0.4	-	V
I_S	V_S supply current	No commutations EN = 0 R_{TOFF} = 10 kΩ	-	2.3	2.75	mA
		No commutations EN = 1 R_{TOFF} = 10 kΩ	-	2.7	3	
V_{STBYL}	Standby low voltage	-	-	-	0.8	V
V_{STBYH}	Standby high voltage	-	2	-		V
$I_{S, STBY}$	V_S supply standby current	STBY = '0'	-	-	45	µA
Power stage						
$R_{DSon\ HS+LS}$	Total on resistance HS + LS	V_S = 21 V I_{OUT} = 1 A	-	1	1.3	Ω
		V_S = 21 V I_{OUT} = 1 A T_j = 125 °C(1)	-	1.4	1.6	
I_{DSS}	Output leakage current	OUTx = V_S = 48 V	-	-	20	µA
		OUTx = -0.3 V	-1	-	-	
V_{DF}	Freewheeling diode forward voltage	I_D = 1.5 A	-	1	-	V
t_{rise}	Rise time	V_S = 21 V	-	120	-	ns
t_{fall}	Fall time	V_S = 21 V	-	60	-	ns
Logic IO						
V_{IH}	High logic level input voltage	-	2	-		V
V_{IL}	Low logic level input voltage	-	-	-	0.8	V
V_{OL}	FAULT low logic level output voltage	I_{OL} = 4 mA	-	-	0.3	V
$V_{RELEASE}$	FAULT open-drain release voltage	-	-	-	0.6	V
R_{STBY}	STBY pull-down resistance	-	-	60	-	kΩ
I_{EN}	Enable pull-down current	-	-	5	-	µA
t_{ENd}	Enable input propagation delay	From EN falling edge to OUTx high impedance	-	400	-	ns

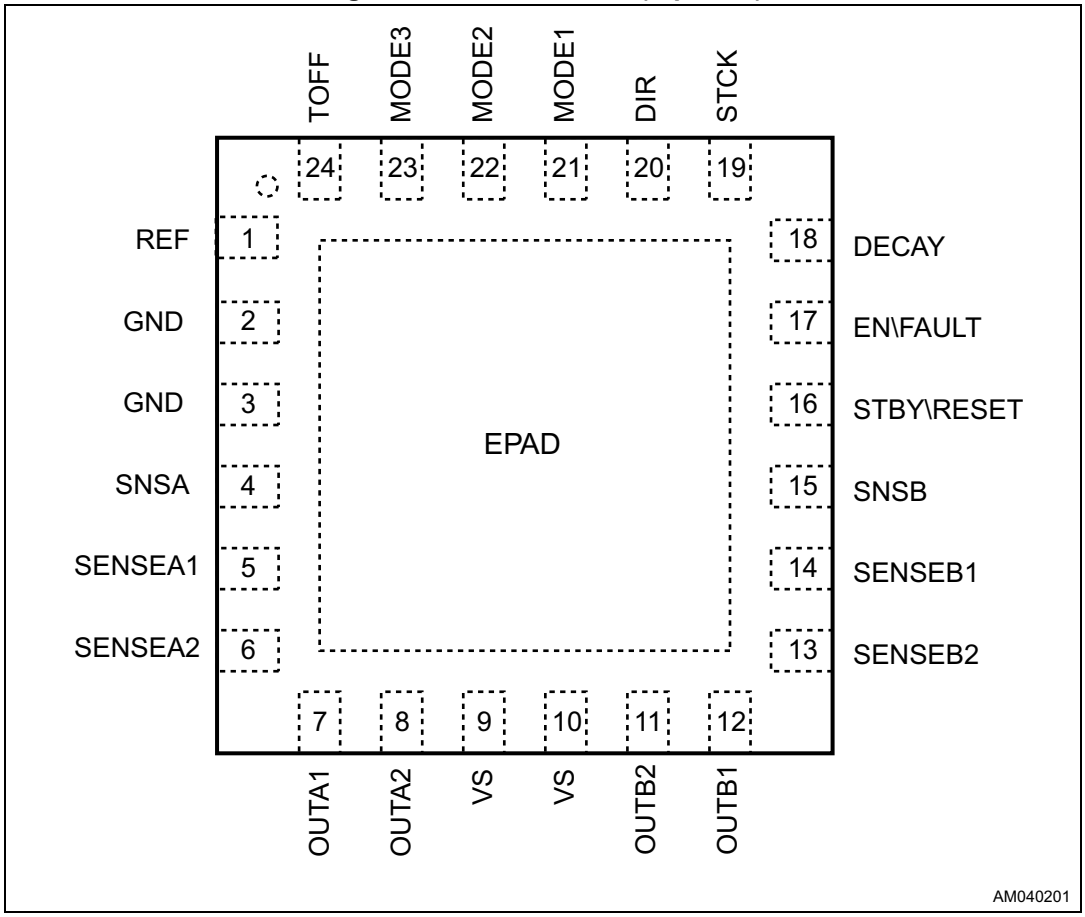
Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{MODE,su}$	MODE inputs setup time	(2)	20	-	-	ns
$t_{MODE,ho}$	MODE inputs hold time	(2)	20	-	-	ns
$t_{DIR,su}$	DIR input setup time	(2)	20	-	-	ns
$t_{DIR,ho}$	DIR input hold time	(2)	20	-	-	ns
t_{STCKH}	STCK input high time	(2)	20	-	-	ns
t_{STCKL}	STCK input low time	(2)	20	-	-	ns
f_{STCK}	STCK input frequency	(2)	-	-	4	MHz
$t_{STCK,d}$	STCK propagation delay	-	-	100	-	ns
PWM current control						
t_{OFF}	Total OFF time	ROFF = 10 kΩ	-	13	-	µs
		ROFF = 160 kΩ	-	146	-	µs
Δt_{OFF}	OFF time precision	Full temperature range(1)	-20%	-	+20%	-
$t_{OFF,jitter}$	Total OFF time jittering	-	-	± 2%	-	-
$t_{OFF,SLOW}$	Slow decay time(3)	DECAY = '0'	-	5/8 × t_{OFF}	-	µs
		DECAY = '1'	-	t_{OFF}	-	µs
$t_{OFF,FAST}$	Fast decay time(3)	DECAY = '0'	-	3/8 × t_{OFF}	-	µs
		DECAY = '1'	-	0	-	µs
Protections						
T_{jSD}	Thermal shutdown threshold	-	-	160	-	°C
$T_{jSD,Hyst}$	Thermal shutdown hysteresis	-	-	40	-	°C
I_{OC}	Overcurrent protection threshold	-	-	3	3.5	A

1. Based on characterization data on a limited number of samples, not tested during production.
2. See *Figure 4 on page 13*.
3. See *Figure 5 on page 17*.

4 Pin connection

Figure 2. Pin connection (top view)



Note: The exposed pad must be connected to ground.

Table 6. Pin description

No.	Name	Type	Function
1	REF	Analog input	Reference voltage for the PWM current control circuitry
2, 3 EPAD	GND	Ground	Device ground
4	SNSA	Analog input	Full-bridge A current regulator sense input
5	SENSEA1	Power output	Sense output of the bridge A
6	SENSEA2	Power output	Sense output of the bridge A
7	OUTA1	Power output	Power bridge output side A1
8	OUTA2	Power output	Power bridge output side A2
9	VS	Supply	Device supply voltage
10	VS	Supply	Device supply voltage
11	OUTB2	Power output	Power bridge output side B2

Table 6. Pin description (continued)

No.	Name	Type	Function
12	OUTB1	Power output	Power bridge output side B1
13	SENSEB2	Power output	Sense output of the bridge B
14	SENSEB1	Power output	Sense output of the bridge B
15	SNSB	Analog input	Full-bridge B current regulator sense input
16	STBY\RESET	Logic input	Standby\reset input. When forced low the device enters in low consumption mode.
17	EN\FAULT	Logic input\ open-drain output	Logic input 5 V compliant with open-drain output. This is the power stage enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs.
18	DECAY	Logic input	Decay mode selection input. High logic level sets slow decay mode; low logic level sets mixed decay mode (see *Section 5.3 on page 16* for more details).
19	STCK	Logic input	Step clock input
20	DIR	Logic input	Direction input
21	MODE1	Logic input	Step mode selection input 1
22	MODE2	Logic input	Step mode selection input 2
23	MODE3	Logic input	Step mode selection input 3
24	TOFF	Analog input	Internal oscillator frequency adjustment

5 Functional description

The STSPIN820 is a stepper motor driver integrating a microstepping sequencer (up to 1/256th step), two PWM current controllers and a power stage composed by two fully-protected full-bridges.

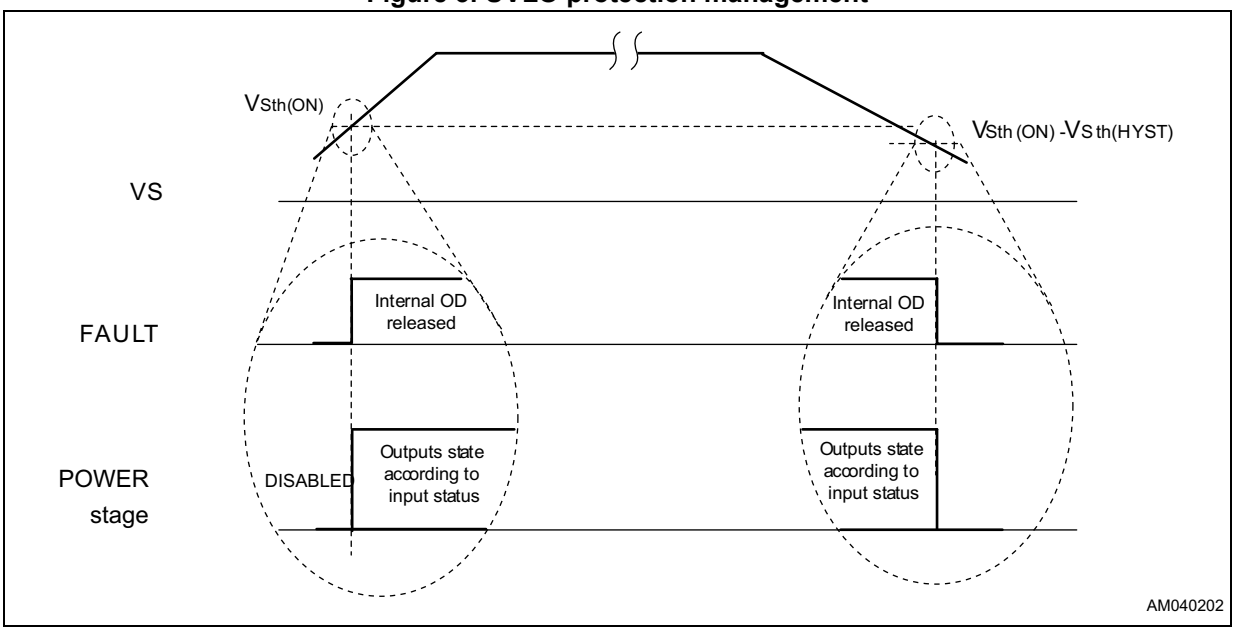
5.1 Power supply and standby

The device is supplied through the VS pins, the two pins **must** be at the same voltage.

At power-up the power stage is disabled and the FAULT pin is forced low until the VS voltage rises above the $V_{Sth(ON)}$ threshold.

If the V_S falls below the $V_{Sth(ON)}$ - $V_{Sth(HYST)}$ value the power stage is immediately disabled and the FAULT pins are forced low.

Figure 3. UVLO protection management



The device provides a low consumption mode which is set forcing the STBY\RESET input below the V_{STBYL} threshold.

When the device is in standby status the power stage is disabled (outputs are in high impedance) and the supply to the integrated control circuitry is strongly reduced. When the device exits the standby status, all of the control circuitry is reset at power-up condition.

5.2 Microstepping sequencer

At each STCK rising edge, the sequencer of the device is increased (DIR input high) or decreased (DIR input low) of a module selected through the MODEx inputs as listed in *Table 7*.

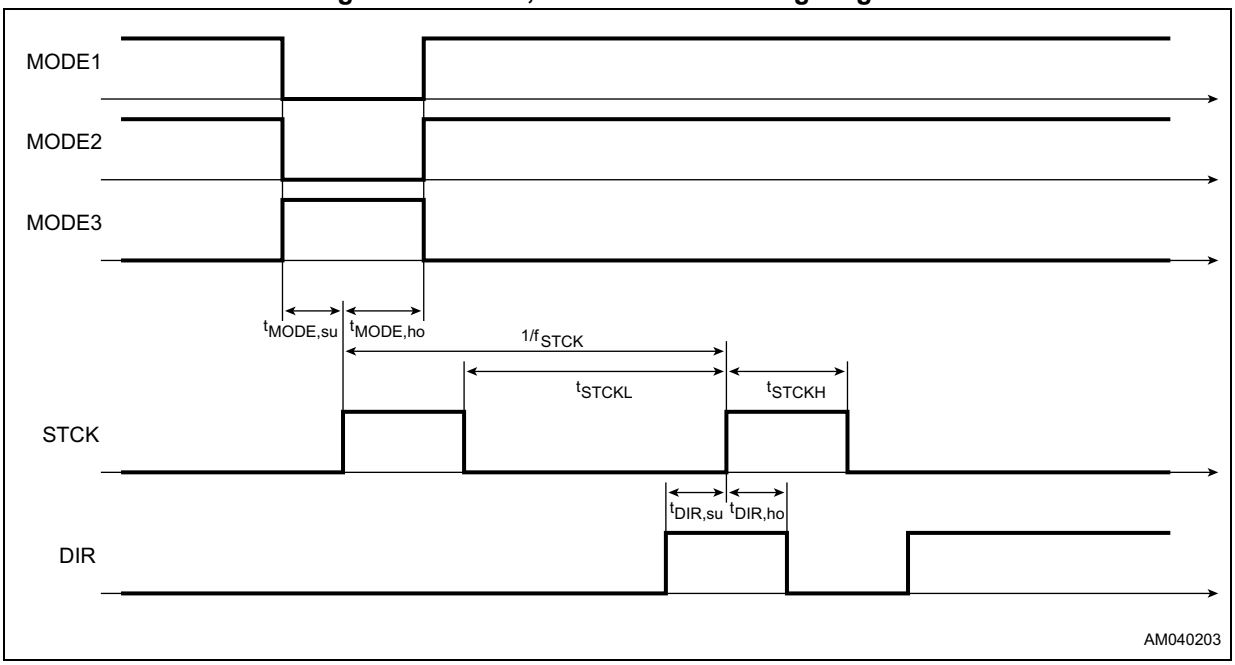
The sequencer is a 10-bit counter that sets the reference value of the PWM current controller and the direction of the current for both of the full-bridges.

Note: The MODE1, MODE2 and MODE3 configuration can be changed in any time and it is immediately applied.

Table 7. Step mode selection through MODEx inputs

MODE3	MODE2	MODE1	Step mode	Counter module (binary)
0	0	0	Full-step	0100000000
0	0	1	½ step	0010000000
0	1	0	¼ step	0001000000
0	1	1	1/8th step	0000100000
1	0	0	1/16th step	0000010000
1	0	1	1/32nd step	0000001000
1	1	0	1/128th step	0000000010
1	1	1	1/256th step	0000000001

Figure 4. MODEx, STCK and DIR timing diagram



When the full-step mode is set, the reference value of the PWM current controllers and the direction of the currents are set as listed in *Table 8*.

Table 8. Target reference and current direction according to sequencer value (full-step mode)

Sequencer value										Phase A		Phase B	
										Reference voltage	Current direction	Reference voltage	Current direction
0	0	X	X	X	X	X	X	X	X	100% × V_{REF}	A1 → A2	100% × V_{REF}	B1 → B2
0	1	X	X	X	X	X	X	X	X	100% × V_{REF}	A1 → A2	100% × V_{REF}	B1 ← B2
1	0	X	X	X	X	X	X	X	X	100% × V_{REF}	A1 ← A2	100% × V_{REF}	B1 ← B2
1	1	X	X	X	X	X	X	X	X	100% × V_{REF}	A1 ← A2	100% × V_{REF}	B1 → B2

When the step mode is different from the full-step mode the values listed in *Table 9* are used.

Table 9. Target reference and current direction according to sequencer value (not full-step mode)

Sequencer value										Phase A		Phase B	
										Reference voltage	Current direction	Reference voltage	Reference voltage
0	0	0	0	0	0	0	0	0	0	Zero (power bridge disabled)	-	100% × V_{REF}	B1 → B2
0	0	N								Sin (N/256 × π/2) × V_{REF}	A1 → A2	-	B1 → B2
0	1	0	0	0	0	0	0	0	0	100% × V_{REF}	A1 → A2	Zero (power bridge disabled)	-
0	1	N								Sin (π/2 + N/256 × π/2) × V_{REF}	A1 → A2	Cos (π/2 + N/256 × π/2) × V_{REF}	B1 ← B2
1	0	0	0	0	0	0	0	0	0	Zero (power bridge disabled)	-	100% × V_{REF}	B1 ← B2
1	0	N								Sin (N/256 × π/2) × V_{REF}	A1 ← A2	Cos (N/256 × π/2) × V_{REF}	B1 ← B2
1	1	0	0	0	0	0	0	0	0	100% × V_{REF}	A1 ← A2	Zero (power bridge disabled)	-
1	1	N								Sin (π/2 + N/256 × π/2) × V_{REF}	A1 ← A2	Cos (π/2 + N/256 × π/2) × V_{REF}	B1 → B2

The DECAY input determinates the behavior of the PWM current control as described in *Section 5.3*.

When the EN\FAULT input is forced low the power stage is immediately disabled (all MOSFETs are turned off). The pin is also used as FAULT indication through the integrated open-drain MOSFET as described in *Section 5.4 on page 19* and *Section 5.5 on page 22*.

Table 10 shows the target reference and sequencer values for the 1/2-, 1/4- and 1/8-step operation. Higher microstepping resolutions follow the same pattern. The reset state (home state) for all stepping mode is entered at power-up or when the device exits the standby status.

Table 10. Example

1/2 step	1/4 step	1/8 step	VREF phase A	VREF phase B	Sequencer value
1	**1**	**1**	**0%**	**100%**	**0000000000 home state**
-	-	2	19.509%	98.079%	0000100000
-	2	3	38.268%	92.388%	0001000000
-	-	4	55.557%	83.147%	0001100000
2	3	5	70.711%	70.711%	0010000000
-	-	6	83.147%	55.557%	0010100000
-	4	7	92.388%	38.268%	0011000000
-	-	8	98.079%	19.509%	0011100000
3	5	9	100%	0%	0100000000
-	-	10	98.079%	-19.509%	0100100000
-	6	11	92.388%	-38.268%	0101000000
-	-	12	83.147%	-55.557%	0101100000
4	7	13	70.711%	-70.711%	0110000000
-	-	14	55.557%	-83.147%	0110100000
-	8	15	38.268%	-92.388%	0111000000
-	-	16	19.509%	-98.079%	0111100000
5	9	17	0%	-100%	1000000000
-	-	18	-19.509%	-98.079%	1000100000
-	10	19	-38.268%	-92.388%	1001000000
-	-	20	-55.557%	-83.147%	1001100000
6	11	21	-70.711%	-70.711%	1010000000
-	-	22	-83.147%	-55.557%	1010100000
-	12	23	-92.388%	-38.268%	1011000000
-	-	24	-98.079%	-19.509%	1011100000
7	13	25	-100%	0%	1100000000
-	-	26	-98.079%	19.509%	1100100000
-	14	27	-92.388%	38.268%	1101000000
-	-	28	-83.147%	55.557%	1101100000
8	15	29	-70.711%	70.711%	1110000000
-	-	30	-55.557%	83.147%	1110100000
-	16	31	-38.268%	92.388%	1111000000
-	-	32	-19.509%	98.079%	1111100000

Note: The positive number means that the output current is flowing from OUTx1 to OUTx2, vice versa the negative numbers mean that the current is flowing from OUTx2 to OUTx1.

5.3 PWM current control

The device implements two independent PWM current controllers, one for each full-bridge.

The voltage of the sense pins (V_{SNSA} and V_{SNSB}) is compared to the respective internal reference voltage based on the sequencer value (see *Table 8* and *Table 9*).

When $V_{SNSX} > V_{REFX}$ the integrated comparator is triggered, the OFF time counter is started and the decay sequence is performed.

The decay sequence starts turning on both the low sides of the full-bridge (slow decay), after the behavior of the PWM current control depends on the DECAY input:

- **When the DECAY input is low (mixed decay):** the system switches from slow decay to quasi-synchronous fast decay (the sinking side of the bridge is put in high impedance) when the counter reaches a fixed threshold corresponding to a 5/8th of the total decay time (t_{OFF}).
  As soon as the counter reaches the end of the count it is reset and the bridges return in the ON state.
- **When the DECAY input is high (slow decay only):** the system stays in slow decay until the counter reaches the end of the count, then it is reset and the bridges returns in the ON state.

The description of the ON, slow decay and fast decay status are listed in *Table 11*.

Table 11. ON, slow decay and fast decay states

Current direction(1)	ON	Slow decay	Fast decay (quasi-synch.)
Zero (power bridge disabled)	HSX1 = OFF LSX1 = OFF HSX2 = OFF LSX2 = OFF	HSX1 = OFF LSX1 = OFF HSX2 = OFF LSX2 = OFF	HSX1 = OFF LSX1 = OFF HSX2 = OFF LSX2 = OFF
X1 → X2	**HSX1 = ON** LSX1 = OFF HSX2 = OFF **LSX2 = ON**	HSX1 = OFF **LSX1 = ON** HSX2 = OFF **LSX2 = ON**	HSX1 = OFF **LSX1 = ON** HSX2 = OFF LSX2 = OFF
X1 ← X2	HSX1 = OFF **LSX1 = ON** **HSX2 = ON** LSX2 = OFF	HSX1 = OFF **LSX1 = ON** HSX2 = OFF **LSX2 = ON**	HSX1 = OFF LSX1 = OFF HSX2 = OFF **LSX2 = ON**

1. The current direction is set according to *Table 8* or *Table 9*.

The reference voltage value, VREF, has to be selected according to the load current target value (peak value) and the sense resistors value.

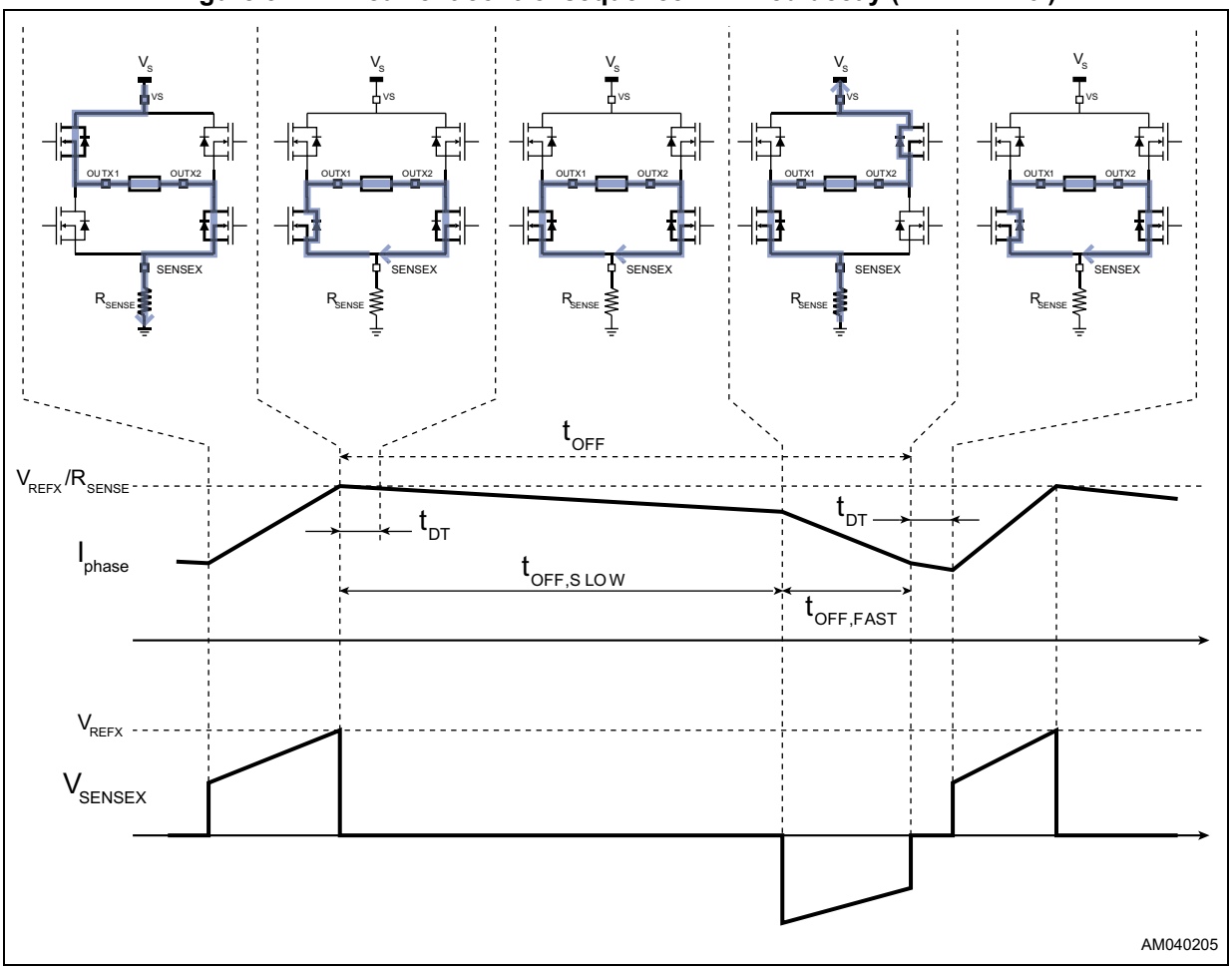
Equation 1

$$V_{REF} = R_{SNS} \cdot I_{LOAD,peak}$$

The choice of the sense resistors value must take into account two main issues:

- The sensing resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during the current recirculation. For this reason the resistance of this component should be kept low (using multiple resistors in parallel will help obtaining the required power rating with standard resistors).
- The lower is the RSNS value, the higher is the peak current error due to noise on the VREF pin and to the input offset of the current sense comparator: too small values of RSNS must be avoided.

Figure 5. PWM current control sequence in mixed decay (DECAY = '0')

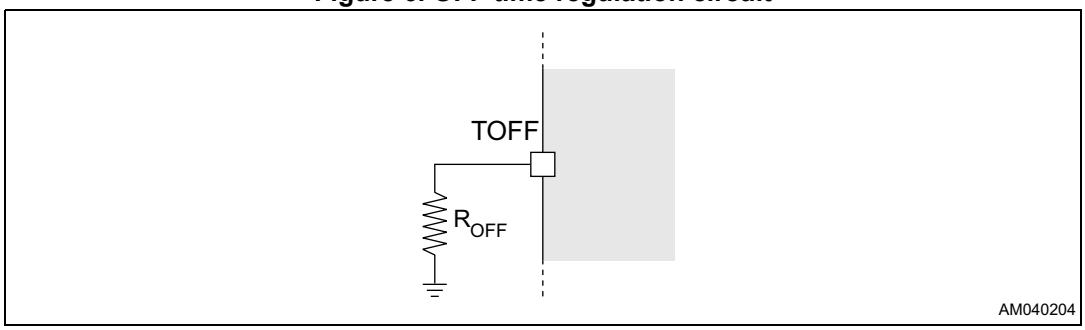


Note: When the voltage on the SNS pins exceeds the absolute ratings, fault condition is triggered and the EN\FAULT output is forced low.

TOFF adjustment

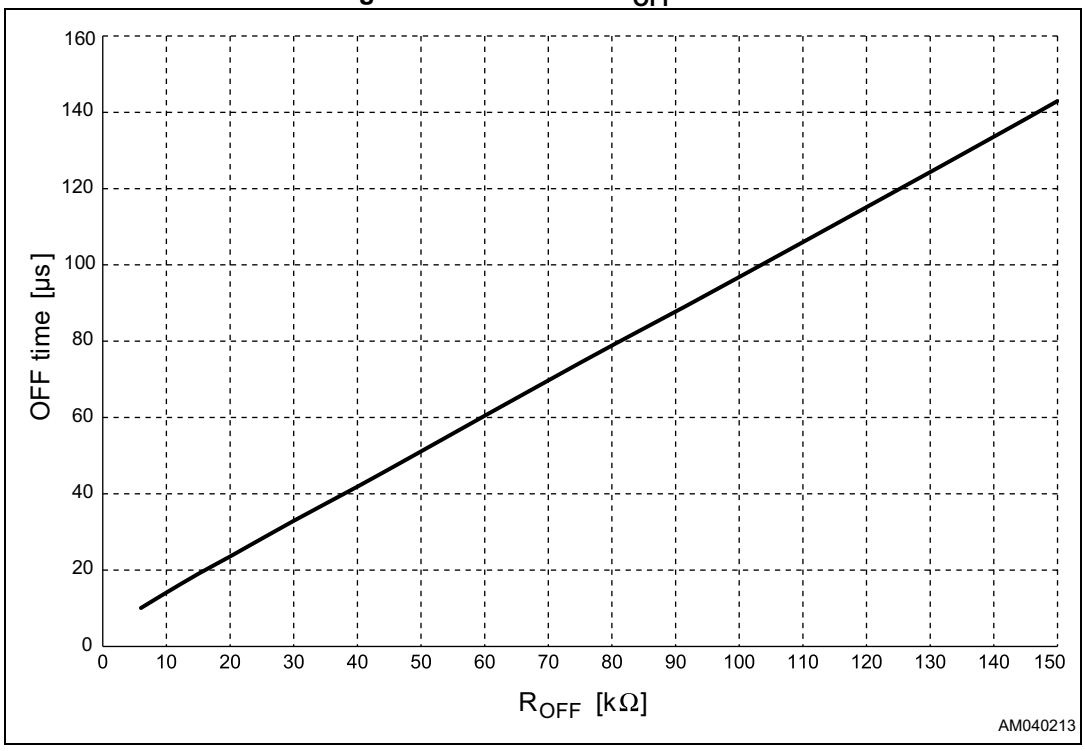
The total OFF time is adjusted through an external resistor connected between the TOFF pin and ground as shown in *Figure 6*.

Figure 6. OFF time regulation circuit



The relation between the total OFF time and the external resistor value is shown in the graph of *Figure 7*. The value typically ranges from 10 µs to 150 µs. The recommended value for R_{OFF} is in the range between 5 kΩ and 180 kΩ.

Figure 7. OFF time vs R_{OFF} value



The resulting OFF time depends on the decay mode selected:

- DECAY = 'L', mixed decay ⇨ $t_{OFF} = t_{OFF,SLOW} + t_{OFF,FAST}$
- DECAY = 'H', slow decay ⇨ $t_{OFF} = t_{OFF,SLOW}$

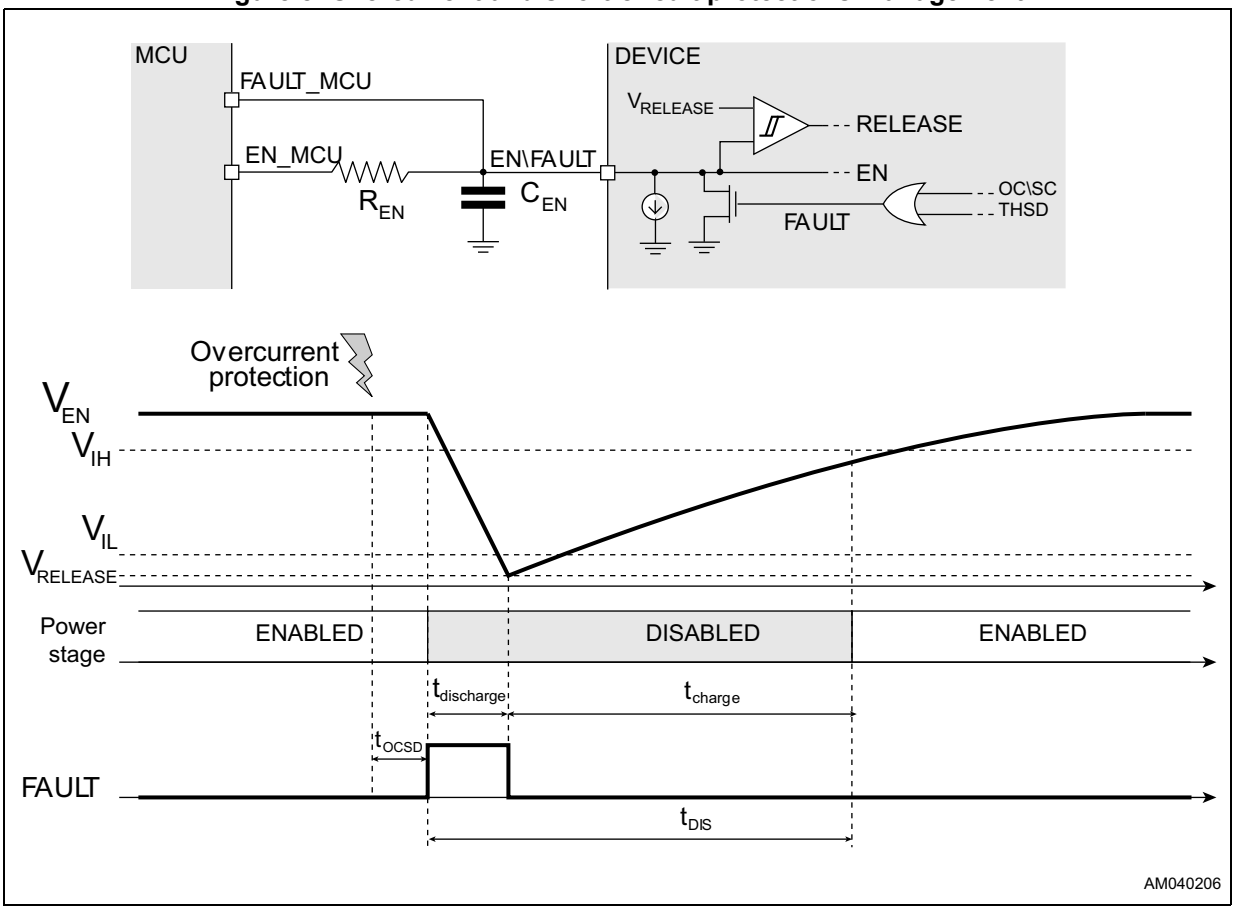
5.4 Overcurrent and short-circuit protections

The device embeds circuitry protecting each power output against the overload and short-circuit conditions (short-circuit to ground, short-circuit to VS and short-circuit between outputs).

When the overcurrent or the short-circuit protection is triggered the power stage is disabled and the EN\FAULT input is forced low through the integrated open-drain MOSFET discharging the external C_{EN} capacitor (refer to *Figure 8*).

The power stage is kept disabled and the open-drain MOSFET is kept ON until the EN\FAULT input falls below the $V_{RELEASE}$ threshold, then the C_{EN} capacitor is charged through the external R_{EN} resistor.

Figure 8. Overcurrent and short-circuit protections management



The total disable time after an overcurrent event can be set sizing properly the external network connected to the EN\FAULT pin (refer to *Figure 9*).

Equation 2

$$t_{DIS} = t_{discharge} + t_{charge}$$

But t_{charge} is normally very higher than $t_{discharge}$ we can consider only the second one contribution:

$$t_{DIS} \cong R_{EN} \bullet C_{EN} \bullet \ln \frac{(V_{DD} - R_{EN} \bullet I_{PD}) - V_{RELEASE}}{(V_{DD} - R_{EN} \bullet I_{PD}) - V_{IH}}$$

Where V_{DD} is the pull-up voltage of the R_{EN} resistor.

Figure 9. Disable time versus R_{EN} and C_{EN} values (V_{DD} = 3.3 V)

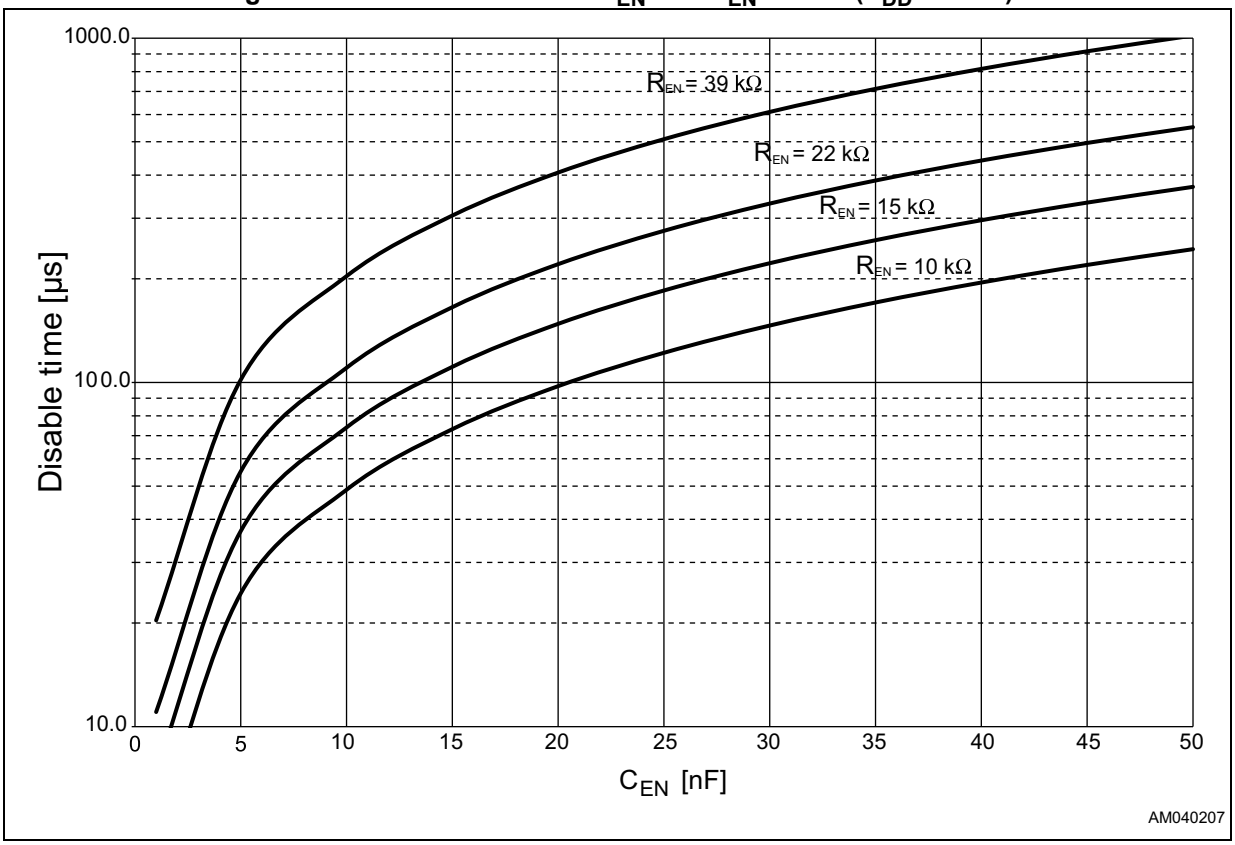
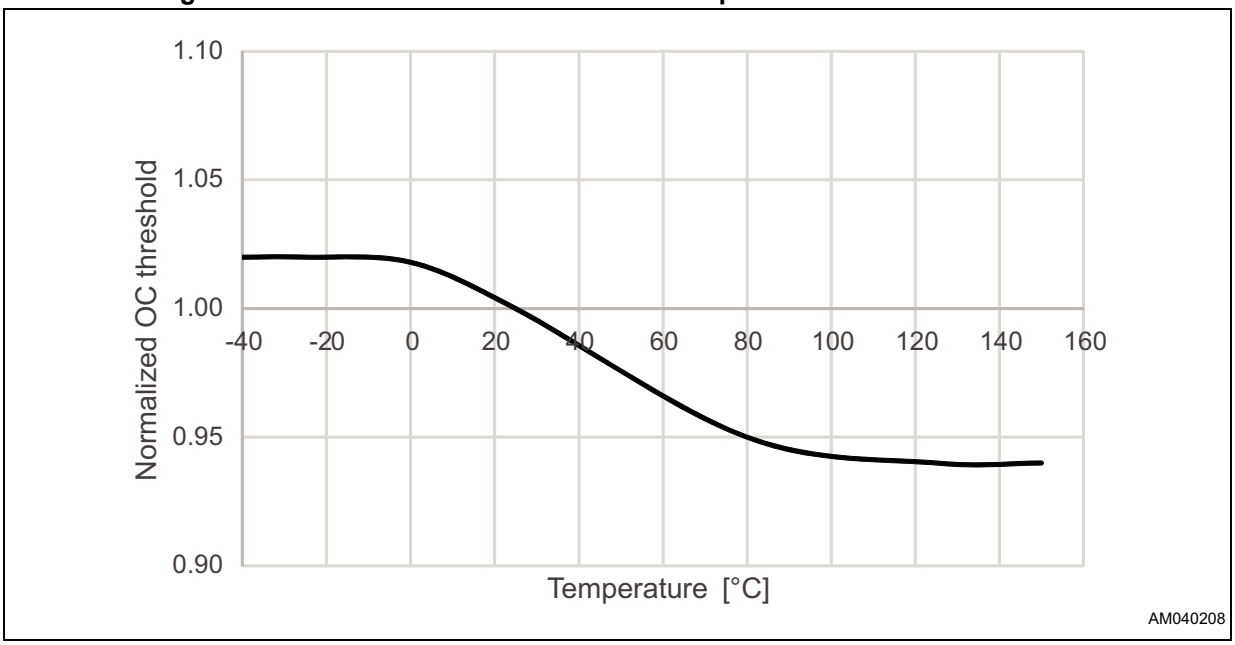


Figure 10. Overcurrent threshold versus temperature normalized at 25 °C



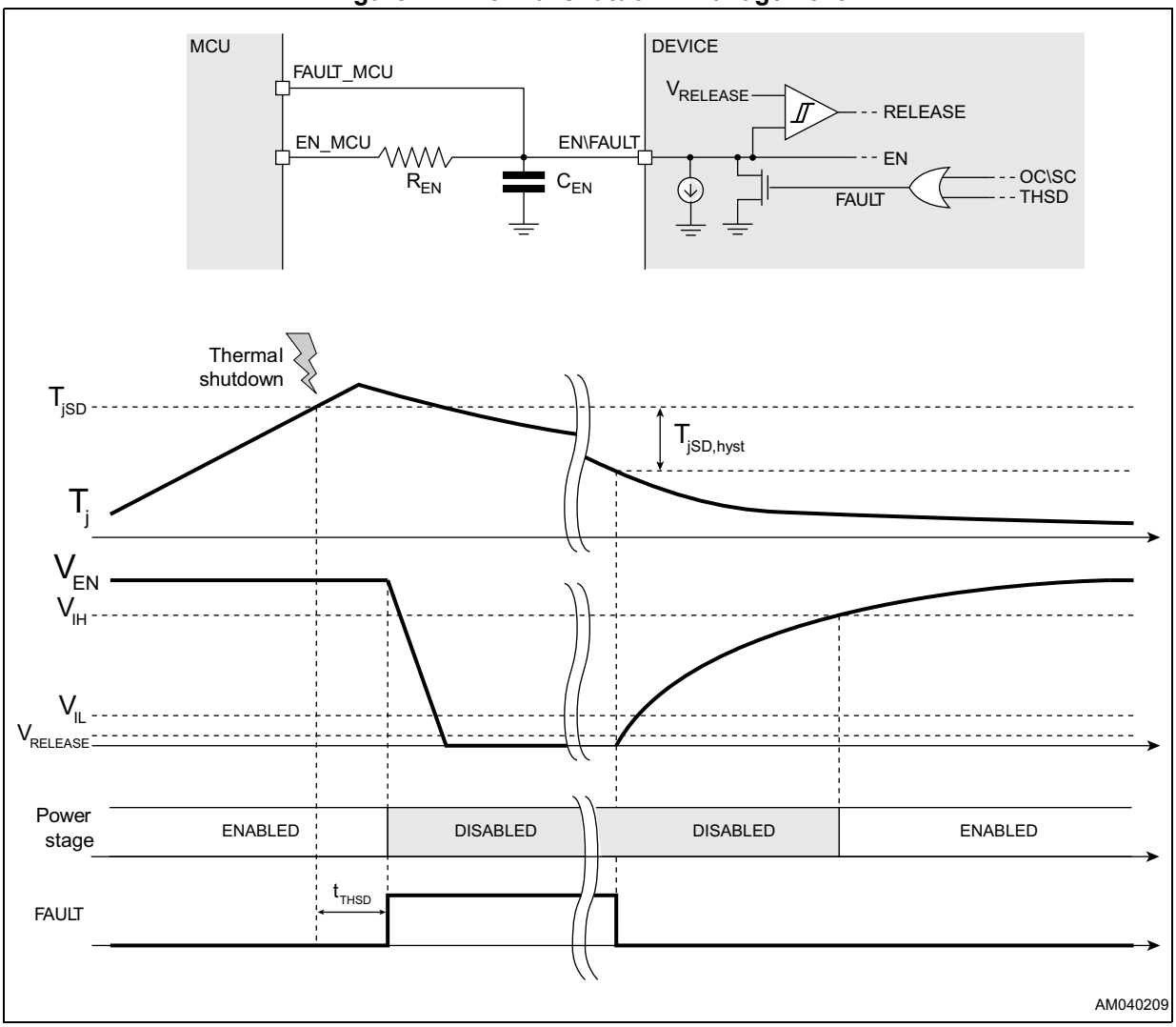
5.5 Thermal shutdown

The device embeds circuitry protecting it from the overtemperature condition.

When the thermal shutdown temperature is reached the power stage is disabled and the EN\FAULT input is forced low through the integrated open-drain MOSFET (refer to *Figure 11*).

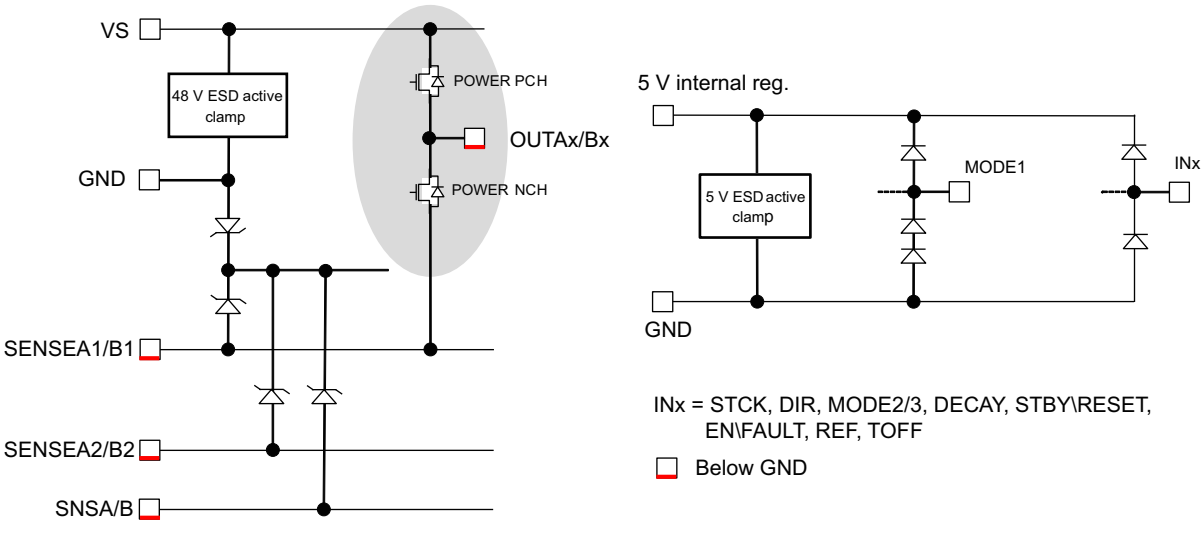
The protection and the EN\FAULT output are released when the IC temperature returns below a safe operating value (T_{jSD} - $T_{jSD,Hyst}$).

Figure 11. Thermal shutdown management



5.6 ESD protection strategy

Figure 12. ESD protection strategy

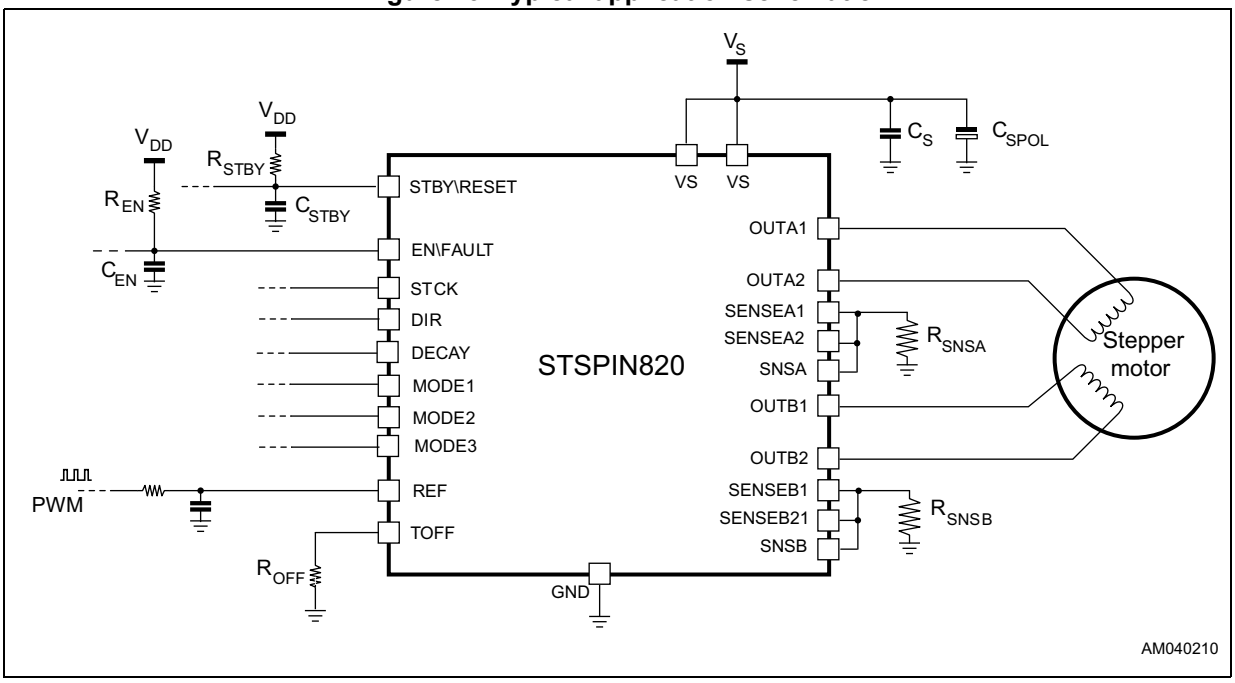


6 Typical applications

Table 12. Typical application values

Name	Value
C_S	330 nF
C_{SPOL}	33 µF
R_{SNSA}, R_{SNSB}	330 mΩ / 1 W
C_{EN}	10 nF
R_{EN}	39 kΩ
C_{STBY}	1 nF
R_{STBY}	18 kΩ
R_{OFF}	10 kΩ ($T_{OFF} \cong$ 13 µs)

Figure 13. Typical application schematic



7 Layout recommendations

The STSPIN820 integrates the power stage; in order to improve the thermal dissipation, the exposed pad must be connected to the ground plane on the bottom layer using multiple vias equally spaced. This ground plane acts as a heatsink, for this reason it should be as wide as possible.

The voltage supply V_S must be stabilized and filtered with a ceramic bypass capacitor, typically 330 nF. It must be placed on the same side and as close as possible to the VS pin in order to reject high frequency noise components on the supply. A bulk capacitor could also be required (typically a 33 µF). The connection between the power supply connector and the V_S pins must be as short as possible using wide traces.

In order to ensure the best ground connection between the STSPIN820 and the other components, a GND plane surrounding the device is recommended.

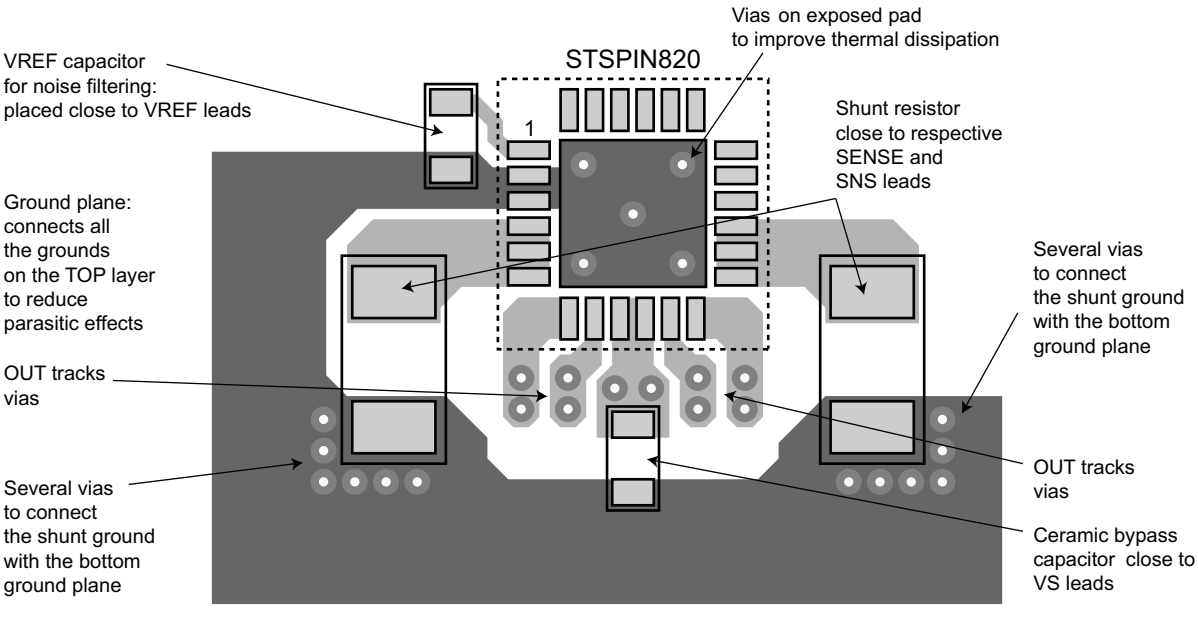
A capacitor between the REF pin and ground should be positioned as near as possible to the device in order to filter the noise and stabilize the reference voltage.

Several vias should be positioned as near as possible each sense resistor connecting them to the ground plane on the bottom layer. In this way, both the GND planes provide a path for the current flowing into the power stage.

The path between the ground of the shunt resistors and the ceramic bypass capacitor of the device is critical; for this reason it must be as short as possible minimizing parasitic inductances that can cause voltage spikes on SENSE and OUT pins.

The OUT pins and the VS nets can be routed using the bottom layer, it is recommended to use two vias for output connections.

Figure 14. PCB layout example (top layer)



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 TFQFPN 4 x 4 x 1.05- 24L package information

Figure 15. TFQFPN 4 x 4 x 1.05- 24L package outline

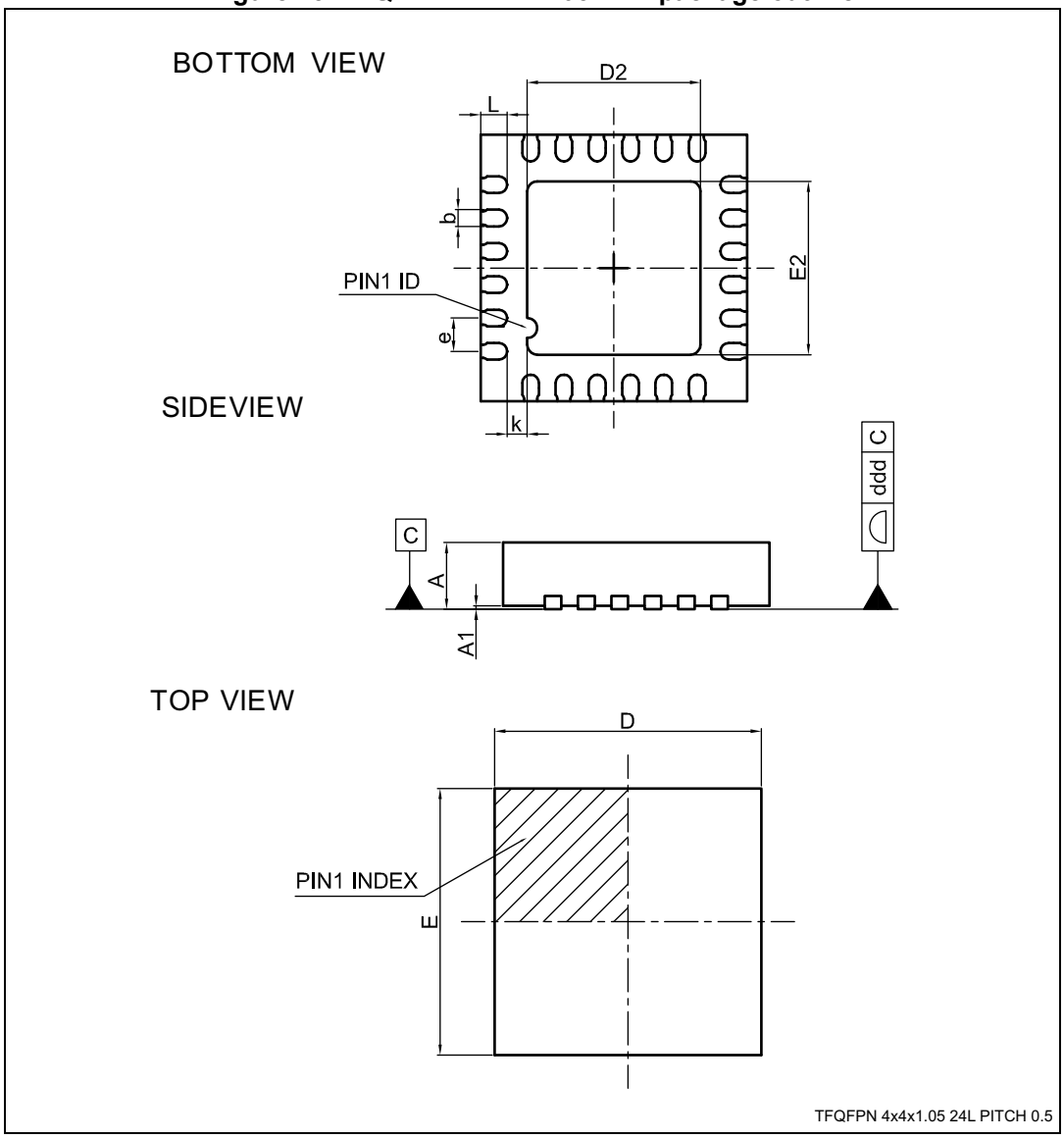
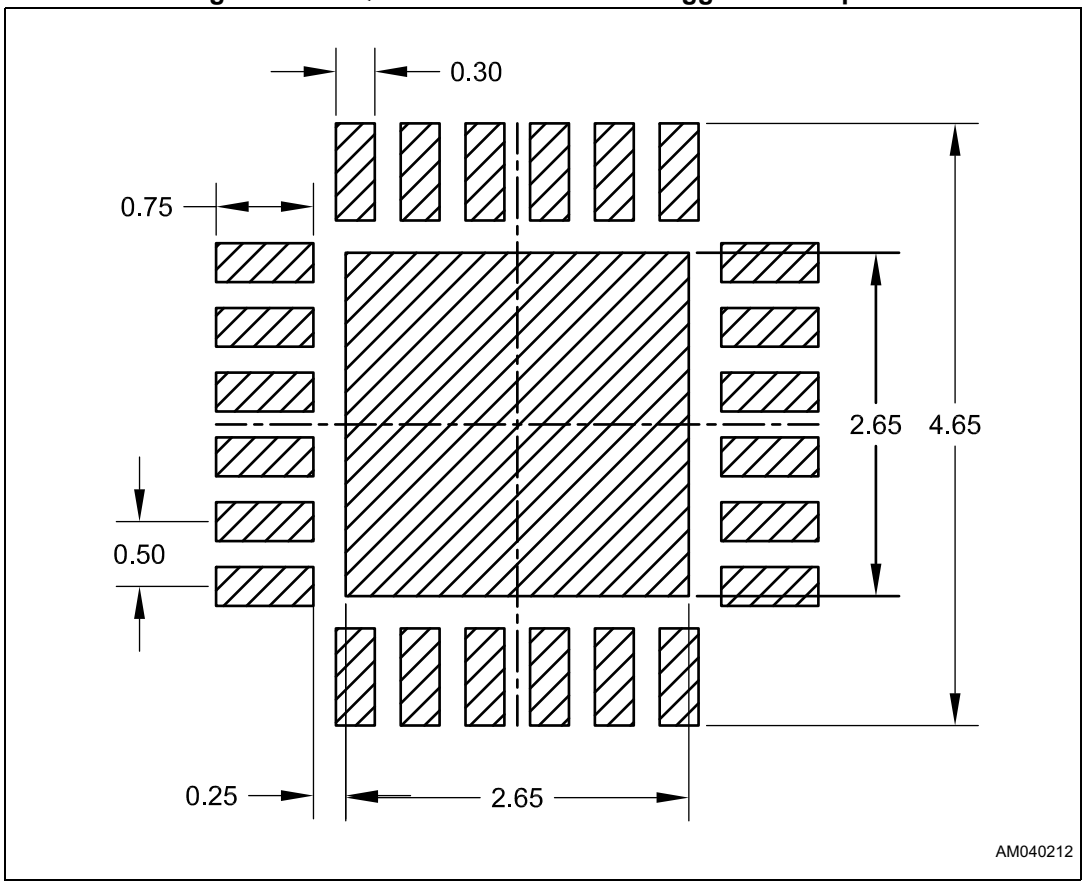


Table 13. TFQFPN 4 x 4 x 1.05 - 24L package mechanical data

Symbol	Dimensions (mm)			Note
	Min.	Typ.	Max.	
A	0.90	1.00	1.10	-
A1	0.00	0.02	0.05	-
b	0.20	0.25	0.30	(1)
D	3.90	4.00	4.10	-
D2	2.55	2.60	2.65	-
E	3.90	4.00	4.10	-
E2	2.55	2.60	2.65	-
e	-	0.50	-	-
L	0.35	0.40	0.45	-
k	-	0.30	-	-
ddd	-	0.05	-	-

1. Dimension “b” does not include the dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm.

Figure 16. TFQFPN 4 x 4 x 1.05 - 24L suggested footprint



9 Ordering information

Table 14. Device summary

Order code	Package	Packaging
STSPIN820	TFQFPN 4 x 4 x 1.05 - 24 L	Tape and reel

10 Revision history

Table 15. Document revision history

Date	Revision	Changes
27-Sep-2017	1	Initial release.
19-Dec-2017	2	Added *Section 2.3: Thermal data on page 6*. Added *Note: on page 17*. Minor modifications throughout document.