

nRF52832 - Product Specification v1.0



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1 Revision history

Date	Version	Description
February 2016	1.0	First release.



2 About this document

This Product Specification is organized into chapters based on the modules and peripherals that are available in this IC.

The peripheral descriptions are broken into separate sections that include the following information:

- A detailed functional description of the peripheral.
- · Register configuration for the peripheral
- Electrical specification tables providing the specified limits of the chip when tested under the conditions defined in the *Recommended operating conditions* on page 17

2.1 Peripheral naming and abbreviations

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM® Cortex® Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

2.2 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.2.1 Fields and values

The Id (Field Id) row specifies the bits that belong to the different fields in the register.

A blank space means that the field is reserved and that it is read as undefined, and must be written as '0' to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column.

If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column. Single-bit bit fields may, however, omit the **Value Id** when values can be substituted with a Boolean type enumerator range, for example, True/False, Disable/Enable, On/Off, and so on.

Values are usually provided as decimal or hexadecimal. Hex values have a '0x' prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example, 1, 3, 9.
- Range of values, e.g. [0..4], that is, all values from and including 0 and 4.
- Implicit values. If no values are indicated in the Value column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value** Id, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with "..".

When an item is marked with the word **Deprecated**, it means this is an attribute applied to a feature to indicate that it should not be used for new designs.



2.3 Registers

Table 1: Register Overview

Register	Offset	Description			
DUMMY	0x514	Example of a register controlling a dummy feature			

2.3.1 **DUMMY**

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number		31	30 2	29 2	8 2	7 2	6 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14 :	l3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id					[) [) D	D						С	С	С							В						Α	Α
Reset 0x00050002		0	0	0 (0 0) (0	0	0	0	0	0	0	1	0	1	0	0	0 (0	0	0	0	0	0	0	0	0 0) 1	0
Id RW Field Va	alue Id	Va	lue						D	escr	ipti	on																		
A RW FIELD_A									Ex	kam	ple	of a	fiel	d w	ith	sev	/era	l er	ium	erat	ted	valu	es							
Di	isabled	0 The example feature is disabled																												
No	ormalMode	1 The example feature is enabled in normal mode																												
Ex	ktendedMode	2 The example feature is enabled along with extra functionality					ctionality																							
B RW FIELD_B									Ex	kam	ple	of a	dep	ored	ate	d f	ield										[Depr	reca	:ed
Di	Disabled 0			The override feature is disabled					0																					
Er	nabled	1							Th	he o	verr	ide	fea	ture	e is	ena	able	d												
C RW FIELD_C									Ex	kam	ple	of a	fiel	d w	ith	a v	alid	rar	ige (of v	alue	es.								
Va	alidRange	[2	.7]						Ex	kam	ple	of a	llow	/ed	val	ues	for	thi	s fie	ld										
D RW FIELD_D									Ex	kam	ple	of a	fiel	d w	ith	no	res	tric	tion	on	the	valu	ıes							



3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

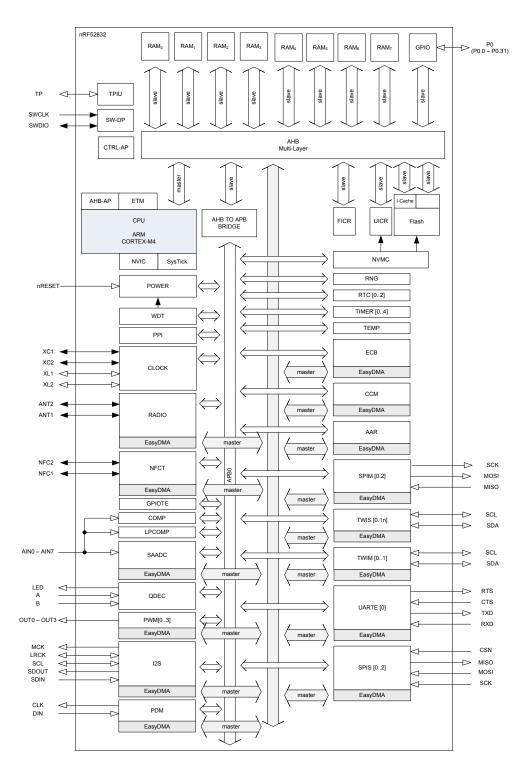


Figure 1: Block diagram



4 Pin assignments

Here we cover the pin assignments for each variant of the chip.

4.1 QFN48 pin assignments

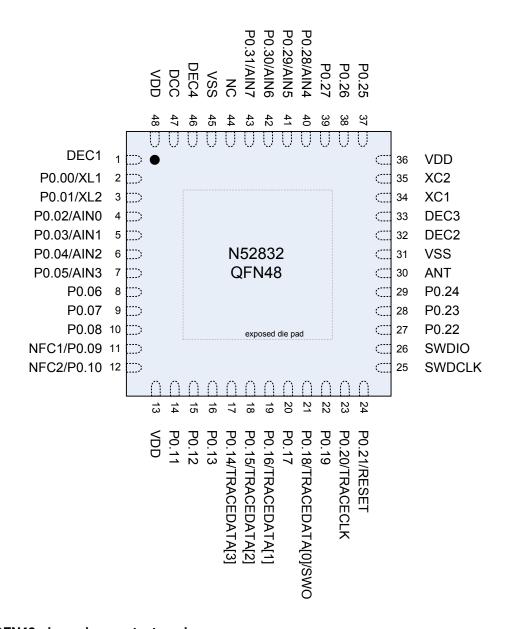


Figure 2: QFN48 pin assignments, top view

Table 2: QFN48 pin assignments

Pin Name		Туре	Description						
Left Side of chip									
1	DEC1	Power	0V9 regulator digital supply decoupling.						
2	P0.00	Digital I/O	General purpose I/O pin.						
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO).						
3	P0.01	Digital I/O	General purpose I/O pin.						



Pin	Name	Туре	Description
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO).
4	P0.02	Digital I/O	General purpose I/O pin.
	AIN0	Analog input	SAADC/COMP/LPCOMP input.
5	P0.03	Digital I/O	General purpose I/O pin.
•		- ·	
_	AIN1	Analog input	SAADC/COMP/LPCOMP input.
6	P0.04	Digital I/O	General purpose I/O pin.
	AIN2	Analog input	SAADC/COMP/LPCOMP input.
7	P0.05	Digital I/O	General purpose I/O pin.
	AIN3	Analog input	SAADC/COMP/LPCOMP input.
8	P0.06	Digital I/O	General purpose I/O pin.
9	P0.07	Digital I/O	General purpose I/O pin.
10	P0.08	Digital I/O	General purpose I/O pin.
11	NFC1	NFC input	NFC antenna connection.
	P0.09	Digital I/O	General purpose I/O pin ¹
12	NFC2	NFC input	NFC antenna connection.
12	INFCZ		
	P0.10	Digital I/O	General purpose I/O pin ¹
Bottom side of chip			
13	VDD	Power	Power-supply pin.
14	P0.11	Digital I/O	General purpose I/O pin.
15	P0.12	Digital I/O	General purpose I/O pin.
16	P0.13	Digital I/O	General purpose I/O pin.
17	P0.14	Digital I/O	General purpose I/O pin.
	TRACEDATA[3]		Trace port output.
18	P0.15	Digital I/O	General purpose I/O pin.
	TRACEDATA[2]		Trace port output.
19	P0.16	Digital I/O	General purpose I/O pin.
		- 18.11.1, 0	
••	TRACEDATA[1]	a. v. 1./a	Trace port output.
20	P0.17	Digital I/O	General purpose I/O pin.
21	P0.18	Digital I/O	General purpose I/O pin.
	TRACEDATA[0] / SWO		Single Wire Output.
			Trace port output.
22	P0.19	Digital I/O	General purpose I/O pin.
23	P0.20	Digital I/O	General purpose I/O pin.
	TRACECLK		Trace port clock output.
24	PO.21	Digital I/O	· · ·
24	PU.21	Digital I/O	General purpose I/O pin.
	RESET		Configurable as pin reset.
Right Side of chip			
25	SWDCLK	Digital input	Serial Wire Debug clock input for debug
			and programming.
26	SWDIO	Digital I/O	Serial Wire Debug I/O for debug and
			programming.
27	P0.22	Digital I/O	General purpose I/O pin ²
28	P0.23	Digital I/O	General purpose I/O pin ²
29	P0.24	Digital I/O	General purpose I/O pin ²
30	ANT	RF	Single-ended radio antenna connection.
31	VSS	Power	Ground pin (Radio supply).
32	DEC2	Power	1V3 regulator supply decoupling (Radio supply).
33	DEC3	Power	Power supply decoupling.
34	XC1	Analog input	Connection for 32 MHz crystal.
35	XC2	Analog input	Connection for 32 MHz crystal.
36	VDD	Power	Power-supply pin.



Pin	Name	Туре	Description
37	P0.25	Digital I/O	General purpose I/O pin ²
38	P0.26	Digital I/O	General purpose I/O pin ²
39	P0.27	Digital I/O	General purpose I/O pin ²
40	P0.28	Digital I/O	General purpose I/O pin ²
	AIN4	Analog input	SAADC/COMP/LPCOMP input.
41	P0.29	Digital I/O	General purpose I/O pin ²
	AIN5	Analog input	SAADC/COMP/LPCOMP input.
42	P0.30	Digital I/O	General purpose I/O pin ²
	AIN6	Analog input	SAADC/COMP/LPCOMP input.
43	P0.31	Digital I/O	General purpose I/O pin ²
	AIN7	Analog input	SAADC/COMP/LPCOMP input.
44	NC		No connect pin. Leave unconnected.
45	VSS	Power	Ground pin.
46	DEC4	Power	1V3 regulator supply decoupling.
			Input from DC/DC regulator. Output from
			1.3 V LDO.
47	DCC	Power	DC/DC regulator output pin.
48	VDD	Power	Power-supply pin.
Bottom of chip			
Die pad	VSS	Power	Ground pad. Exposed die pad must be
			connected to ground (VSS) for proper
			device operation.

See *NFC antenna pins* on page 110 for more information.

See *GPIO located near the radio* on page 109 for more information.



5 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 3: Absolute maximum ratings

	Note	Min.	Max.	Unit
Supply voltages				
VDD		-0.3	+3.9	V
VSS			0	V
I/O pin voltage				
V _{I/O} , VDD ≤3.6 V		-0.3	VDD + 0.3 V	V
V _{I/O} , VDD >3.6 V		-0.3	3.9 V	V
NFC antenna pin current				
I _{NFC1/2}			80	mA
Radio				
RF input level			10	dBm
Environmental (QFN package)				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model		4	kV
ESD CDM _{QF}	Charged Device Model		750	V
	(QFN48, 6x6 mm package)			
Flash memory				
Endurance		10 000		Write/erase cycles
Retention		10 years at 40°C		





6 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 4: Recommended operating conditions

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Supply voltage, independent of DCDC enable		1.7	3.0	3.6	V
t_{R_VDD}	Supply rise time (0 V to 1.7 V)				60	ms
TĀ	Operating temperature		-40	25	85	°C

Important: The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.



7 CPU

The ARM® Cortex®-M4 processor with floating-point unit (FPU) has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- · Hardware divide
- 8 and 16-bit single instruction multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the Nested Vectored Interrupt Controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 Series. An instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see *Cache* on page 27. The section *Electrical Specification* on page 18 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

7.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions when used due to e.g. overflow or underflow. These exceptions will trigger the FPU interrupt (see *Instantiation* on page 21). To clear the IRQ line when an exception has occurred, the relevant exception bit within the FPSCR register needs to be cleared. For more information about the FPSCR or other FPU registers, see *Cortex-M4 Devices Generic User Guide*.

7.2 Electrical Specification

7.2.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark[™] benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Тур.	Max.	Units
W _{FLASH}	CPU wait states, running from flash, cache disabled	0		2	
W _{FLASHCACHE}	CPU wait states, running from flash, cache enabled	0		3	
W _{RAM}	CPU wait states, running from RAM			0	
I _{DDFLASHCACHE}	CPU current, running from flash, cache enabled, LDO		7.4		mA
I _{DDFLASHCACHEDCDC}	CPU current, running from flash, cache enabled, DCDC 3V		3.7		mA
I _{DDFLASH}	CPU current, running from flash, cache disabled, LDO		8.0		mA
I _{DDFLASHDCDC}	CPU current, running from flash, cache disabled, DCDC 3V		3.9		mA
I _{DDRAM}	CPU current, running from RAM, LDO		6.7		mA
I _{DDRAMDCDC}	CPU current, running from RAM, DCDC 3V		3.3		mA
I _{DDFLASH/MHz}	CPU efficiency, running from flash, cache enabled, LDO		125		μΑ/
					MHz
I _{DDFLASHDCDC/MHz}	CPU efficiency, running from flash, cache enabled, DCDC 3V		58		μΑ/
					MHz



Symbol	Description	Min.	Тур.	Max.	Units
CM_{FLASH}	CoreMark ³ , running from flash, cache enabled		215		CoreN
$CM_{FLASH/MHz}$	CoreMark per MHz, running from flash, cache enabled		3.36		CoreN
					MHz
CM _{FLASH/mA}	CoreMark per mA, running from flash, cache enabled, DCDC 3V		58		CoreN
					mA

7.3 CPU and support module configuration

The ARM® Cortex®-M4 processor has a number of CPU options and support modules implemented on the device.

Option / Module	Description	Implemented
Core options		
NVIC	Nested Vector Interrupt Controller	37 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup Interrupt Controller	NO
Endianness	Memory system endianness	Little endian
Bit Banding	Bit banded memory	NO
DWT	Data Watchpoint and Trace	YES
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating point unit	YES
DAP	Debug Access Port	YES
ETM	Embedded Trace Macrocell	YES
ITM	Instrumentation Trace Macrocell	YES
TPIU	Trace Port Interface Unit	YES
ETB	Embedded Trace Buffer	NO
FPB	Flash Patch and Breakpoint Unit	YES
HTM	AHB Trace Macrocell	NO

³ Using IAR v6.50.1.4452 with flags --endian=little --cpu=Cortex-M4 -e --fpu=VFPv4_sp -Ohs --no_size_constraints



8 Memory

The nRF52832 contains Flash and RAM that can be used for code and data storage.

The amount of RAM and Flash will vary depending on variant, see *Table 5: Memory variants* on page 20.

Table 5: Memory variants

Device name	RAM	Flash	Comments
nRF52832	64 kBvte	512 kBvte	

The CPU and the EasyDMA can access memory via the AHB multilayer interconnect. The CPU is also able to access peripherals via the AHB multilayer interconnect, as illustrated in *Figure 3: Memory layout* on page 20.

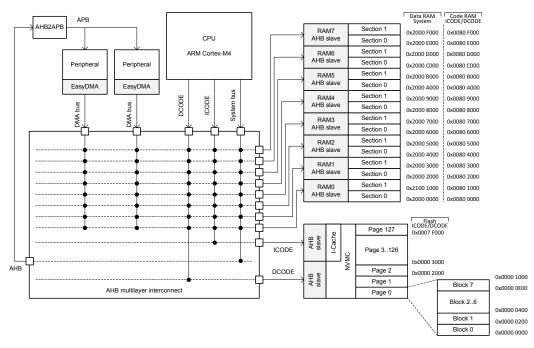


Figure 3: Memory layout

See *AHB multilayer* on page 23 and *EasyDMA* on page 24 for more information about the AHB multilayer interconnect and the EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

8.1 RAM - Random access memory

The RAM interface is divided into multiple RAM AHB slaves.

Each RAM AHB slave is connected to two 4-kilobyte RAM sections, see Section 0 and Section 1 in *Figure 3: Memory layout* on page 20.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the *POWER — Power supply* on page 76).

8.2 Flash - Non-volatile memory

The Flash can be read an unlimited number of times by the CPU, but it has restrictions on the number of times it can be written and erased and also on how it can be written.



Writing to Flash is managed by the Non-volatile memory controller (NVMC), see *NVMC — Non-volatile memory controller* on page 26.

The Flash is divided into multiple pages that can be accessed by the CPU via both the ICODE and DCODE buses as shown in, *Figure 3: Memory layout* on page 20. Each page is divided into 8 blocks.

8.3 Memory map

The complete memory map is shown in *Figure 4: Memory map* on page 21. As described in *Memory* on page 20, Code RAM and the Data RAM are the same physical RAM.

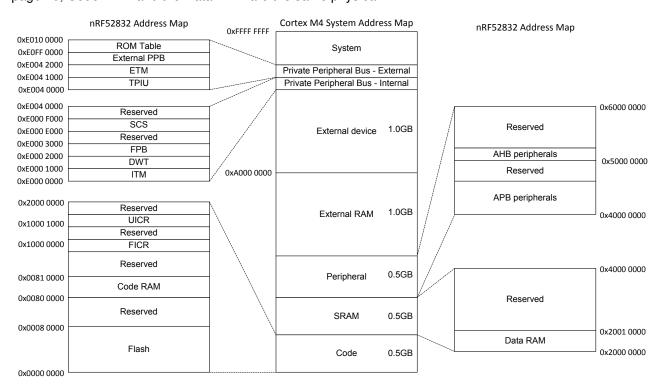


Figure 4: Memory map

8.4 Instantiation

Table 6: Instantiation table

ID	Base Address	Peripheral	Instance	Description	
0	0x40000000	CLOCK	CLOCK	Clock control	
0	0x40000000	POWER	POWER	Power Control	
0	0x40000000	BPROT	BPROT	Block Protect	
1	0x40001000	RADIO	RADIO	2.4 GHz radio	
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/Transmitter	Deprecated
2	0x40002000	UARTE	UARTE0	Universal Asynchronous Receiver/Transmitter with EasyDMA	
3	0x40003000	TWIM	TWIM0	Two-wire interface master 0	
3	0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
3	0x40003000	SPIM	SPIM0	SPI master 0	
3	0x40003000	SPIS	SPIS0	SPI slave 0.	
3	0x40003000	SPI	SPI0	SPI master 0	Deprecated
3	0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
4	0x40004000	SPI	SPI1	SPI master 1	Deprecated
4	0x40004000	TWIS	TWIS1	Two-wire interface slave 1	
4	0x40004000	SPIM	SPIM1	SPI master 1	
4	0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated



ID	Base Address	Peripheral	Instance	Description	
4	0x40004000	TWIM	TWIM1	Two-wire interface master 1	
4	0x40004000	SPIS	SPIS1	SPI slave 1	
5	0x40005000	NFCT	NFCT	Near Field Communication Tag	
6	0x40006000	GPIOTE	GPIOTE	GPIO tasks and events	
7	0x40007000	SAADC	SAADC	Analog to digital converter	
8	0x40008000	TIMER	TIMER0	Timer 0	
9	0x40009000	TIMER	TIMER1	Timer 1	
10	0x4000A000	TIMER	TIMER2	Timer 2	
11	0x4000B000	RTC	RTC0	Real-time counter 0	
12	0x4000C000	TEMP	TEMP	Temperature Sensor	
13	0x4000D000	RNG	RNG	Random Number Generator	
14	0x4000E000	ECB	ECB	AES ECB Mode Encryption	
15	0x4000F000	ССМ	CCM	AES CCM Mode Encryption	
15	0x4000F000	AAR	AAR	Accelerated Address Resolver	
16	0x40010000	WDT	WDT	Watchdog Timer	
17	0x40011000	RTC	RTC1	Real-time counter 1	
18	0x40012000	QDEC	QDEC	Quadrature decoder	
19	0x40013000	LPCOMP	LPCOMP	Low power comparator	
19	0x40013000	COMP	COMP	General Purpose Comparator	
20	0x40014000	EGU	EGU0	Event Generator Unit 0	
20	0x40014000	SWI	SWI0	Software interrupt 0	
21	0x40015000	SWI	SWI1	Software interrupt 1	
21	0x40015000	EGU	EGU1	Event Generator Unit 1	
22	0x40016000	SWI	SWI2	Software interrupt 2	
22	0x40016000	EGU	EGU2	Event Generator Unit 2	
23	0x40017000	SWI	SWI3	Software interrupt 3	
23	0x40017000	EGU	EGU3	Event Generator Unit 3	
24	0x40018000	EGU	EGU4	Event Generator Unit 4	
24	0x40018000	SWI	SWI4	Software interrupt 4	
25	0x40019000	SWI	SWI5	Software interrupt 5	
25	0x40019000	EGU	EGU5	Event Generator Unit 5	
26	0x4001A000	TIMER	TIMER3	Timer 3	
27	0x4001B000	TIMER	TIMER4	Timer 4	
28	0x4001C000	PWM	PWM0	Pulse Width Modulation Unit 0	
29	0x4001D000	PDM	PDM	Pulse Density Modulation (Digital Microphone) Interface	
30	0x4001E000	NVMC	NVMC	Non Volatile Memory Controller	
31	0x4001F000	PPI	PPI	PPI controller	
32	0x40020000	MWU	MWU	Memory Watch Unit	
33	0x40021000	PWM	PWM1	Pulse Width Modulation Unit 1	
34	0x40022000	PWM	PWM2	Pulse Width Modulation Unit 2	
35	0x40023000	SPI	SPI2	SPI master 2.	Deprecated
35	0x40023000	SPIS	SPIS2	SPI slave 2.	
35	0x40023000	SPIM	SPIM2	SPI master 2.	
36	0x40024000	RTC	RTC2	Real-time counter 2.	
37	0x40025000	125	I2S	Inter-IC Sound interface	
38	0x40026000	FPU	FPU	FPU interrupt	
N/A	0x10000000	FICR	FICR	Factory Information Configuration	
N/A	0x10001000	UICR	UICR	User Information Configuration	
N/A	0x50000000	GPIO	PO	General purpose input and output	
N/A	0x50000000	GPIO	GPIO	General purpose input and output	Deprecated
				•	



9 AHB multilayer

The CPU and all of the EasyDMAs are AHB bus masters on the AHB multilayer, while the RAM and various other modules are AHB slaves.

See Figure 1: Block diagram on page 12 for an overview of which peripherals implement EasyDMA.

The CPU has exclusive access to all AHB slaves except for the RAM that can also be accessed by the EasyDMA.

Access rights to each of the RAM AHB slaves are resolved using the priority of the different bus masters in the system

See *AHB multilayer priorities* on page 23 for information about the priority of the different AHB bus masters in the system. It is possible for two or more bus masters to have the same priority in cases where it is guaranteed by design that the related masters will never be able to access the same slave at the same time.

9.1 AHB multilayer priorities

Each master connected to the AHB multilayer is assigned a priority.

Table 7: AHB bus masters

Bus master name	Priority	Description
CPU	Highest priority	
SPIS1		Applies to SPIM1, SPIS1, TWIM1, TWIS1
RADIO		
CCM/ECB/AAR		
SAADC		
UARTE		
SERIALO		Applies to SPIMO, SPISO, TWIMO, TWISO
SERIAL2		Applies to SPIM2, SPIS2
NFCT		
12\$		12S
PDM		PDM
PWM	Lowest priority	Applies to PWM0, PWM1, PWM2



10 EasyDMA

EasyDMA is an easy-to-use direct memory access module that some peripherals implement to gain direct access to Data RAM.

The EasyDMA is an AHB bus master similar to the CPU and it is connected to the AHB multilayer interconnect for direct access to the Data RAM. The EasyDMA is not able to access the Flash.

A peripheral can implement multiple EasyDMA instances, for example to provide a dedicated channel for reading data from RAM into the peripheral at the same time as a second channel is dedicated for writing data to the RAM from the peripheral. This concept is illustrated in *Figure 5: EasyDMA example* on page 24

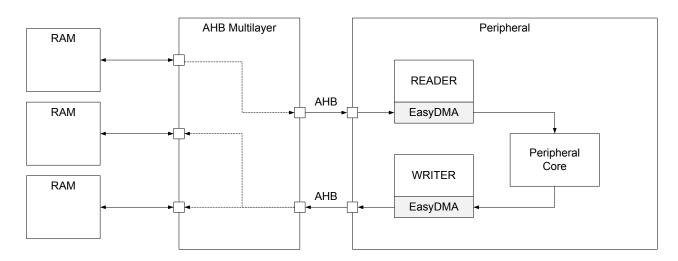


Figure 5: EasyDMA example

An EasyDMA channel is usually exposed to the user in the form illustrated below, but some variations may occur:

```
READERBUFFER_SIZE 5
WRITERBUFFER_SIZE 6

uint8_t readerBuffer[READERBUFFER_SIZE] __at__ 0x20000000;
uint8_t writerBuffer[WRITERBUFFER_SIZE] __at__ 0x20000005;

// Configuring the READER channel
MYPERIPHERAL->READER.MAXCNT = READERBUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &readerBuffer;

// Configure the WRITER channel
MYPERIPHERAL->WRITER.MAXCNT = WRITEERBUFFER_SIZE;
MYPERIPHERAL->WRITER.PTR = &writerBuffer;
```

This example shows a peripheral called MYPERIPHERAL that implements two EasyDMA channels, one for reading, called READER, and one for writing, called WRITER. When the peripheral is started, it is here assumed that the peripheral will read 5 bytes from the readerBuffer located in RAM at address 0x20000000, process the data and then write no more than 6 bytes back to the writerBuffer located in RAM at address 0x20000005. The memory layout of these buffers is illustrated in *Figure 6: EasyDMA memory layout* on page 25.



0x20000000	readerBuffer[0]	readerBuffer[1]	readerBuffer[2]	readerBuffer[3]
0x20000004	readerBuffer[4]	writerBuffer[0]	writerBuffer[1]	writerBuffer[2]
0x20000008	writerBuffer[3]	writerBuffer[4]	writerBuffer[5]	

Figure 6: EasyDMA memory layout

The EasyDMA channel's MAXCNT register cannot be specified larger than the actual size of the buffer. If, for example, the WRITER.MAXCNT register is specified larger than the size of the writerBuffer, the WRITER EasyDMA channel may overflow the writerBuffer.

After the peripheral has completed the EasyDMA transfer, the CPU can read the EasyDMA channel's AMOUNT register to see how many bytes that were transferred, e.g. it is possible for the CPU to read the MYPERIPHERAL->WRITER.AMOUNT register to see how many bytes the WRITER wrote to RAM.

10.1 EasyDMA array list

The EasyDMA is able to operate in a mode called array list.

The EasyDMA array list can be represented by the data structure ArrayList_type illustrated in the code example below.

This data structure includes only a buffer with size equal to READER.MAXCNT. EasyDMA will use the READER.MAXCNT register to determine when the buffer is full.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
   uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3];

READER.MAXCNT = BUFFER_SIZE;
READER.PTR = &ReaderList;
```

READER.PTR = &ReaderList

0x20000000 : ReaderList[0]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000004 : ReaderList[1]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000008 : ReaderList[2]	buffer[0]	buffer[1]	buffer[2]	buffer[3]

Figure 7: EasyDMA array list



11 NVMC — Non-volatile memory controller

The Non-volatile memory controller (NVMC) is used for writing and erasing the internal Flash memory and the UICR.

Before a write can be performed, the NVMC must be enabled for writing in CONFIG.WEN. Similarly, before an erase can be performed, the NVMC must be enabled for erasing in CONFIG.EEN, see *CONFIG* on page 28. The user must make sure that writing and erasing are not enabled at the same time. Failing to do so may result in unpredictable behavior.

11.1 Writing to Flash

When writing is enabled, the Flash is written by writing a full 32-bit word to a word-aligned address in the Flash.

The NVMC is only able to write '0' to bits in the Flash that are erased, that is, set to '1'. It cannot write back a bit to '1'.

As illustrated in *Figure 3: Memory layout* on page 20, the Flash is divided into multiple pages that are further divided into multiple blocks. The same block in the Flash can only be written *n_{WRITE}* number of times before an erase must be performed using *ERASEPAGE* or *ERASEALL*. See the memory size and organization in *Memory* on page 20 for block size.

Only full 32-bit words can be written to Flash using the NVMC interface. To write less than 32 bits to Flash, write the data as a word, and set all the bits that should remain unchanged in the word to '1'. Note that the restriction about the number of writes (see above) still applies in this case.

The time it takes to write a word to the Flash is specified by t_{WRITE} . The CPU is halted while the NVMC is writing to the Flash.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a hard fault.

11.2 Erasing a page in Flash

When erase is enabled, the Flash can be erased page by page using the ERASEPAGE register.

After erasing a Flash page, all bits in the page are set to '1'. The time it takes to erase a page is specified by $t_{ERASEPAGE}$. The CPU is halted while the NVMC performs the erase operation.

11.3 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as Flash. After UICR has been written, the new UICR configuration will only take effect after a reset.

UICR can only be written n_{WRITE} number of times before an erase must be performed using ERASEUICR or ERASEALL.

The time it takes to write a word to the UICR is specified by t_{WRITE} . The CPU is halted while the NVMC is writing to the UICR.

11.4 Erasing user information configuration registers (UICR)

When erase is enabled, UICR can be erased using the ERASEUICR register.

After erasing UICR all bits in UICR are set to '1'. The time it takes to erase UICR is specified by $t_{ERASEPAGE}$. The CPU is halted while the NVMC performs the erase operation.



11.5 Erase all

When erase is enabled, the whole Flash and UICR can be erased in one operation by using the ERASEALL register. ERASEALL will not erase the factory information configuration registers (FICR).

The time it takes to perform an ERASEALL command is specified by $t_{ERASEALL}$. The CPU is halted while the NVMC performs the erase operation.

11.6 Cache

An instruction cache (I-Cache) can be enabled for the ICODE bus in the NVMC.

See the Memory map in *Memory map* on page 21 for the location of Flash.

A cache hit is an instruction fetch from the cache, and it has a 0 wait-state delay. The number of wait-states for a cache miss, where the instruction is not available in the cache and needs to be fetched from Flash, depends on the processor frequency and is shown in *CPU* on page 18

Enabling the cache can increase CPU performance and reduce power consumption by reducing the number of wait cycles and the number of flash accesses. This will depend on the cache hit rate. Cache will use some current when enabled. If the reduction in average current due to reduced flash accesses is larger than the cache power requirement, the average current to execute the program code will reduce.

When disabled, the cache does not use current and does not retain its content.

It is possible to enable cache profiling to analyze the performance of the cache for your program using the *ICACHECNF* register. When profiling is enabled, the *IHIT* and *IMISS* registers are incremented for every instruction cache hit or miss respectively. The hit and miss profiling registers do not wrap around after reaching the maximum value. If the maximum value is reached, consider profiling for a shorter duration to get correct numbers.

11.7 Registers

Table 8: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001E000	NVMC	NVMC	Non Volatile Memory Controller	

Table 9: Register Overview

Register	Offset	Description	
READY	0x400	Ready flag	
CONFIG	0x504	Configuration register	
ERASEPAGE	0x508	Register for erasing a page in Code area	
ERASEPCR1	0x508	Register for erasing a page in Code area. Equivalent to ERASEPAGE.	Deprecated
ERASEALL	0x50C	Register for erasing all non-volatile user memory	
ERASEPCR0	0x510	Register for erasing a page in Code area. Equivalent to ERASEPAGE.	Deprecated
ERASEUICR	0x514	Register for erasing User Information Configuration Registers	
ICACHECNF	0x540	I-Code cache configuration register.	
IHIT	0x548	I-Code cache hit counter.	
IMISS	0x54C	I-Code cache miss counter.	

11.7.1 READY

Address offset: 0x400

Ready flag



Bitı	numb	er		31	30 2	9 2	8 27	7 26	5 25	5 24	23	22	21	20	19	18 1	17 1	6 1	5 14	1 13	12	11	10 9	8	7	6	5	4	3	2 1	1 0
Id																															Α
Res	et 0x(0000000		0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0
Id	RW	Field	Value Id	Val	ue						De	scri	ipti	on																	
Α	R	READY									N۷	/MC	is	reac	dy o	r bu	ısy														
			Busy	0							N۷	/MC	is	busy	y (o	n-go	oing	wri	te c	r er	ase	ope	ratio	on)							
			Ready	1							N۷	/MC	is	reac	dy																

11.7.2 **CONFIG**

Address offset: 0x504 Configuration register

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21 2	20 :	19 1	18	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																				
Α	RW	WEN										Pro	ogra	m n	nen	nor	y ac	cces	s n	nod	e. I	t is	str	ong	ly r	eco	mm	nen	ded	t					
												to	only	act	iva	te e	ras	se a	nd	wri	te r	no	des	wh	en '	the	y ar	e a	ctiv	ely	,				
												use	ed. E	Enab	olin	g w	rite	or	era	se	wil	inv	vali	dat	e th	e c	ach	e a	nd	kee	p				
												it i	nval	idat	ed.																				
			Ren	0								Rea	ad o	nly	acc	ess																			
			Wen	1								Wr	ite l	Enal	ole	t																			
			Een	2								Era	ise e	enat	olec	i																			

11.7.3 ERASEPAGE

Address offset: 0x508

Register for erasing a page in Code area

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15 1	14 1	13 1	12 1	11 1	.0 9	9 (3 7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	Α ,	Δ ,	4 4	Α Α	. Δ	A	Α	Α	Α	Α	А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							De	scri	ptio	n																			
Α	RW	ERASEPAGE										Re	gist	er fo	or s	tar	ing	era	se	of a	ра	ge i	in C	ode	are	a								
												Th	e va	lue	is t	he	ado	lres	s to	the	e pa	ige '	to b	e e	rase	ed.	(Ad	dre	sses	s of				
												firs	st w	ord	in į	pag	e).	Not	e tl	hat	cod	e ei	rase	e ha	s to	be	ena	able	d b	У				
												СО	NFI	G.EI	ΕN	bef	ore	the	pa	ige (can	be	era	sed	. At	ten	npts	to	era	se				
												pa	ges	that	ar	e o	uts	de 1	he	coc	le a	rea	ma	y r	esul	t in	und	desi	rab	le				
												be	hav	iour	, e.	g. t	he	wro	ng	pag	e m	nay	be e	eras	sed.									

11.7.4 ERASEPCR1 (Deprecated)

Address offset: 0x508

Register for erasing a page in Code area. Equivalent to ERASEPAGE.

Bit	numb	er		31	L 30	29	28	27	26	25	24	23 :	22 2	1 2	0 1	9 1	3 17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 Α	4 Δ		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Д	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							Des	crip	tio	n																		
Α	RW	ERASEPCR1										Reg	iste	r fo	r era	asin	g a	pag	e in	Со	de a	rea	. Ec	uiv	/ale	nt i	to						
												ERA	SEP	AGI	E.																		

11.7.5 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory



Bit r	numbe	r		31	1 30	29	28	3 27	7 26	5 25	5 2	4 2	3 2	2 2	1 2	0 1	9 1	.8 1	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																				Α
Res	et 0x0	0000000		0	0	0	0	0	0	0) () () (0) () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	!						D	esc	ript	tior	1																				
Α	RW	ERASEALL										Ε	rase	e all	l no	n-v	/ola	tile	e m	em	ory	/ in	clud	ding	UI	CR ı	regi	iste	rs.	Not	te					
												tl	nat	cod	le e	ras	e h	as '	to k	e e	ena	ble	d b	y C	INC	IG.	EEN	N b	efo	re t	he					
												U	ICR	cai	n be	e er	rase	ed.																		
			NoOperation	0								N	lo o	per	atio	on																				
			Erase	1								S	tart	chi	ip e	ras	e																			

11.7.6 ERASEPCR0 (Deprecated)

Address offset: 0x510

Register for erasing a page in Code area. Equivalent to ERASEPAGE.

Bit r	numbe	er		31	1 30	29	28	3 27	7 26	25	5 24	1 23	22	21	20	19	18	17	16	15	14	13 1	.2 1	11 1	.0	9	8	7	6	5	4	3	2	1 0	ı
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ.	A ,	Д	Α	Α	Α	Α	Α	Α	Α .	Δ.	ΑА	l
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	l
Id	RW	Field	Value Id	Va	alue							De	scr	ipti	on																				l
Α	RW	ERASEPCR0										Re	gist	er f	or s	tar	ting	era	se	of a	ра	ge i	n C	ode	ar	ea.	Eq	uiv	aler	nt to	o				١
												ER	ASI	PA	GE.																				

11.7.7 ERASEUICR

Address offset: 0x514

Register for erasing User Information Configuration Registers

Bitı	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	3 12	2 1	1 10	0 9	9 8	3 7	7 6	5 5	5 4	1 3	2	1	. 0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () () () () () (0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																				
Α	RW	ERASEUICR										Re	gist	er s	star	ting	g er	ase	of	all	Use	er lı	nfo	rma	atio	n C	ont	figu	rat	ion					
												Re	gist	ers	. No	ote	tha	it co	ode	era	ase	has	s to	be	en	abl	ed	by							
												CC	NF	IG.E	EN	be	for	e th	ie U	JICF	R ca	ın b	e e	ras	ed.										
			NoOperation	0								No	ор	era	tio	n																			
			Erase	1								Sta	art e	eras	e c	of U	ICR																		

11.7.8 ICACHECNF

Address offset: 0x540

I-Code cache configuration register.

Bit	numbe	r		31	. 30	29	28	8 27	7 2	6 2	5 2	24 :	23 :	22	21	20	19	9 18	8 1	7 1	6 1	15 :	14 :	13 :	12	11 :	10	9	8	7	6	5	4	3	2	1 ()
Id																													В							1	Д
Res	et 0x0	0000000		0	0	0	0	0	(0 ()	0	0	0	0	0	0	0) () ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							ı	Des	cri	pti	on																					
Α	RW	CACHEEN										(Cac	he	en	abl	e																				
			Disabled	0								-	Disa	abl	e ca	ach	e.	Inv	alio	date	es a	all c	ach	e e	ntr	ies.											
			Enabled	1								-	Ena	ble	e ca	che	е																				
В	RW	CACHEPROFEN										(Cac	he	pro	ofili	ing	en	ab	le																	
			Disabled	0								- 1	Disa	abl	e ca	ach	e p	oro	filir	ng																	
			Enabled	1								-	Ena	ble	e ca	che	ер	rof	ilin	g																	

11.7.9 IHIT

Address offset: 0x548
I-Code cache hit counter.

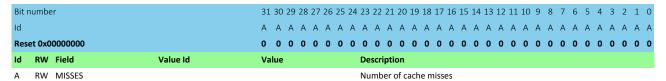


Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	13 1	12 1	11 1	.0 9	9 8	3 7	' 6	5 5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α .	A ,	Δ .	۱ ۸	4 <i>A</i>	\ <i>A</i>	A A	Α	Α	Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0) (0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	HITS										Nu	mb	er o	f ca	che	e hit	ts															

11.7.10 IMISS

Address offset: 0x54C

I-Code cache miss counter.



11.8 Electrical Specification

11.8.1 Flash programming

Symbol	Description	Min.	Тур. М	ax. Units	
n _{WRITE,BLOCK}	Amount of writes allowed in a block between erase		18	1	
t _{WRITE}	Time to write one word	67.5	33	8 μs	
t _{ERASEPAGE}	Time to erase one page	2.05	89	.7 ms	
t _{ERASEALL}	Time to erase all flash	6.72	29	5.3 ms	

11.8.2 Cache size

Symbol	Description	Min.	Тур.	Max.	Units
Size _{ICODE}	I-Code cache size		2048		Bytes



12 BPROT — Block protection

The mechanism for protecting non-volatile memory can be used to prevent application code from erasing or writing to protected blocks.

Non-volatile memory can be protected from erases and writes depending on the settings in the CONFIG registers. One bit in a CONFIG register represents one protected block of 4 kB. There are four CONFIG registers of 32 bits, which means there are 128 protectable blocks in total.

Important: If an erase or write to a protected block is detected, the CPU will hard fault. If an ERASEALL operation is attempted from the CPU while any block is protected, it will be blocked and the CPU will hard fault.

On reset, all the protection bits are cleared. To ensure safe operation, the first task after reset must be to set the protection bits. The only way of clearing protection bits is by resetting the device from any reset source.

The protection mechanism is turned off when in debug interface mode (a debugger is connected) and the DISABLEINDEBUG register is set to disable. For more information, see *Debug and trace* on page 70.

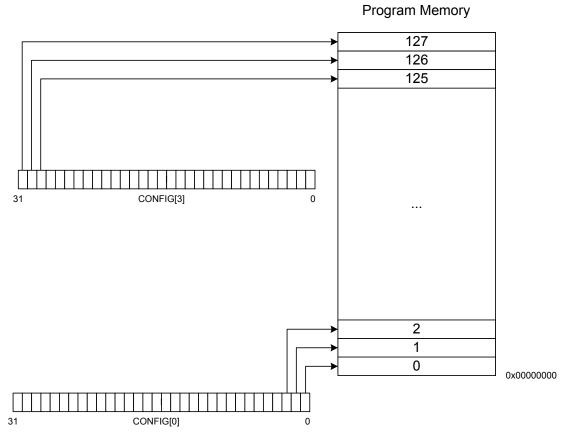


Figure 8: Protected regions of program memory

12.1 Registers

Table 10: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40000000	BPROT	BPROT	Block Protect		



Table 11: Register Overview

Register	Offset	Description	
CONFIG0	0x600	Block protect configuration register 0	
CONFIG1	0x604	Block protect configuration register 1	
DISABLEINDEBUG	0x608	Disable protection mechanism in debug interface mode	
	0x60C		Reserved
CONFIG2	0x610	Block protect configuration register 2	
CONFIG3	0x614	Block protect configuration register 3	

12.1.1 CONFIG0

Address offset: 0x600

Block protect configuration register 0

	numbe	er			23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				fedcbaZY	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
A	RW	REGION0			Enable protection for region 0. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
В	RW	REGION1			Enable protection for region 1. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
С	RW	REGION2			Enable protection for region 2. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
D	RW	REGION3			Enable protection for region 3. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
E	RW	REGION4			Enable protection for region 4. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
F	RW	REGION5			Enable protection for region 5. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
G	RW	REGION6			Enable protection for region 6. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
Н	RW	REGION7			Enable protection for region 7. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
ı	RW	REGION8			Enable protection for region 8. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
J	RW	REGION9			Enable protection for region 9. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
K	RW	REGION10			Enable protection for region 10. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
L	RW	REGION11			Enable protection for region 11. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
М	RW	REGION12	••		Enable protection for region 12. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enable
N	B/V	REGION13	LIMOICU	-	Enable protection for region 13. Write '0' has no effect.
1	KVV	VEGION13			Enable protection for region 15. write 0 has no effect.



Bit r	number			31 30	29 28 2	27 26	5 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x000	000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW F	ield	Value Id	Value				Description
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
0	RW R	REGION14						Enable protection for region 14. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
P	RW R	REGION15						Enable protection for region 15. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
Q	RW R	REGION16						Enable protection for region 16. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
R	RW R	REGION17						Enable protection for region 17. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
S	RW R	EGION18						Enable protection for region 18. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
Т	RW R	REGION19						Enable protection for region 19. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
U	RW R	REGION20						Enable protection for region 20. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
V	RW R	REGION21						Enable protection for region 21. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
W	RW R	REGION22						Enable protection for region 22. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
X	RW R	REGION23						Enable protection for region 23. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
Y	RW R	EGION24		_				Enable protection for region 24. Write '0' has no effect.
			Disabled	0				Protection disabled
_			Enabled	1				Protection enable
Z	RW R	EGION25	a					Enable protection for region 25. Write '0' has no effect.
			Disabled	0				Protection disabled
	D) 4/ D	VECTONIAS	Enabled	1				Protection enable
a	RW R	EGION26	D: 11 1	•				Enable protection for region 26. Write '0' has no effect.
			Disabled	0				Protection disabled
L	DVA/ D	AFCIONI27	Enabled	1				Protection enable
b	RW R	EGION27	Disabled	0				Enable protection for region 27. Write '0' has no effect.
			Disabled	0				Protection disabled
_	DIA/ D	AECIONI20	Enabled	1				Protection enable
С	ĸw R	EGION28	Disabled	0				Enable protection for region 28. Write '0' has no effect.
			Disabled	0				Protection disabled
d	D147 ~	IFCION30	Enabled	1				Protection enable
t	KW R	EGION29	Disabled	0				Enable protection for region 29. Write '0' has no effect.
			Disabled	0				Protection disabled
	Divi -	IFCION20	Enabled	1				Protection enable
9	KW R	EGION30	6: 11 1					Enable protection for region 30. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
	RW R	EGION31	5					Enable protection for region 31. Write '0' has no effect.
			Disabled	0				Protection disabled



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Enabled	1 Protection enable

12.1.2 CONFIG1

Address offset: 0x604

Block protect configuration register 1

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id				f e d c b a Z Y	'XWVUTSRQPONMLKJIHGFEDCB,
Rese	et 0x0	0000000		0 0 0 0 0 0 0 0	000000000000000000000000000000000000000
ld	RW	Field	Value Id	Value	Description
A	RW	REGION32			Enable protection for region 32. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
В	RW	REGION33			Enable protection for region 33. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
С	RW	REGION34			Enable protection for region 34. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
D	RW	REGION35			Enable protection for region 35. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
E	RW	REGION36			Enable protection for region 36. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
F	RW	REGION37			Enable protection for region 37. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
G	RW	REGION38			Enable protection for region 38. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
Н	RW	REGION39			Enable protection for region 39. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
I	RW	REGION40			Enable protection for region 40. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
J	RW	REGION41			Enable protection for region 41. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
K	RW	REGION42			Enable protection for region 42. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
L	RW	REGION43			Enable protection for region 43. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
М	RW	REGION44			Enable protection for region 44. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
N	RW	REGION45			Enable protection for region 45. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
0	RW	REGION46			Enable protection for region 46. Write '0' has no effect.



Bit n	umbe	r		31 30	29	9 28 2	27 20	5 25	24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d	С	b a	Z	Υ	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	t 0x0	0000000		0 0	0	0	0 0	0	0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value	е					Description
			Enabled	1						Protection enabled
Р	RW	REGION47								Enable protection for region 47. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
Q	RW	REGION48								Enable protection for region 48. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
R	RW	REGION49								Enable protection for region 49. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
S	RW	REGION50								Enable protection for region 50. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
Т	RW	REGION51								Enable protection for region 51. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
U	RW	REGION52								Enable protection for region 52. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
V	RW	REGION53								Enable protection for region 53. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
W	RW	REGION54								Enable protection for region 54. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
X	RW	REGION55								Enable protection for region 55. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
Υ	RW	REGION56								Enable protection for region 56. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
Z	RW	REGION57								Enable protection for region 57. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
а	RW	REGION58								Enable protection for region 58. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
b	RW	REGION59	5							Enable protection for region 59. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
С	RW	REGION60	D: 11 1	•						Enable protection for region 60. Write '0' has no effect.
			Disabled	0						Protection disabled
		25010110	Enabled	1						Protection enabled
d	RW	REGION61	5							Enable protection for region 61. Write '0' has no effect.
			Disabled	0						Protection disabled
	B	DECIONICA	Enabled	1						Protection enabled
е	RW	REGION62		_						Enable protection for region 62. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled
f	RW	REGION63								Enable protection for region 63. Write '0' has no effect.
			Disabled	0						Protection disabled
			Enabled	1						Protection enabled



12.1.3 DISABLEINDEBUG

Address offset: 0x608

Disable protection mechanism in debug interface mode

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 :	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																				
Α	RW	DISABLEINDEBUG										Disa	able	e th	e p	rot	ect	ion	me	cha	anis	m f	or I	IVI	∕l re	gic	ns	whi	ile						
												in d	lebu	ıg iı	nte	rfa	ce ı	no	de.	Thi	s re	gis	er	will	onl	y d	isal	ole 1	the						
												pro	tect	tior	n m	ech	nan	ism	if t	he	dev	ice	is i	n de	bu	g in	iter	fac	e m	od	e.				
			Disabled	1								Disa	able	e in	de	bug	3																		
			Enabled	0								Ena	ble	in (det	oug																			

12.1.4 CONFIG2

Address offset: 0x610

Block protect configuration register 2

	numbe	er		31 30	0 29	28 2	27 26	25 2	24 2	23 2	22 2:	1 20	19	18	17	16	15 1	4 1	3 12	2 11	10	9	8	7	6	5	4 3	3 2	1	0
Id				f e	e d	С	b a	Z	Υ :	X١	w v	/ U	Т	S	R	Q	P (N C	IM	l L	K	J	1	Н	G	F	E [) C	В	Α
Res	et 0x0	0000000		0 0	0	0	0 0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Valu	e				0	Des	cript	tion																		
Α	RW	REGION64							E	Enal	ble p	orote	ectio	on f	or re	egic	n 6	4. W	/rite	'0'	has	no	effe	ect.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					F	Prot	tecti	on e	nab	led																
В	RW	REGION65							E	Enal	ble p	orote	ectio	on f	or re	egic	n 6	5. W	/rite	'0'	has	no	effe	ect.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					P	Prot	tecti	on e	nab	led																
С	RW	REGION66							E	Enal	ble p	orote	ectio	on f	or r	egic	n 6	5. W	/rite	'0'	has	no	effe	ct.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					P	Prot	tecti	on e	nab	led																
D	RW	REGION67							E	Enal	ble p	orote	ectio	on f	or re	egic	n 6	7. W	/rite	'0'	has	no	effe	ct.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					P	Prot	tecti	on e	nab	led																
Ε	RW	REGION68							E	Enal	ble p	orote	ectio	on f	or r	egic	n 6	3. W	/rite	'0'	has	no	effe	ct.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					P	Prot	tecti	on e	nab	led																
F	RW	REGION69							E	Enal	ble p	orote	ectio	on f	or re	egic	n 6	9. W	/rite	'0'	has	no	effe	ct.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					P	Prot	tecti	on e	nab	led																
G	RW	REGION70							E	Enal	ble p	orote	ectio	on f	or re	egic	n 7). W	/rite	'0'	has	no	effe	ct.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					P	Prot	tecti	on e	nab	led																
Н	RW	REGION71							Е	Enal	ble p	orote	ectio	on f	or re	egic	n 7	1. W	/rite	'0'	has	no	effe	ct.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					P	Prot	tecti	on e	nab	led																
I	RW	REGION72							Е	Enal	ble p	orote	ectio	on f	or re	egic	n 7	2. W	/rite	'0'	has	no	effe	ct.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					P	Prot	tecti	on e	nab	led																
J	RW	REGION73							Е	Enal	ble p	orote	ectio	on f	or re	egic	n 7	3. W	/rite	'0'	has	no	effe	ct.						
			Disabled	0					P	Prot	tecti	on d	lisab	oled																
			Enabled	1					P	Prot	tecti	on e	nab	led																
K	RW	REGION74							Е	Enal	ble p	orote	ectio	on f	or re	egic	n 7	4. W	/rite	'0'	has	no	effe	ct.						
			Disabled	0					F	Prot	tecti	on d	lisab	oled																
			Enabled	1					F	Prot	tecti	on e	nab	led																
L	RW	REGION75							Е	Enal	ble p	orote	ectio	on f	or re	egic	n 7	5. W	/rite	'0'	has	no	effe	ct.						
			Disabled	0							tecti																			



Bit r	numbe	er		31 30	29 2	28 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d	c b	а	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0	0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value					Description
			Enabled	1					Protection enabled
M	RW	REGION76							Enable protection for region 76. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
N	RW	REGION77							Enable protection for region 77. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
0	RW	REGION78							Enable protection for region 78. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Р	RW	REGION79							Enable protection for region 79. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Q	RW	REGION80							Enable protection for region 80. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
R	RW	REGION81							Enable protection for region 81. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
S	RW	REGION82							Enable protection for region 82. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
T	RW	REGION83							Enable protection for region 83. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
U	RW	REGION84							Enable protection for region 84. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
V	RW	REGION85		_					Enable protection for region 85. Write '0' has no effect.
			Disabled	0					Protection disabled
		250,0105	Enabled	1					Protection enabled
W	RW	REGION86	5						Enable protection for region 86. Write '0' has no effect.
			Disabled	0					Protection disabled
.,		250101105	Enabled	1					Protection enabled
Х	RW	REGION87	5	_					Enable protection for region 87. Write '0' has no effect.
			Disabled	0					Protection disabled
		250,01100	Enabled	1					Protection enabled
Υ	кW	REGION88	Disabled	0					Enable protection for region 88. Write '0' has no effect.
			Disabled	0					Protection disabled
,	Dist	DECIONO	Enabled	1					Protection enabled
Z	RW	REGION89	D: 11 1	•					Enable protection for region 89. Write '0' has no effect.
			Disabled	0					Protection disabled
	D	DECIONOS	Enabled	1					Protection enabled
a	кW	REGION90	Disabled	0					Enable protection for region 90. Write '0' has no effect.
			Disabled	0					Protection disabled
L	Divi	DECIONOS	Enabled	1					Protection enabled
b	КW	REGION91	Disabled	0					Enable protection for region 91. Write '0' has no effect.
			Disabled	0					Protection disabled
		DECIONAL	Enabled	1					Protection enabled
С	КW	REGION92	D: 11 1	•					Enable protection for region 92. Write '0' has no effect.
			Disabled	0					Protection disabled
		250,01100	Enabled	1					Protection enabled
d	RW	REGION93	5						Enable protection for region 93. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled



Bit r	numbe	r		31	30 2	29	28 2	27	26 2	5 2	24 2	3 2	2 21	L 20	19	18	17	16	15 1	.4 1	3 1	2 11	10	9	8	7	6	5	4	3	2 :	1 0
Id				f	e	d	С	b	a Z	7_	Y >	(V	V V	U	Т	S	R	Q	Р (1 C	N N	1 L	K	J	1	Н	G	F	Ε	D	C I	ВА
Res	et 0x0	0000000		0	0	0	0	0	0 ()	0 0) (0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 (0 (
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion																		
е	RW	REGION94									Е	nab	le p	rote	ectio	on f	or r	egio	on 9	4. V	Vrite	e '0'	has	no	eff	ect.						
			Disabled	0							Р	rote	ectio	on d	isak	oled																
			Enabled	1							Р	rote	ectio	on e	nab	led																
f	RW	REGION95									Е	nab	le p	rote	ectio	on f	or r	egio	on 9	5. V	Vrite	e '0'	has	no	eff	ect.						
			Disabled	0							Р	rote	ectio	on d	isak	oled																
			Enabled	1							Р	rote	ectic	on e	nab	led																

12.1.5 CONFIG3

Address offset: 0x614

Block protect configuration register 3

	numbe	er			23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id					X W V U T S R Q P O N M L K J I H G F E D C B A
Res		0000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld		Field	Value Id	Value	Description
A	RW	REGION96			Enable protection for region 96. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
В	RW	REGION97			Enable protection for region 97. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
С	RW	REGION98			Enable protection for region 98. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
D	RW	REGION99			Enable protection for region 99. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
E	RW	REGION100			Enable protection for region 100. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
F	RW	REGION101			Enable protection for region 101. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
G	RW	REGION102			Enable protection for region 102. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
Н	RW	REGION103			Enable protection for region 103. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
ı	RW	REGION104			Enable protection for region 104. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
J	RW	REGION105			Enable protection for region 105. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
K	RW	REGION106			Enable protection for region 106. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
L	RW	REGION107			Enable protection for region 107. Write '0' has no effect.
			Disabled	0	Protection disabled
			Enabled	1	Protection enabled
М	R\M	REGION108	LIIGOICU	-	Enable protection for region 108. Write '0' has no effect.
	1.00		Disabled	0	Protection disabled
			Enabled	1	Protection disabled Protection enabled



Bit r	numbe	r		31 30	29 28	3 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a :	ΖY	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000		0 0	0 0	0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
N	RW	REGION109							Enable protection for region 109. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
0	RW	REGION110							Enable protection for region 110. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Р	RW	REGION111							Enable protection for region 111. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Q	RW	REGION112							Enable protection for region 112. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
R	RW	REGION113							Enable protection for region 113. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
S	RW	REGION114							Enable protection for region 114. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Т	RW	REGION115							Enable protection for region 115. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
U	RW	REGION116							Enable protection for region 116. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
V	RW	REGION117							Enable protection for region 117. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
W	RW	REGION118	5. 11.1						Enable protection for region 118. Write '0' has no effect.
			Disabled	0					Protection disabled
.,		550,000,00	Enabled	1					Protection enabled
Х	KW	REGION119	Dividity I	•					Enable protection for region 119. Write '0' has no effect.
			Disabled	0					Protection disabled
V	D\A/	DECIONATO	Enabled	1					Protection enabled
Υ	KVV	REGION120	Disabled	0					Enable protection for region 120. Write '0' has no effect.
			Disabled Enabled	1					Protection disabled Protection enabled
7	D\A/	RECION131	Enabled	1					
Z	IVV	REGION121	Disabled	0					Enable protection for region 121. Write '0' has no effect. Protection disabled
			Enabled	1					Protection disabled Protection enabled
2	D\A/	REGION122	Ellabled	1					
а	11.44	MEGIOIVIZZ	Disabled	0					Enable protection for region 122. Write '0' has no effect. Protection disabled
			Enabled	1					Protection disabled
b	R/M	REGION123	Litabica	_					Enable protection for region 123. Write '0' has no effect.
J	TVV	ILCIOIVI25	Disabled	0					Protection disabled
			Enabled	1					Protection disabled Protection enabled
С	R/V/	REGION124	Enabled	1					Enable protection for region 124. Write '0' has no effect.
C	11.00	NEGION124	Disabled	0					Protection disabled
			Enabled	1					Protection disabled
d	R\M	REGION125	2ubicu	•					Enable protection for region 125. Write '0' has no effect.
u	11.00	MEGIOIVIZJ	Disabled	0					Protection disabled
			Enabled	1					Protection disabled Protection enabled
e	R/V/	REGION126	Enabled	_					Enable protection for region 126. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection disabled
f	R/M	REGION127	2ubicu	•					Enable protection for region 127. Write '0' has no effect.
	11.00	MEGIOIVIZ/							Endoic protection for region 127. Write o has no effect.



Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	fedcbaZY	X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000	0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value	Description
Disabled	0	Protection disabled
Enabled	1	Protection enabled



13 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

13.1 Registers

Table 12: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x10000000	FICR	FICR	Factory Information Configuration		

Table 13: Register Overview

Register	Offset	Description	
CODEPAGESIZE	0x010	Code memory page size	
CODESIZE	0x014	Code memory size	
DEVICEID[0]	0x060	Device identifier	
DEVICEID[1]	0x064	Device identifier	
ER[0]	0x080	Encryption Root, word 0	
ER[1]	0x084	Encryption Root, word 1	
ER[2]	0x088	Encryption Root, word 2	
ER[3]	0x08C	Encryption Root, word 3	
IR[0]	0x090	Identity Root, word 0	
IR[1]	0x094	Identity Root, word 1	
IR[2]	0x098	Identity Root, word 2	
IR[3]	0x09C	Identity Root, word 3	
DEVICEADDRTYPE	0x0A0	Device address type	
DEVICEADDR[0]	0x0A4	Device address 0	
DEVICEADDR[1]	0x0A8	Device address 1	
INFO.PART	0x100	Part code	
INFO.VARIANT	0x104	Part Variant, Hardware version and Production configuration	
INFO.PACKAGE	0x108	Package option	
INFO.RAM	0x10C	RAM variant	
INFO.FLASH	0x110	Flash variant	
	0x114		Reserved
	0x118		Reserved
	0x11C		Reserved
TEMP.A0	0x404	Slope definition A0.	
TEMP.A1	0x408	Slope definition A1.	
TEMP.A2	0x40C	Slope definition A2.	
TEMP.A3	0x410	Slope definition A3.	
TEMP.A4	0x414	Slope definition A4.	
TEMP.A5	0x418	Slope definition A5.	
TEMP.B0	0x41C	y-intercept BO.	
TEMP.B1	0x420	y-intercept B1.	
TEMP.B2	0x424	y-intercept B2.	
TEMP.B3	0x428	y-intercept B3.	
TEMP.B4	0x42C	y-intercept B4.	
TEMP.B5	0x430	y-intercept B5.	
TEMP.TO	0x434	Segment end TO.	
TEMP.T1	0x438	Segment end T1.	
TEMP.T2			
TEIVII . TE	0x43C	Segment end T2.	
TEMP.T3	0x43C 0x440	Segment end 12. Segment end T3.	



Register	Offset	Description
NFC.TAGHEADER0	0x450	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER1	0x454	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER2	0x458	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER3	0x45C	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.

13.1.1 CODEPAGESIZE

Address offset: 0x010 Code memory page size

Bit	numb	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
^	n	CODEDACECIZE		Code manuscriptor

A R CODEPAGESIZE Code memory page size

13.1.2 CODESIZE

Address offset: 0x014 Code memory size

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A R CODESIZE		Code memory size in number of pages

Total code space is: CODEPAGESIZE * CODESIZE

13.1.3 DEVICEID[0]

Address offset: 0x060

Device identifier

В	t numl	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	.7 1	.6 1	5 1	4 13	3 12	11	10 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ ,	Δ /	Δ Α	4 A	A	Α	A A	A	Α	Α	Α	Α	Α	Α .	А А
R	eset Ox	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	1 1	1 1	1	1	1 1	. 1	1	1	1	1	1	1	1 1
Id	RW	/ Field	Value Id	Va	lue							De	scri	otic	n																	
Α	R	DEVICEID										64	bit ι	unio	que	de	vice	ide	ntif	ier												
															•						•	nifica										
												ide	ntifi	ier.	DE'	VIC	EID[1] c	ont	ain	s the	e mo	st s	gnif	can	bit	s of	fthe	e			
												de	vice	ide	ntif	fier.																

13.1.4 DEVICEID[1]

Address offset: 0x064

Device identifier

Bit number	31 30 29 28	3 27 26 25 24 23 22 21 20 19 18 3	17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id	АААА	A A A A A A A A A	A A A A A A A A	A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description		

A R DEVICEID 64 bit unique device identifier



Bit number	31 30	29 28 27	7 26 25 2	4 23 22	21 20 19	9 18 17 :	16 15 1	l4 13 1	.2 11 1	0 9	8 7	6	5 4	3	2 1	0
Id	A A	A A A	AAA	A A A	A A A	. A A	АА	A A	4 A A	A A	A A	Α	A A	A A	А А	Α
Reset 0xFFFFFFF	1 1	1 1 1	11:	l 1 1	1 1 1	1 1	1 1	1 1	1 1 :	1 1	1 1	1	1 1	. 1	1 1	1
Id RW Field Va	alue Id Value	2		Descri	otion											

DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.

13.1.5 ER[0]

Address offset: 0x080 Encryption Root, word 0

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A R ER		Encryption Root, word n

13.1.6 ER[1]

Address offset: 0x084 Encryption Root, word 1

Bit r	numbe	er		31	1 30	29	9 28	8 2	7 2	5 2	5 2	4 2	3 2	2 2	1 2	0 1	9 1	8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	. 4	\ <i>A</i>	Δ Δ	. 4	\ <i>A</i>	λ /	\ <i>A</i>	4 <i>A</i>	۱ ۸	Δ Α	A /	A /	\ A	A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 <i>A</i>	A A
Res	et OxF	FFFFFF		1	1	1	. 1	L 1	L 1	. 1	. 1	L 1	1 1	1 1	L 1	1 :	L 1	L 1	۱ 1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	l 1
Id	RW	Field	Value Id	Va	alue	•						D	esc	rip	tio	1																		
Α	R	ER										Ε	ncr	ypti	ion	Ro	ot, v	wor	d n															

13.1.7 ER[2]

Address offset: 0x088 Encryption Root, word 2

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19	18 17 16 15 14 13 12 11	1 10 9 8 7 6 5 4 3 2 1 0
Id		$A \; A \; A \; A \; A \; A \; A$	A A A A A A A	A A A A A A A	. A A A A A A A A A A
Reset 0xFFFF	FFF	1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1
Id RW Fie	d Value Id	Value	Description		
A R ER			Encryption Root	, word n	

13.1.8 ER[3]

Address offset: 0x08C Encryption Root, word 3

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 1	7 1	6 15	5 1	4 13	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A A	Δ ,	Δ Δ	A A	. Α	. 4	. Δ	. 4		Α	. Α	. Α	A	Α	Α	Α	Α	Α	Α.	4
Res	et Oxl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	L 1	. 1	. 1	. 1	1	. 1	. 1	. 1	1	. 1	1	1	1	1	1	1	Ĺ
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																			ı
Α	R	ER										Enc	rypt	tior	Ro	ot,	wor	d n																7

13.1.9 IR[0]

Address offset: 0x090 Identity Root, word 0



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	$1 \;\; 1 \;\; 1 \;\; 1 \;\; 1 \;\; 1 \;\; 1 \;\; 1 \;$
Id RW Field Value Id	Value Description
A R IR	Identity Root, word n

13.1.10 IR[1]

Address offset: 0x094 Identity Root, word 1

Bit	nur	nbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	А А
Re	set (0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1
Id	R	w	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	R		IR										Ide	ntii	tv R	oot	, w	ord	n																

13.1.11 IR[2]

Address offset: 0x098 Identity Root, word 2

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9	9 8 7 6 5 4 3 2 1 0
Id		$A \ A \ A \ A \ A$	A A A A A A A A A	A A A A A A A	A A A A A A A A
Reset 0xFFF	FFFF	1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1
Id RW Fi	eld Value Id	Value	Description		
A R IF			Identity Root, word n		

13.1.12 IR[3]

Address offset: 0x09C Identity Root, word 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A R IR		Identity Root, word n

13.1.13 DEVICEADDRTYPE

Address offset: 0x0A0

Device address type

Bit	numbe	er		31 3	0 29	28	3 27	26	25	24	23 2	22 2	21 2	0 1	9 1	8 17	' 16	15	14 :	13 1	2 11	10	9	8	7	6	5 -	4 3	2	1	0
Id																															Α
Res	et 0xF	FFFFFF		1 1	. 1	1	1	1	1	1	1	1	1 :	1 1	1	. 1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Valu	е						Des	crip	tio	n																	
Α	R	DEVICEADDRTYPE									Dev	ice	add	res	s ty	oe															
			Public	0							Pub	lic a	ddı	ess																	
			Random	1							Ran	don	n ac	ddre	SS																

13.1.14 **DEVICEADDR**[0]

Address offset: 0x0A4 Device address 0

address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used.



Bitı	iumbe	er		31	L 30	29	28	3 27	7 26	25	24	23	22 2	1 2	0 19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3	2 :	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	Δ ,	4 А	Α	Α	Α	Α	Α	A A	Δ Δ	ι A	Α	Α	Α	Α	Α	Α	Α .	A A	АА
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1	1 1	l 1
Id	RW	Field	Value Id	Va	alue							Des	crip	tio	n																	
Id A	RW R	Field DEVICEADDR	Value Id	Va	alue										n ce ad	ldre	ess															

13.1.15 DEVICEADDR[1]

Address offset: 0x0A8

Device address 1

Bit nu	mbe	r		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	.8 1	7 1	.6 1	.5 1	L4 1	3 12	2 11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A	A A	Δ ,	Δ Α	Δ ,	Δ,	A A	A	Α	Α	Α	Α	Α	Α	Α ,	A A	A A	Α	Α
Reset	0xFl	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 :	1 :	1 :	1 1	. 1	1	1	1	1	1	1	1	1 :	l 1	1	1
ld F	RW	Field	Value Id	Va	lue							Des	scrip	tio	n																		
A F	R	DEVICEADDR										48	bit d	levi	ice a	addı	ress	5															
												ado	dress	s. D	EVI	CEA	DD	R[1	.] cc	onta	east ains 15:0	the	mo	st si	gnit	ficaı	nt b	its	of				

13.1.16 INFO.PART

Address offset: 0x100

Part code

Bit r	numbe	er		31	1 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14 1	13 1	2 13	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	A A	A	Α	Α	Α	Α	Α	A A	A	Α.	Α	Α	Α	Α	Α	Α	Α .	Δ ,	A A
Res	et 0x0	0052832		0	0	0	0	0	0	0	0	0	0	0 0	0	1	0	1	0	0	1 () 1	0	0	0	0	0	1	1	0	0 :	L O
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 Value								Des	crip	tior	1																	
Α	R	PART										Par	t co	de																		
			N52832	0х	(528	332						nRF	528	32																		
			Unspecified	0х	(FFF	FFF	FF					Uns	pec	ified	ł																	

13.1.17 INFO.VARIANT

Address offset: 0x104

Part Variant, Hardware version and Production configuration

Bit	numb	er		31	. 30	29	28	27	26	25 2	24 2	23 2	2 2	1 20	19	9 18	17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	A	A A	A /	А А	Α	A	Α	Α	Α	Α	Α	Α	A ,	Δ Α	. Α	. A	Α	Α	Α	Α	Α	А А
Res	et 0x4	11414142		0	1	0	0	0	0	0	1	0 1	۱ (0 0	0	0	0	1	0	1	0	0	0	0) 1	0	1	0	0	0	0	1 0
Id	RW	Field	Value Id	Va	lue							Desc	rip	tion																		
Α	R	VARIANT									F	art	Var	riant	, На	ardv	var	e ve	ersio	on a	nd	Prod	duct	ion	cor	figu	ırat	ion	,			
											e	enco	de	d as	ASC	CII																
			AAAA	0x	414	141	141				A	AAA	Д																			
			AAAB	0x	414	141	142				A	AAA	В																			
			AABA	0x	414	142	241				A	AAB	4																			
			AABB	0x	414	142	242				A	AABI	В																			
			Unspecified	0x	FFF	FFF	FF				ι	Jnsp	eci	ified																		

13.1.18 INFO.PACKAGE

Address offset: 0x108

Package option



Bit	numbe	r		31	L 30	29	28	3 27	7 26	25	24	23	22 2	21 2	20 :	19 1	18 1	.7 1	.6 1	15 :	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Δ,	Δ.	Α	Α	A A	Α Α	A	Α	Α	Α	Α	Α	Α	Α	A A	A A
Res	et 0x0	0002000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 (0	0	0	0	0	0	0	0	0	0 (0
Id	RW	Field	Value Id	Va	alue	•						De	scrip	otio	n																		
Α	R	PACKAGE										Pa	ckag	e o	ptic	n																	
			QF	0x	200	00						QF	xx -	48-	pin	QFI	N																
			CH	0x	200)1						СН	xx -	7x8	WI	LCSI	P 56	ba	lls														
			Unspecified	0x	FFF	FFF	FF					Un	spec	ifie	ed																		

13.1.19 INFO.RAM

Address offset: 0x10C

RAM variant

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α Α	A	Α
Res	et 0x0	0000040		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0 0	0	0
Id	RW	Field	Value Id	lue							De	scri	ptic	n																				
Α	R	RAM										RA	Μv	aria	nt																			
			K16	0x	10							16	kBy	te F	RAN	Л																		
			K32	0x	20							32	kBy	te F	RAN	Л																		
			K64	0x	40							64	kBy	te F	RAN	Л																		
			Unspecified	0x	FFF	FFF	FF					Un	spe	cifie	ed																			

13.1.20 INFO.FLASH

Address offset: 0x110

Flash variant

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	18 1	.7 1	16 1	15 1	.4 1	.3 1	2 1:	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Δ.	Α.	Α.	A A	Δ ,	A A	Α	Α	Α	Α	Α	Α	Α	Α	A A	А А
Res	et 0x0	0000200		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	1	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	llue							De	scrip	ptio	n																		
Α	R	FLASH										Fla	sh v	aria	nt																		
			K128	0x	80							128	3 kB	yte	FLA	ASH																	
			K256	0x	100							256	6 kB	yte	FLA	ASH																	
			K512	0x	200							512	2 kB	yte	FLA	ASH																	
			Unspecified	0x	FFFF	FFF	FF					Un	spe	cifie	d																		

13.1.21 TEMP.A0

Address offset: 0x404 Slope definition A0.

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23 :	22 :	21	20	19	18	17	16	15	14	13 :	L2 1	1 1	0 9	9 8	3 7	7 6	5 5	4	3	2	1	0
Id																							,	Α Α	A A	Α Α	Δ ,	A A	A	Α	Α	Α	Α	Α
Res	et OxO	0000320		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () 1	L 1	1 () () 1	0	0	0	0	o
Id	RW	Field	Value Id	Va	alue							Des	crip	otic	n																			
Α	R	Α										A (s	lop	e d	efir	nitic	on)	reg	iste	r.														7

13.1.22 TEMP.A1

Address offset: 0x408 Slope definition A1.



Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18	17	16	15 :	14 :	13 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																							A	A	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	00000343		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	1	1	0	1	0	0	0	0	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																		
Α	R	A										A (:	slop	e d	efir	itio	n) ı	regi	iste	r.													

13.1.23 TEMP.A2

Address offset: 0x40C Slope definition A2.

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	18 :	17 1	L6 1	15 2	14 1	13 1	2 13	10	9	8	7	6	5	4	3	2	1 0
Id																							Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	000035D		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	1	1	0	1	0	1	1	1	0 1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	Α										A (s	lope	e d	efin	itio	n) r	egi	stei	٠.													

13.1.24 TEMP.A3

Address offset: 0x410 Slope definition A3.

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0
Id					A A A A A	A A A A A A
Reset 0x00000400		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 1 0 0 0	0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			
A R A			A (slope definition) re	egister.		

13.1.25 TEMP.A4

Address offset: 0x414 Slope definition A4.

Bitı	numb	er		31	30 2	29 2	28 2	7 26	25	24	23	22 2	21 2	0 1	9 1	8 17	⁷ 16	15	14	13 :	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																					A	A	Α	Α	Α	Α	Α.	A	А А	Α	Α
Res	et Ox(00000452		0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (1	0	0	0	1	0	1	0 0	1	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tio	n																	
Α	R	Α		Value Id Value							A (s	qol	e de	efini	tior	ı) re	gist	er.													

13.1.26 TEMP.A5

Address offset: 0x418 Slope definition A5.

Bit	numbe	er		31	30	29 :	28	27 2	26 2	25 2	24	23	22 2	1 2	0 1	9 1	8 1	7 1	5 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id																							Α	Α	Α	Α	Α	Α	Α	Α	ΑА	A A	А А
Res	et 0x0	000037В		0	0	0	0	0	0	0	0	0	0)	0 () (0	0	0	0	0	0	0	0	1	1	0	1	1	1	1 0) 1	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	Α										A (s	lope	de	fini	tio	n) re	gis	ter.														

13.1.27 TEMP.B0

Address offset: 0x41C y-intercept B0.



Bit	numb	er		31 3	30 29	28	3 27	26	25 2	24 2	23 2	2 21	20	19	18	17	16 3	L5 1	4 1	3 12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id																			Δ	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	Α	Α
Res	et 0x	00003FCC		0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0 () 1	1	1	1	1	1	1	1	0	0 :	l 1	0	0
Id	RW	Field	Value Id	Valu	ıe						Desc	ript	ion																		
Α	R	В	Value Id Value								3 (y-	inte	rcer	ot)																	

13.1.28 TEMP.B1

Address offset: 0x420

y-intercept B1.

Bi	t nun	nbe	r		31	30 2	29 2	28 2	7 26	25	24	23	22 2	21 2	20 1	9 1	.8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id																					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	А А
Re	eset (0x0	0003F98		0	0	0	0 0	0	0	0	0	0	0	0	0 (0 (0	0	0	1	1	1	1	1	1	1	0	0	1	1 (0	0 0
Id	R	w	Field	Value Id	Va	lue						Des	crip	otio	n																		
Α	R		В									В (у	-int	erc	ept)																	

13.1.29 TEMP.B2

Address offset: 0x424

y-intercept B2.

Bit	nu	mbe	er		31 30 29 28 27	7 26	25 2	24 2	3 22	21 :	20 1	.9 18	3 17	16	15 :	L4 13	12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id																Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	4 A	AA
Re	set	0x0	0003F98		0 0 0 0 0	0	0	0	0 0	0	0 (0 0	0	0	0	0 1	1	1	1	1	1	1	0	0	1	1	0 0	0
Id	ı	RW	Field	Value Id	Value				escr	iptio	n																	
Α	F	R	В					Е	(v-i	nterc	ent)																

13.1.30 TEMP.B3

Address offset: 0x428

y-intercept B3.

A R B			B (y-intercept)			
Id RW Field	Value Id	Value	Description			
Reset 0x00000012		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0	0010010
Id				A A	A A A A	
Bit number		31 30 29 28 27 3	26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12	11 10 9 8 7	6 5 4 3 2 1 0
Pit number		21 20 20 20 27 :	26 25 24 22 22 21 20 10 10 1	17 16 16 14 10 10	11 10 0 0 7	6 6 4 2 2

13.1.31 TEMP.B4

Address offset: 0x42C

y-intercept B4.

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	17 16 15 14 1	.3 12 11 10	9 8	7 6 !	5 4 3 2	2 1 0
Id				,	A A A A	A A .	4 A A	4 A A A	A A A
Reset 0x0000004D		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0	0 0	0 1 (0 0 1 1	l 0 1
Id RW Field	Value Id	Value	Description						
A R B			B (y-intercept)						

13.1.32 TEMP.B5

Address offset: 0x430

y-intercept B5.



Bit	numb	er		31	30 2	9 :	28	27 2	26 2	25 2	24 2	23 2	22 2	21 2	20 1	9 1	.8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 A	A
Res	et 0x0	00003E10		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	1	1	1	1	1	0	0	0	0	1	0 (0 0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	В									E	3 (y	-int	erc	ept)																	

13.1.33 TEMP.T0

Address offset: 0x434 Segment end T0.

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x000000E2		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 1 1 0 0 0 1 0
Id RW Field	Value Id	Value	Description		
A D T			T /	_	

A R T T (segment end)register.

13.1.34 TEMP.T1

Address offset: 0x438 Segment end T1.

Bitı	numbe	er		31 30 29 28 27	26 25 24	23 22 21	20 19	18 17	16 1	L5 14	13 12	2 11 1	9	8	7	6	5	4	3 2	2 1	0
Id															Α	Α	Α	Α	A A	A A	Α
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	0 0 0	0 0	0 0	0	0 0	0 0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value		Description	on														
Α	R	Т				T (segme	nt end)	regist	er.												_

13.1.35 TEMP.T2

Address offset: 0x43C Segment end T2.

Bit number		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000014		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A R T			T (segment end)register.

13.1.36 TEMP.T3

Address offset: 0x440 Segment end T3.

Bit	numbe	r		31 30 29 28 27	26 25 24 23 22 21 20 19 1	8 17 16 15 14	13 12 11 1	9 8	7	6 5	4	3 2	1	O .
Id									Α	A A	Α.	A A	Α.	A
Res	et 0x0	0000019		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0 0	1	1 0	0	1
Id	RW	Field	Value Id	Value	Description									
Α	R	Т			T (segment end)re	egister.								

13.1.37 TEMP.T4

Address offset: 0x444 Segment end T4.



Bit numl	per		31 3	0 29	28	27 26	5 25	24	23	22 2	21 2	0 19	9 18	3 17	16	15 1	14 13	3 12	11	10 9	9 8	3 7	6	5	4	3 2	2 1	. 0
Id																						Α	Α	Α	Α	A A	A	A
Reset 0x	d0000050		0 (0	0	0 0	0	0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0 () (0	1	0	1	0 0	0	0
Id RV	/ Field	Value Id	Valu	e					Des	crip	tio	n																
A R	T								T (s	egn	nent	end	d)re	giste	er.													

13.1.38 NFC.TAGHEADER0

Address offset: 0x450

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit r	numbe	er		31	. 30	29	28	27	7 26	5 25	5 24	23	22 2	21 2	20 1	19 :	18 1	7 :	16 1	15 :	14 :	13	12 1	11 :	10	9	8	7	6	5	4	3	2	1 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	C (С	С	В	В	В	В	В	В	В	В	Α	Α	Α	Α	Α	Α.	А А
Res	et OxF	FFFF5F		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue	:						Des	crip	tio	n																			
Α	R	MFGID										Def	ault	M	anu	fac	ture	er II	D: N	lor	dic	Ser	nico	nd	uct	or A	٩SA	ha	s IC	M				
												0x5	F																					
В	R	UD1										Uni	que	ide	enti	fier	byt	e 1																
С	R	UD2										Uni	que	ide	enti	fier	byt	e 2	!															
D	R	UD3										Uni	que	ide	enti	fier	bvt	e 3	}															

13.1.39 NFC.TAGHEADER1

Address offset: 0x454

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit	numbe	er		31	. 30	29	28	3 27	26	5 25	24	23	22 :	21 :	20 1	L9 1	8 1	7 1	6 15	5 14	13	12	11 :	LO !	9	8	7	6 !	5 4	1 3	2	1	0
Id				D	D	D	D	D	D	D	D	С	С	С	С	C (C (0	В	В	В	В	В	В	В	В	١	Α /	4 4	A A	Α	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	. 1	. 1	1	1	1	1	1	1 :	L	1 :	1 1	l 1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																		
Α	R	UD4										Uni	ique	ide	enti	fier	byt	e 4															
В	R	UD5										Uni	ique	ide	enti	fier	byt	e 5															
С	R	UD6										Uni	ique	ide	enti	fier	byt	e 6															
D	R	UD7										Uni	ique	ide	enti	fier	byt	e 7															

13.1.40 NFC.TAGHEADER2

Address offset: 0x458

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	.8 1	7 1	5 1	5 14	1 13	12	11	10	9	8	7	5 5	4	3	2	1 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	C (C (0	: E	В	В	В	В	В	В	В	۱ ۱	4 <i>A</i>	A	Α	Α	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	. 1	. 1	1	1	1	1	1	1 :	L	1 1	. 1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	R	UD8										Uni	que	ide	enti	fier	byt	e 8														
В	R	UD9										Uni	que	ide	enti	fier	byt	e 9														
С	R	UD10										Uni	que	ide	enti	fier	byt	e 10)													
D	R	UD11										Uni	que	ide	enti	fier	byt	e 1:	L													

13.1.41 NFC.TAGHEADER3

Address offset: 0x45C

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.



Bitı	numbe	er		31	1 30	29	28	8 27	7 26	25	24	23	22 2	1 2	0 19	18	17	16	15	14	13	12 1	.1 1	0 9	8	7	6	5	4	3 2	2 1	L 0
Id				D	D	D	D	D	D	D	D	С	C (0	: c	С	С	С	В	В	В	В	ВЕ	3 E	3 B	Α	Α	Α	Α	A A	4 Α	A A
Res	et OxF	FFFFFF		1	1	1	1	. 1	1	1	1	1	1 1	L 1	. 1	1	1	1	1	1	1	1	1 1	L 1	l 1	1	1	1	1	1 1	l 1	1
Id	RW	Field	Value Id	Va	alue	:						Des	crip	tior	1																	
Α	R	UD12										Uni	que	ide	ntifi	er b	yte	12														
В	R	UD13										Uni	que	ide	ntifi	er b	yte	13														
С	R	UD14										Uni	que	ide	ntifi	er b	yte	14														
D	R	UD15										Uni	que	ide	ntifi	er b	yte	15														



14 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user specific settings.

For information on writing UICR registers, see the *NVMC — Non-volatile memory controller* on page 26 and *Memory* on page 20 chapters.

14.1 Registers

Table 14: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x10001000	UICR	UICR	User Information Configuration		

Table 15: Register Overview

Register	Offset	Description	
	0x000		Reserved
	0x004		Reserved
	0x008		Reserved
	0x010		Reserved
NRFFW[0]	0x014	Reserved for Nordic firmware design	
NRFFW[1]	0x018	Reserved for Nordic firmware design	
NRFFW[2]	0x01C	Reserved for Nordic firmware design	
NRFFW[3]	0x020	Reserved for Nordic firmware design	
NRFFW[4]	0x024	Reserved for Nordic firmware design	
NRFFW[5]	0x028	Reserved for Nordic firmware design	
NRFFW[6]	0x02C	Reserved for Nordic firmware design	
NRFFW[7]	0x030	Reserved for Nordic firmware design	
NRFFW[8]	0x034	Reserved for Nordic firmware design	
NRFFW[9]	0x038	Reserved for Nordic firmware design	
NRFFW[10]	0x03C	Reserved for Nordic firmware design	
NRFFW[11]	0x040	Reserved for Nordic firmware design	
NRFFW[12]	0x044	Reserved for Nordic firmware design	
NRFFW[13]	0x048	Reserved for Nordic firmware design	
NRFFW[14]	0x04C	Reserved for Nordic firmware design	
NRFHW[0]	0x050	Reserved for Nordic hardware design	
NRFHW[1]	0x054	Reserved for Nordic hardware design	
NRFHW[2]	0x058	Reserved for Nordic hardware design	
NRFHW[3]	0x05C	Reserved for Nordic hardware design	
NRFHW[4]	0x060	Reserved for Nordic hardware design	
NRFHW[5]	0x064	Reserved for Nordic hardware design	
NRFHW[6]	0x068	Reserved for Nordic hardware design	
NRFHW[7]	0x06C	Reserved for Nordic hardware design	
NRFHW[8]	0x070	Reserved for Nordic hardware design	
NRFHW[9]	0x074	Reserved for Nordic hardware design	
NRFHW[10]	0x078	Reserved for Nordic hardware design	
NRFHW[11]	0x07C	Reserved for Nordic hardware design	
CUSTOMER[0]	0x080	Reserved for customer	
CUSTOMER[1]	0x084	Reserved for customer	
CUSTOMER[2]	0x088	Reserved for customer	
CUSTOMER[3]	0x08C	Reserved for customer	
CUSTOMER[4]	0x090	Reserved for customer	
CUSTOMER[5]	0x094	Reserved for customer	
CUSTOMER[6]	0x098	Reserved for customer	



Register	Offset	Description
CUSTOMER[7]	0x09C	Reserved for customer
CUSTOMER[8]	0x0A0	Reserved for customer
CUSTOMER[9]	0x0A4	Reserved for customer
CUSTOMER[10]	0x0A8	Reserved for customer
CUSTOMER[11]	0x0AC	Reserved for customer
CUSTOMER[12]	0x0B0	Reserved for customer
CUSTOMER[13]	0x0B4	Reserved for customer
CUSTOMER[14]	0x0B8	Reserved for customer
CUSTOMER[15]	0x0BC	Reserved for customer
CUSTOMER[16]	0x0C0	Reserved for customer
CUSTOMER[17]	0x0C4	Reserved for customer
CUSTOMER[18]	0x0C8	Reserved for customer
CUSTOMER[19]	0x0CC	Reserved for customer
CUSTOMER[20]	0x0D0	Reserved for customer
CUSTOMER[21]	0x0D4	Reserved for customer
CUSTOMER[22]	0x0D8	Reserved for customer
CUSTOMER[23]	0x0DC	Reserved for customer
CUSTOMER[24]	0x0E0	Reserved for customer
CUSTOMER[25]	0x0E4	Reserved for customer
CUSTOMER[26]	0x0E8	Reserved for customer
CUSTOMER[27]	0x0EC	Reserved for customer
CUSTOMER[28]	0x0F0	Reserved for customer
CUSTOMER[29]	0x0F4	Reserved for customer
CUSTOMER[30]	0x0F8	Reserved for customer
CUSTOMER[31]	0x0FC	Reserved for customer
PSELRESET[0]	0x200	Mapping of the nRESET function (see POWER chapter for details)
PSELRESET[1]	0x204	Mapping of the nRESET function (see POWER chapter for details)
APPROTECT	0x208	Access Port protection
NFCPINS	0x20C	Setting of pins dedicated to NFC functionality: NFC antenna or GPIO

14.1.1 NRFFW[0]

Address offset: 0x014

Reserved for Nordic firmware design

Bit n	umbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12 :	11 :	10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	4 А
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	NRFFW										Res	erv	/ed	for	No	rdic	fir	nw	are	de	sigr												

14.1.2 NRFFW[1]

Address offset: 0x018

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	$1 \;\; 1 \;\; 1 \;\; 1 \;\; 1 \;\; 1 \;\; 1 \;\; 1 \;$
Id RW Field Value Id	Value Description
A RW NRFFW	Reserved for Nordic firmware design

14.1.3 NRFFW[2]

Address offset: 0x01C

Reserved for Nordic firmware design



14.1.4 NRFFW[3]

Address offset: 0x020

Reserved for Nordic firmware design

14.1.5 NRFFW[4]

Address offset: 0x024

Reserved for Nordic firmware design

14.1.6 NRFFW[5]

Address offset: 0x028

Reserved for Nordic firmware design

14.1.7 NRFFW[6]

Address offset: 0x02C

Reserved for Nordic firmware design

14.1.8 NRFFW[7]

. . . NEEDWEN

Address offset: 0x030

Reserved for Nordic firmware design

RW NRFFW Reserved for Nordic firmware design



14.1.9 NRFFW[8]

Address offset: 0x034

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

14.1.10 NRFFW[9]

Address offset: 0x038

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

14.1.11 NRFFW[10]

Address offset: 0x03C

Reserved for Nordic firmware design

Bit	numbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Δ	. 4	A	Α	Α	Α	Α	Α	Α.	А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1	. 1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	scr	iptio	on																			
Α	RW	NRFFW										Re	ser	ved	for	No	rdic	fir	mw	are	de	sigr	1											

14.1.12 NRFFW[11]

Address offset: 0x040

Reserved for Nordic firmware design

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19	18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id		AAAAA	. A A A A A A A	A A A A A A A A	A A A A A A A A A
Reset 0xFFFFF	FF	1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
Id RW Fiel	Value Id	Value	Description		
A RW NRI	-W		Reserved for No	rdic firmware design	

14.1.13 NRFFW[12]

Address offset: 0x044

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 3	. 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	on

A RW NRFFW Reserved for Nordic firmware design

14.1.14 NRFFW[13]

Address offset: 0x048

Reserved for Nordic firmware design



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

14.1.15 NRFFW[14]

Address offset: 0x04C

Reserved for Nordic firmware design

Bit	numbe	er		31	1 30	29	28	27	7 26	25	24	23	22	21	20	19	18 1	17 :	16 1	L5 1	.4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Δ,	Δ .	A /	A	Α	Α	Α	Α	Α	Α	Α	A ,	4 А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	n																		
Α	RW	NRFFW										Res	serv	/ed	for	Nor	dic	firr	nwa	are	des	ign											

14.1.16 NRFHW[0]

Address offset: 0x050

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

14.1.17 NRFHW[1]

Address offset: 0x054

Reserved for Nordic hardware design

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	16 1	L5 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A A	A /	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	. A	Α
Rese	t 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	. 1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	NRFHW										Res	erv	ed '	for	Nor	dic	har	dw	are	des	ign											

14.1.18 NRFHW[2]

Address offset: 0x058

Reserved for Nordic hardware design

Bit r	numbe	er		31	30 :	29	28 :	27	26	25	24	23	22 2	21 2	20 1	.9 1	.8 1	.7 1	.6 1	L5 1	.4 1	.3 1	.2 1	.1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	Δ ,	Δ ,	Δ ,	Δ.	Α ,	Δ ,	Δ.	Δ,	Δ ,	Δ Δ	Α	Α	Α	Α	Α	A	Δ,	А А
Res	et OxF	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 :	1	1 :	1 :	1	1	1 :	l 1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Val	lue							Des	crip	otio	n																		
Α	RW	NRFHW										Res	erv	ed f	or I	Vor	dic	har	dw	are	des	sigr	1										

14.1.19 NRFHW[3]

Address offset: 0x05C

Reserved for Nordic hardware design

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16 1	L5 1	l4 1	3 1	2 1:	10	9	8	7	6	5	4	3 2	2 1	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A A	Δ 4	A A	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	l 1	1	1	1	1	1	1	1	1 :	L 1	l 1
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																		

RW NRFHW Reserved for Nordic hardware design



14.1.20 NRFHW[4]

Address offset: 0x060

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

Reserved for Nordic hardware design

14.1.21 NRFHW[5]

Address offset: 0x064

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
December OverFFFFFF		
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

14.1.22 NRFHW[6]

Address offset: 0x068

Reserved for Nordic hardware design

Bit numb	er		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 :	19 1	18 1	17 1	16 1	15 1	.4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 :	1 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A A	A .	A	Α ,	Δ .	۱ ۸	Α Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	A A
Reset 0xF	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1 :	1 :	1 :	L 1	l 1	1	1	1	1	1	1	1 :	1 1	l 1
ld RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
A RW	NRFHW										Res	erv	ed f	for I	Nor	dic	har	dw	are	des	ign											

14.1.23 NRFHW[7]

Address offset: 0x06C

Reserved for Nordic hardware design

Bit number		31	1 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 :	10	9	8 7	7 6	5 5	4	3	2	1 (C
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A A	Α Α	Α	Α	Α	Α ,	4
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 1	l 1	1	1	1	1	l
ld RW Field	Value Id	Va	alue	:						De	scri	ptic	on																			
A RW NRFHW										Res	serv	ed	for	No	rdic	: ha	rdv	vare	e de	sig	n											

14.1.24 NRFHW[8]

Address offset: 0x070

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW NRFHW Reserved for Nordic hardware design

14.1.25 NRFHW[9]

Address offset: 0x074

Reserved for Nordic hardware design



Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 3	14 :	.3 1	2 1	1 10	9	8	7	6	5	4	3	2 1	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ ,	A /	A A	Α	Α	Α	Α	Α	Α	Α /	A /	A A
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	l 1	1	1	1	1	1	1	1 :	L 1	l 1
Id RW Field	Value Id	Va	lue							De	scri	ptic	on																		
A RW NRFHW										Re	serv	/ed	for	Noi	dic	ha	rdw	/are	de	sign											

14.1.26 NRFHW[10]

Address offset: 0x078

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

14.1.27 NRFHW[11]

Address offset: 0x07C

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

14.1.28 CUSTOMER[0]

Address offset: 0x080 Reserved for customer

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.29 CUSTOMER[1]

Address offset: 0x084 Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

14.1.30 CUSTOMER[2]

Address offset: 0x088 Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW CUSTOMER Reserved for customer



14.1.31 CUSTOMER[3]

Address offset: 0x08C Reserved for customer

Bit	numbe	er		31	. 30	29	28	3 2	7 26	5 25	5 24	1 23	3 22	2 21	. 20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	. Α	. A	. Д	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	. Α	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue	9						De	escr	ripti	ion																			
	D14/	CUCTONACD										_																						

A RW CUSTOMER Reserved for customer

14.1.32 CUSTOMER[4]

Address offset: 0x090 Reserved for customer

Bi	t nu	mbe	r		31	. 30	2 (9 2	8 2	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Δ		۸ ۸	А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A	Ą
Re	eset	0xFl	FFFFFF		1	1	. 1	ι :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L
Id	ı	RW	Field	Value Id	Va	alu	е							De	scri	ptic	on																				
Δ	F	R/V/	CUSTOMER											Re	erv	/ed	for	CHIS	tor	ner																	Ξ.

A RW CUSTOMER Reserved for custome

14.1.33 CUSTOMER[5]

Address offset: 0x094 Reserved for customer

Bit	numbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14 :	13 :	L2 1	11 1	0 9) 8	3 7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	A A		. Δ	. Δ	A	Α	Α	Α	АА
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1	1	. 1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	CUSTOMER										Res	serv	ed	for	cus	ton	ner															

14.1.34 CUSTOMER[6]

Address offset: 0x098
Reserved for customer

Bit	numb	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	0
Id				A A A A A A A A A A A A A A A A A A A	Α
Re	set OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1
Id	RW	Field	Value Id	Value Description	
Α	RW	CUSTOMER		Reserved for customer	_

14.1.35 CUSTOMER[7]

Address offset: 0x09C Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW CUSTOMER Reserved for customer

14.1.36 CUSTOMER[8]

Address offset: 0x0A0
Reserved for customer



Bit number		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10 9 8 7 6 5 4 3	2 1 0
Id		A A A A A A	A A A A A A A A A	A A A A A A A A A A A A	A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1
Id RW Field	Value Id	Value	Description		
A RW CUSTOME	R		Reserved for customer		

14.1.37 CUSTOMER[9]

Address offset: 0x0A4
Reserved for customer

Bit	numbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20	19 :	18 1	17 1	16 1	.5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ ,	Δ Α	. Α	A	Α	Α	Α	Α	Α	Α	Α	A A	4 Α	А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	. 1	. 1	1	1	1	1	1	1	1	1 1	l 1	. 1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	n																		
Α	RW	CUSTOMER										Res	erv	ed '	for	cus	tom	ner															

14.1.38 CUSTOMER[10]

Address offset: 0x0A8
Reserved for customer

Bit nu	mbe	r		33	1 30	29	9 28	27	7 26	25	24	23	22	21	20 :	19 1	18 1	17 1	.6 1	5 1	4 13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	. A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	A	Δ ,	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α Α	A A	. A
Reset	0xFI	FFFFFF		1	1	1	. 1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 1	. 1	1	1	1	1	1	1	1	1	1	1 1	l 1	1
ld I	RW	Field	Value Id	V	alue	•						De	scri	ptic	n																		
A I	RW	CUSTOMER										Res	serv	ed	for	cust	tom	ner															

14.1.39 CUSTOMER[11]

Address offset: 0x0AC Reserved for customer

Bitı	numbe	er		33	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	LO	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	A	۸ ۸	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	. :	1 1
Id	RW	Field	Value Id	V	alue							De	scr	pti	on																			
Α	RW	CUSTOMER										Re	ser	ved	for	cus	stor	ner																

14.1.40 CUSTOMER[12]

Address offset: 0x0B0 Reserved for customer

Bit n	umbe	r		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Rese	t 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.41 CUSTOMER[13]

Address offset: 0x0B4 Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description

A RW CUSTOMER Reserved for customer



14.1.42 CUSTOMER[14]

Address offset: 0x0B8 Reserved for customer

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	4 A
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 1	1 1
Id	RW	Field	Value Id	Va	llue	•						De	scri	pti	on																			
^	DIA	CLICTOMACD										n -			£																			

A RW CUSTOMER Reserved for customer

14.1.43 CUSTOMER[15]

Address offset: 0x0BC Reserved for customer

																																				ï
Bit	nu	ımbe	r		31	. 30	29	28	27	7 26	25	5 24	1 23	3 22	2 2:	1 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	ı
																																				L
Id					Α	Α	Α	Α	Α	. A	Α	. A	. Α	ιА	. A	. А	. А	Α	Α	Α	Α	Α	Α	А	Α	А	Α	Α	Α	А	Α	А	Α .	Α.	A A	L
Ro	cot	OVE	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L
	JCL	OAI			-	-	_	-	-	-	-	-	-	-	_	-	-	_	-	-	-	-	-	•	-	•	-	-	•	-	-	-	•	-		L
Id		RW	Field	Value Id	Va	ılue	•						D	esci	ript	ion																				
																																				4
		DIA	CLICTONALD										ъ.					4 _		_																

A RW CUSTOMER Reserved for customer

14.1.44 CUSTOMER[16]

Address offset: 0x0C0 Reserved for customer

Bit	numbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14 :	13 :	L2 1	11 1	0 9) 8	3 7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	A A		. Δ	. Δ	A	Α	Α	Α	АА
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1	1	. 1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	CUSTOMER										Res	serv	ed	for	cus	ton	ner															

14.1.45 CUSTOMER[17]

Address offset: 0x0C4
Reserved for customer

Bit number			31	30	29	28 :	27 :	26	25 2	24	23 2	22 2	1 2	0 19	9 18	8 17	16	15	14	13	12 1	1 1	0 9	8	7	6	5	4	3 2	. 1	L 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ ,	4 А	. A	A	Α	Α	Α	Α	A A	Δ	A	Α	Α	Α	Α	Α	A A	. Α	A A
Reset 0xFFI	FFFFF		1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	1	. 1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1 1	. 1	1
Id RW I	Field	Value Id	Va	lue							Des	crip	tio	n																	
A RW (CUSTOMER										Rese	≥rve	d f	or ci	ısto	nme	r														

14.1.46 CUSTOMER[18]

Address offset: 0x0C8
Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 3	. 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	on

A RW CUSTOMER Reserved for customer

14.1.47 CUSTOMER[19]

Address offset: 0x0CC Reserved for customer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

14.1.48 CUSTOMER[20]

Address offset: 0x0D0 Reserved for customer

Bit	numb	er		31	1 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16 :	15 1	L4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	Α Α	λ Α	A	Α	Α	Α	Α	Α	Α	A	Δ Α	A A
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	. 1	1	1	1	1	1	1	1 :	1 1	l 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	n																		
Α	RW	CUSTOMER										Res	erv	ed	for	cus	ton	ner															

14.1.49 CUSTOMER[21]

Address offset: 0x0D4
Reserved for customer

Bit	numbe	er		31	1 30	29	28	3 27	7 26	25	24	23	22	21	20 :	19 1	18 1	17 1	16 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Α,	A A	λ Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α .	4 Α	A	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	. 1	1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	n																		
Α	RW	CUSTOMER										Res	erv	ed '	for	cust	tom	er															

14.1.50 CUSTOMER[22]

Address offset: 0x0D8
Reserved for customer

Bitı	numbe	er		33	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	LO	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	A	۸ ۸	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	. :	1 1
Id	RW	Field	Value Id	V	alue							De	scr	pti	on																			
Α	RW	CUSTOMER										Re	ser	ved	for	cus	stor	ner																

14.1.51 CUSTOMER[23]

Address offset: 0x0DC Reserved for customer

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	LO	9	8	7	6	5 -	4	3 2	. 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α.	Α	Α	A	Α	А А		4 А
Res	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	CUSTOMER										Re	serv	/ed	for	cus	ton	ner																

14.1.52 CUSTOMER[24]

Address offset: 0x0E0
Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description

A RW CUSTOMER Reserved for customer



14.1.53 CUSTOMER[25]

Address offset: 0x0E4 Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

14.1.54 CUSTOMER[26]

Address offset: 0x0E8 Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field Value Id	Value Description
A RW CUSTOMER	Reserved for customer

A RW CUSTOMER Reserved for customer

14.1.55 CUSTOMER[27]

Address offset: 0x0EC Reserved for customer

Bit	numbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14 :	13 :	L2 1	11 1	0 9) 8	3 7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	A A		. Δ	. Δ	A	Α	Α	Α	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1	1	. 1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	CUSTOMER										Res	serv	ed	for	cus	ton	ner															

14.1.56 CUSTOMER[28]

Address offset: 0x0F0 Reserved for customer

Bit number	31 30 29	9 28 27 26 25 24 3	23 22 21 20 19 1	8 17 16 15 14 13 12	11 10 9 8 7 6 !	5 4 3 2 1 0
Id	A A A	4 A A A A A	A A A A A	A A A A A A	A A A A A A	A A A A A
Reset 0xFFFFFFF	1 1 1	11111	1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 :	1 1 1 1 1 1
Id RW Field Value	ld Value	r	Description			

A RW CUSTOMER Reserved for customer

14.1.57 CUSTOMER[29]

Address offset: 0x0F4 Reserved for customer

Bit number	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	5 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id	A A A A A A A	A A A A A A A	A A A A A A A	A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description		

A RW CUSTOMER Reserved for customer

14.1.58 CUSTOMER[30]

Address offset: 0x0F8 Reserved for customer



Bit r	numbe	r		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.59 CUSTOMER[31]

Address offset: 0x0FC Reserved for customer

Bit r	numbe	r		31	30 2	29 2	8 2	7 26	5 25	24	23	22 :	21	20 1	19 1	.8 1	7 1	5 15	5 14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id				А	Α	A A	A A	A	Α	Α	Α	Α	Α	Α.	A A	Δ	Α Α	A	A	Α	Α	Α	Α	Α	Α.	Α	A	4 4	A	Α	Α	Α
Res	et 0xF	FFFFFF		1	1	1 :	1 1	. 1	1	1	1	1	1	1	1 :	1 1	l 1	. 1	. 1	1	1	1	1	1	1	1	1	1 1	1	1	1	1
Id	RW	Field	Value Id	Val	ue						De	scrip	otic	n																		
Α	RW	CUSTOMER									Res	serv	ed ·	for o	cust	om	er															

14.1.60 PSELRESET[0]

Address offset: 0x200

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they don't, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bit	numbe	er		31 30 29 28 27 26 25	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		21	GPIO number P0.n onto which Reset is exposed
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

14.1.61 PSELRESET[1]

Address offset: 0x204

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they don't, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		21	GPIO number P0.n onto which Reset is exposed
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

14.1.62 APPROTECT

Address offset: 0x208
Access Port protection

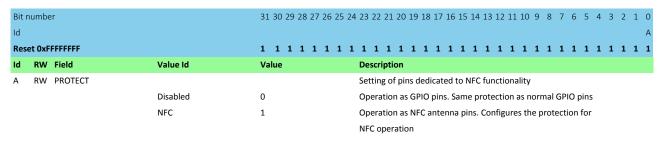


В	it n	umbe	r		31	30 2	9 2	8 2	7 26	25	24	23	22 2	1 2	0 1	9 1	8 17	16	15	14	13 3	12 1	1 10	9	8	7	6	5	4	3	2 1	1 0
le	b																									Α	Α	Α	Α	Α	A A	A A
R	lese	t OxF	FFFFFF		1	1 :	1 1	1 1	. 1	1	1	1	1	1 :	1 1	1	. 1	1	1	1	1	1 :	l 1	1	1	1	1	1	1	1	1 1	l 1
I	d	RW	Field	Value Id	Val	ue						Des	crip	tio	n																	
Δ	١.	RW	PALL									Ena	ble	or c	lisal	ole .	Acce	ess F	ort	pro	otec	tion										
												See	Del	oug	and	l tro	ice (n p	age	70	for	mor	e inf	orm	atio	n.						
				Disabled	0xF	F						Disa	able																			
				Enabled	0x0	00						Ena	ble																			

14.1.63 NFCPINS

Address offset: 0x20C

Setting of pins dedicated to NFC functionality: NFC antenna or GPIO





15 Peripheral interface

Peripherals are controlled by the CPU by writing to configuration registers and task registers. Peripheral events are indicated to the CPU by event registers and interrupts if they are configured for a given event.

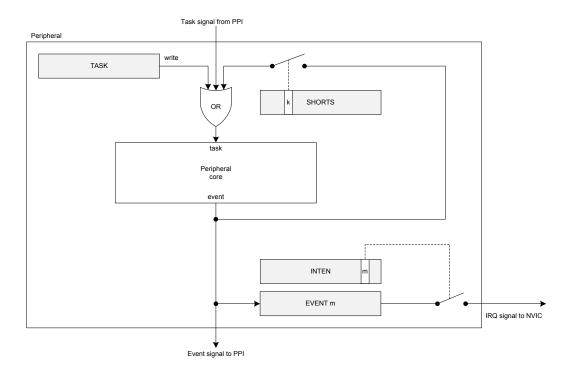


Figure 9: Tasks, events, shortcuts, and interrupts

15.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32 bit registers.

See *Instantiation* on page 21 for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between the peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Some peripherals share some registers or other common resources.
- Operation is mutually exclusive. Only one of the peripherals can be used at a time.
- Switching from one peripheral to another must follow a specific pattern (disable the first, then enable the second peripheral).

15.2 Peripherals with shared ID

In general, and with the exception of ID 0, peripherals sharing an ID and base address may not be used simultaneously. The user can only enable one at the time on this specific ID.

When switching between two peripherals that share an ID, the user should do the following to prevent unwanted behavior:



- · Disable the previously used peripheral
- Remove any PPI connections set up for the peripheral that is being disabled
- Clear all bits in the INTEN register, i.e. INTENCLR = 0xFFFFFFF.
- Explicitly configure the peripheral that you enable and do not rely on configuration values that may be inherited from the peripheral that was disabled.
- · Enable the now configured peripheral.

For each of the rows in the following table, the instance ID listed is shared by the peripherals in the same row.

Table 16: Peripherals sharing an ID

Instance						
ID 2 (0x40002000)	UARTE	UART				
-						
ID 3 (0x40003000)	SPIM	SPIS	SPI	TWIM	TWIS	TWI
ID 4 (0x40004000)	SPIM	SPIS	SPI	TWIM	TWIS	TWI
ID 35 (0x40023000)	SPIM	SPIS	SPI			
-						
ID 15 (0x4000F000)	AAR	CCM				
-						
ID 19 (0x40013000)	COMP	LPCOMP				
-						
ID 20 (0x40014000)	SWI	EGU				
ID 21 (0x40015000)	SWI	EGU				
ID 22 (0x40016000)	SWI	EGU				
ID 23 (0x40017000)	SWI	EGU				
ID 24 (0x40018000)	SWI	EGU				
ID 25 (0x40019000)	SWI	EGU				

15.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified in the relevant chapter, the peripheral registers (in particular the PSEL registers) must be configured before enabling the peripheral.

Note that the peripheral must be enabled before tasks and events can be used.

15.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the "set-and-clear" pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map where the main register is followed by a dedicated SET and CLR register in that order.

The SET register is used to set individual bits in the main register while the CLR register is used to clear individual bits in the main register. Writing a '1' to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing a '0' to a bit in the SET or CLR register has no effect. Reading the SET or CLR registers returns the value of the main register.

Restriction: The main register may not be visible and hence not directly accessible in all cases.

15.5 Tasks

Tasks are used to trigger actions in a peripheral, for example, to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes a '1' to the task register or when the peripheral itself or another peripheral toggles the corresponding task signal. See *Figure 9: Tasks, events, shortcuts, and interrupts* on page 66.



15.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example, a state change in a peripheral. A peripheral may generate multiple events with each event having a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated. See *Figure 9: Tasks, events, shortcuts, and interrupts* on page 66. An event register is only cleared when firmware writes a '0' to it.

Events can be generated by the peripheral even when the event register is set to '1'.

15.7 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, its associated task is automatically triggered when its associated event is generated.

Using a shortcut is the equivalent to making the same connection outside the peripheral and through the PPI. However, the propagation delay through the shortcut is usually shorter than the propagation delay through the PPI.

Shortcuts are predefined, which means their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

15.8 Interrupts

All peripherals support interrupts. Interrupts are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the Nested Vectored Interrupt Controller (NVIC).

Using the INTEN, INTENSET and INTENCLR registers, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR, and the INTEN register is not available on those peripherals. Refer to the individual chapters for details. In all cases, however, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is shown in *Figure 9: Tasks, events, shortcuts, and interrupts* on page 66.

15.8.1 Interrupt clearing

When clearing an interrupt by writing "0" to an event register, or disabling an interrupt using the INTENCLR register, it can take up to four CPU clock cycles to take effect. This means that an interrupt may reoccur immediatelly even if a new event has not come, if the program exits an interrupt handler after the interrupt is cleared or disabled, but before four clock cycles have passed.

Important: To avoid an interrupt reoccurring before a new event has come, the program should perform a read from one of the peripheral registers, for example, the event register that has been cleared, or the INTENCLR register that has been used to disable the interrupt.

This will cause a one to three-cycle delay and ensure the interrupt is cleared before exiting the interrupt handler. Care should be taken to ensure the compiler does not remove the read operation as an optimization. If the program can guarantee a four-cycle delay after event clear or interrupt disable another way, then a read of a register is not required.





16 Debug and trace

The debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

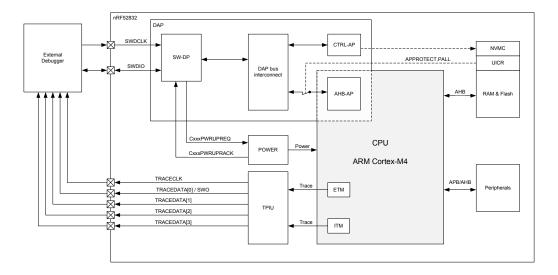


Figure 10: Debug and trace overview

The main features of the debug and trace system are:

- Two-pin Serial Wire Debug (SWD) interface
- Flash Patch and Breakpoint Unit (FPB) supports:
 - Two literal comparators
 - Six instruction comparators
- Data Watchpoint and Trace Unit (DWT)
 - · Four comparators
- Instrumentation Trace Macrocell (ITM)
- Embedded Trace Macrocell (ETM)
- Trace Port Interface Unit (TPIU)
 - 4-bit parallel trace of ITM and ETM trace data
 - · Serial Wire Output (SWO) trace of ITM data

16.1 DAP - Debug Access Port

An external debugger can access the device via the DAP.

The SW-DP implements the Serial Wire Debug protocol (SWD) that is a two-pin serial interface, see SWDCLK and SWDIO in *Figure 10: Debug and trace overview* on page 70.

In addition to the default access port in the CPU (AHB-AP), the DAP includes a custom Control Access Port (CTRL-AP). The CTRL-AP is described in more detail in *CTRL-AP - Control Access Port* on page 71.

Important:

- · The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.



16.2 CTRL-AP - Control Access Port

The Control Access Port (CTRL-AP) is a custom access port that enables control of the device even if the other access ports in the DAP are being disabled by the access port protection.

Access port protection blocks the debugger from read and write access to all CPU registers and memory-mapped addresses. See the UICR register *APPROTECT* on page 64 for more information about enabling access port protection.

This access port enables the following features:

- Soft reset, see Reset on page 80 for more information
- Disable access port protection

Access port protection can only be disabled by issuing an ERASEALL command via CTRL-AP. This command will erase the Flash, UICR, and RAM.

16.2.1 Registers

Table 17: Register Overview

Register	Offset	Description
RESET	0x000	Soft reset triggered through CTRL-AP
ERASEALL	0x004	Erase all
ERASEALLSTATUS	0x008	Status register for the ERASEALL operation
APPROTECTSTATUS	0x00C	Status register for access port protection
IDR	0x0FC	CTRL-AP Identification Register, IDR

RESET

Address offset: 0x000

Soft reset triggered through CTRL-AP

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW RESET			Soft reset triggered through CTRL-AP. See Reset Behaviour in
			POWER chapter for more details.
	NoReset	0	Reset is not active
	Reset	1	Reset is active. Device is held in reset

ERASEALL

Address offset: 0x004

Erase all

Bit	numbe	er		3	1 30	29	9 28	8 27	7 26	6 2	5 24	4 2	3 2	2 2	1 2	20 2	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0) (0 0) (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	9						D	eso	crip	tio	n																			
Α	W	ERASEALL										Ε	ras	e al	l FI	LAS	На	ınd	RA	M															
			NoOperation	0								Ν	lo c	pei	rati	ion																			
			Erase	1								Ε	ras	e al	l FI	LAS	На	ınd	RA	M															

ERASEALLSTATUS

Address offset: 0x008

Status register for the ERASEALL operation



Bit r	numbe	er		31 3	0 29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	L3 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																																Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	е						Des	scri	ptic	on																		
Α	R	ERASEALLSTATUS									Sta	tus	reg	giste	er fo	or th	ne E	RA	SEA	LL (ope	rati	on									
			Ready	0							ER/	ASE.	ALL	. is r	eac	dy																
			Busy	1							ER/	4SE	ALL	. is t	ousy	y (o	n-g	oing	g)													

APPROTECTSTATUS

Address offset: 0x00C

Status register for access port protection

Bit	numl	ber			31	30 :	29 2	28 2	27 2	26 :	25 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Re	et 0	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RV	N	Field	Value Id	Val	ue							De	scri	pti	on																			
Α	R		APPROTECTSTATUS										Sta	tus	re	gist	er f	or a	ссе	ess	por	t p	rote	ecti	on										
				Enabled	0								Acc	ess	рс	ort p	rot	ect	ion	en	abl	ed													
				Disabled	1								Acc	ess	рс	ort p	rot	ect	ion	no	t e	nab	led												

IDR

Address offset: 0x0FC

CTRL-AP Identification Register, IDR

Bitı	numb	er		31	1 30	29	28 2	27 :	26 2	25 24	1 23	22	21 2	20 1	19 1	8 1	7 16	5 15	14	13	12 1	.1 10	9	8	7	6	5	4	3 2	2 2	0 1
Id				Ε	Ε	Ε	Ε	D	D [D D	С	С	С	С	C (2 0	В	В	В	В					Α	Α	Α	Α	A	Α Α	А А
Res	et 0x0	2880000		0	0	0	0	0	0 :	1 0	1	0	0	0	1 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	alue	2					De	escri	otio	n																	
Α	R	APID									AF	Ide	ntifi	cati	ion																
В	R	CLASS									Ac	cess	Por	rt (A	AP) d	lass	;														
			NotDefined	0>	κ0						No	def	ined	d cla	ass																
			MEMAP	0>	ĸ8						M	emo	ry A	ссе	ss P	ort															
С	R	JEP106ID									JEI	DEC.	JEP:	106	ide	ntity	/ co	de													
D	R	JEP106CONT									JEI	DEC.	JEP:	106	cor	tinu	ıatio	on c	ode	9											
Е	R	REVISION									Re	visio	n																		

16.3 Debug interface mode

Before the external debugger can access the CPU's access port (AHB-AP) or the Control Access Port (CTRL-AP), the debugger must first request the device to power up via CxxxPWRUPREQ in the SWJ-DP.

As long as the debugger is requesting power via CxxxPWRUPREQ, the device will be in debug interface mode. If the debugger is not requesting power via CxxxPWRUPREQ, the device will be in normal mode.

Some peripherals will behave differently in debug interface mode compared to normal mode. These differences are described in more detail in the chapters of the peripherals that are affected.

When a debug session is over, the external debugger must make sure to put the device back into normal mode since the overall power consumption will be higher in debug interface mode compared to normal mode.

For details on how to use the debug capabilities please read the debug documentation of your IDE.

If the device is in System OFF when power is requested via CxxxPWRUPREQ, the system will wake up and the DIF flag in *RESETREAS* on page 83 will be set.

16.4 Real-time debug

The nRF52832 supports real-time debugging.



Real-time debugging will allow interrupts to execute to completion in real time when breakpoints are set in Thread mode or lower priority interrupts. This enables the developer to set a breakpoint and single-step through their code without a failure of the real-time event-driven threads running at higher priority. For example, this enables the device to continue to service the high-priority interrupts of an external controller or sensor without failure or loss of state synchronization while the developer steps through code in a low-priority thread.

16.5 Trace

The device supports ETM and ITM trace.

Trace data from the ETM and the ITM is sent to an external debugger via a 4-bit wide parallel trace port (TPIU), see TRACEDATA[0] through TRACEDATA[3] and TRACECLK in *Figure 10: Debug and trace overview* on page 70.

In addition to parallel trace, the TPIU supports serial trace via the Serial Wire Output (SWO) trace protocol.

Parallel and serial trace cannot be used at the same time.

ETM trace is only supported in parallel trace mode while ITM trace is supported in both parallel and serial trace modes.

For details on how to use the trace capabilities, please read the debug documentation of your IDE.

TPIU's trace pins are multiplexed with GPIOs, and SWO and TRACEDATA[0] use the same GPIO, see *Pin assignments* on page 13 for more information.

Trace speed is configured in the *TRACECONFIG* on page 105 register.

The speed of the trace pins depends on the DRIVE setting of the GPIOs that the trace pins are multiplexed with, see *PIN_CNF[14]* on page 139, *PIN_CNF[15]* on page 139, *PIN_CNF[16]* on page 140, *PIN_CNF[18]* on page 141 and *PIN_CNF[20]* on page 143. Only S0S1 and H0H1 drives are suitable for debugging. S0S1 is the default DRIVE at reset. If parallel or serial trace port signals are not fast enough in the debugging conditions, all GPIOs in use for tracing should be set to high drive (H0H1). The user shall make sure that these GPIOs' DRIVE is not overwritten by software during the debugging session.

16.5.1 Electrical Specification

Trace port

Symbol	Description	Min.	Тур.	Max.	Units
T _{cyc}	Clock period, as defined by ARM (See ARM Infocenter,	62.5		500	ns
	Embedded Trace Macrocell Architecture Specification, Trace				
	Port Physical Interface, Timing specifications)				



17 Power and clock management

Power and clock management in nRF52832 is optimized for ultra-low power applications.

The core of the power and clock management system is the Power Management Unit (PMU) illustrated in *Figure 11: Power Management Unit* on page 74.

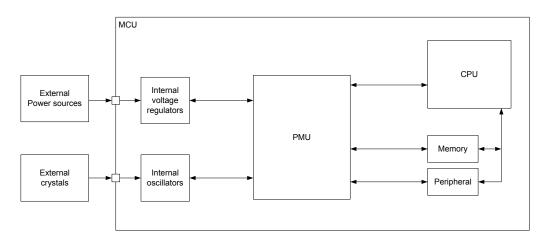


Figure 11: Power Management Unit

The user application is not required to actively control power and clock, since the PMU is able to automatically detect which resources are required by the different components in the system at any given time. The PMU will continuously optimize the system based on this information to achieve the lowest power consumption possible without user interaction.

17.1 Current consumption scenarios

As the system is being constantly tuned by the PMU, estimating the energy consumption of an application can be challenging if the designer is not able to do measurements on the hardware directly. See *Electrical Specification* on page 74 for application scenarios showing average current drawn from the VDD supply.

Each scenario specifies a set of active operations and conditions applying to the given scenario. *Table 18: Current consumption scenarios, common conditions* on page 74 shows the conditions used for a scenario unless otherwise is stated in the scenario description.

Table 18: Current consumption scenarios, common conditions

Condition	Value
VDD	3 V
Temperature	25°C
CPU	WFI/WFE sleep
Peripherals	All idle
Clock	Not running
Clock Regulator	DCDC

17.1.1 Electrical Specification

Current consumption: Radio

			_			
Symbol	Description	Min.	Тур.	Max.	Units	
I _{RADIO_TX0}	0 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		7.1		mA	
I _{RADIO_TX1}	-40 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock =		4.1		mA	
	HFXO					
I _{RADIO RXO}	Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		6.5		mA	



Current consumption: Radio protocol configurations

Symbol	Description	Min.	Тур.	Max.	Units
I _{SO}	CPU running CoreMark from Flash, Radio 0 dBm TX @ 1 Mb/s		9.6		mA
	Bluetooth Low Energy mode, Clock = HFXO, Cache enabled				
I _{S1}	CPU running CoreMark from Flash, Radio RX @ 1 Mb/s		9.0		mA
	Bluetooth Low Energy mode, Clock = HFXO, Cache enabled				

Current consumption: Ultra-low power

Symbol	Description	Min.	Тур.	Max.	Units
I _{ON_RAMOFF_EVENT}	System ON, No RAM retention, Wake on any event		1.2		μΑ
I _{ON_RAMON_EVENT}	System ON, Full RAM retention, Wake on any event		1.5		μΑ
I _{ON_RAMOFF_RTC}	System ON, No RAM retention, Wake on RTC		1.9		μΑ
I _{OFF_RAMOFF_RESET}	System OFF, No RAM retention, Wake on reset		0.7		μΑ
I _{OFF_RAMOFF_GPIO}	System OFF, No RAM retention, Wake on GPIO		1.2		μΑ
I _{OFF_RAMOFF_LPCOMP}	System OFF, No RAM retention, Wake on LPCOMP		1.9		μΑ
I _{OFF_RAMOFF_NFC}	System OFF, No RAM retention, Wake on NFC field		0.7		μΑ
I _{OFF_RAMON_RESET}	System OFF, Full RAM retention, Wake on reset		1.0		μΑ



18 POWER — Power supply

This device has the following power supply features:

- · On-chip LDO and DC/DC regulators
- Global System ON/OFF modes
- Individual RAM section power control for all system modes
- · Analog or digital pin wakeup from System OFF
- Supervisor HW to manage power on reset, brownout, and power fail
- Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency
- Automatic switching between LDO and DC/DC regulator based on load to maximize efficiency

Note: Two additional external passive components are required to use the DC/DC regulator.

18.1 Regulators

The following internal power regulator alternatives are supported:

- · Internal LDO regulator
- · Internal DC/DC regulator

The LDO is the default regulator.

The DC/DC regulator can be used as an alternative to the LDO regulator and is enabled through the *DCDCEN* on page 86 register. Using the DC/DC regulator will reduce current consumption compared to when using the LDO regulator, but the DC/DC regulator requires an external LC filter to be connected, as shown in *Figure 13: DC/DC regulator setup* on page 77.

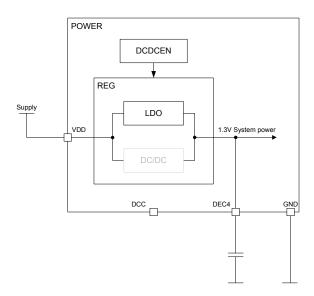


Figure 12: LDO regulator setup



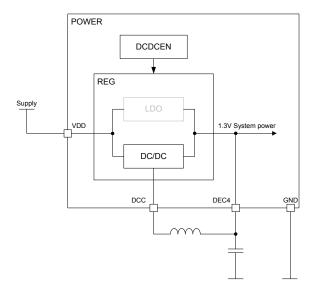


Figure 13: DC/DC regulator setup

18.2 System OFF mode

System OFF is the deepest power saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.

The device can be put into System OFF mode using the POWER register interface. When in System OFF mode, the device can be woken up through one of the following signals:

- 1. The DETECT signal, optionally generated by the GPIO peripheral
- 2. The ANADETECT signal, optionally generated by the LPCOMP module
- 3. The SENSE signal, optionally generated by the NFC module to "wake-on-field"
- 4. A reset

When the system wakes up from System OFF mode, it gets reset. For more details, see *Reset behavior* on page 81.

One or more RAM sections can be retained in System OFF mode depending on the settings in the RAM[n].POWER registers.

RAM[n].POWER are retained registers, see *Reset behavior*. Note that these registers are usually overwritten by the startup code provided with the nRF application examples.

Before entering System OFF mode, the user must make sure that all on-going EasyDMA transactions have been completed. This is usually accomplished by making sure that the EasyDMA enabled peripheral is not active when entering System OFF.

18.2.1 Emulated System OFF mode

If the device is in debug interface mode, System OFF will be emulated to secure that all required resources needed for debugging are available during System OFF.

See *Debug and trace* on page 70 for more information. Required resources needed for debugging include the following key components: *Debug and trace* on page 70, *CLOCK* — *Clock control* on page 98, *POWER* — *Power supply* on page 76, *NVMC* — *Non-volatile memory controller* on page 26, CPU, Flash, and RAM. Since the CPU is kept on in an emulated System OFF mode, it is recommended to add an infinite loop directly after entering System OFF, to prevent the CPU from executing code that normally should not be executed.



18.3 System ON mode

System ON is the default state after power-on reset. In System ON, all functional blocks such as the CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing.

Register *RESETREAS* on page 83 provides information about the source that caused the wakeup or reset.

The system can switch on and off the appropriate internal power sources, depending on how much power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral is usually raised and lowered when specific tasks are triggered or events are generated.

18.3.1 Sub power modes

In System ON mode, when both the CPU and all the peripherals are in IDLE mode, the system can reside in one of the two sub power modes.

The sub power modes are:

- · Constant latency
- Low power

In constant latency mode the CPU wakeup latency and the PPI task response will be constant and kept at a minimum. This is secured by forcing a set of base resources on while in sleep. The advantage of having a constant and predictable latency will be at the cost of having increased power consumption. The constant latency mode is selected by triggering the CONSTLAT task.

In low power mode the automatic power management system, described in *System ON mode* on page 78, ensures the most efficient supply option is chosen to save the most power. The advantage of having the lowest power possible will be at the cost of having varying CPU wakeup latency and PPI task response. The low power mode is selected by triggering the LOWPWR task.

When the system enters System ON mode, it will, by default, reside in the low power sub-power mode.

18.4 Power supply supervisor

The power supply supervisor initializes the system at power-on and provides an early warning of impending power failure.

In addition, the power supply supervisor puts the system in a reset state if the supply voltage is too low for safe operation (brownout). The power supply supervisor is illustrated in *Figure 14: Power supply supervisor* on page 79.



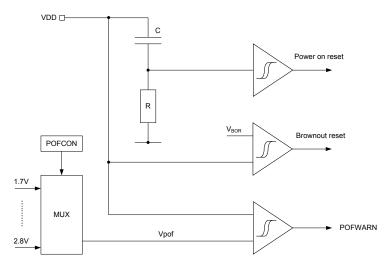


Figure 14: Power supply supervisor

18.4.1 Power-fail comparator

The power-fail comparator (POF) can provide the CPU with an early warning of impending power failure. It will not reset the system, but give the CPU time to prepare for an orderly power-down.

The comparator features a hysteresis of V_{HYST} , as illustrated in *Figure 15: Power-fail comparator (BOR = Brownout reset)* on page 79. The threshold V_{POF} is set in register *POFCON* on page 84. If the POF is enabled and the supply voltage falls below V_{POF} , the POFWARN event will be generated. This event will also be generated if the supply voltage is already below V_{POF} at the time the POF is enabled, or if V_{POF} is reconfigured to a level above the supply voltage.

If power-fail warning is enabled and the supply voltage is below V_{POF} the power-fail comparator will prevent the NVMC from performing write operations to the NVM. See NVMC - Non-volatile memory controller on page 26 for more information about the NVMC.

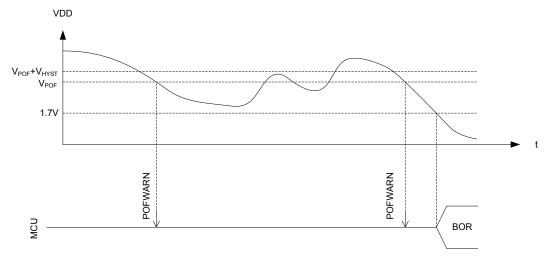


Figure 15: Power-fail comparator (BOR = Brownout reset)

To save power, the power-fail comparator is not active in System OFF or in System ON when HFCLK is not running.

18.5 RAM sections

RAM section power control is used for retention in System OFF mode and for powering down unused sections in System ON mode.



Each RAM section can power up and down independently in both System ON and System OFF mode. See chapter *Memory* for more information on RAM sections.

18.6 Reset

There are multiple sources that may trigger a reset.

After a reset has occurred, register *RESETREAS* can be read to determine which source generated the reset.

18.6.1 Power-on reset

The power-on reset generator initializes the system at power-on.

The system is held in reset state until the supply has reached the minimum operating voltage and the internal voltage regulators have started.

A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

18.6.2 Pin reset

A pin reset is generated when the physical reset pin on the device is asserted.

Pin reset is configured via the *PSELRESET[0]* and *PSELRESET[1]* registers.

18.6.3 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

The DAP is not reset following a wake up from System OFF mode if the device is in debug interface mode. Refer to chapter *Debug and trace* on page 70 for more information.

18.6.4 Soft reset

A soft reset is generated when the SYSRESETREQ bit of the Application Interrupt and Reset Control Register (AIRCR register) in the ARM® core is set.

Refer to ARM documentation for more details.

A soft reset can also be generated via the *RESET* on page 71 register in the CTRL-AP.

18.6.5 Watchdog reset

A Watchdog reset is generated when the watchdog times out.

Refer to chapter WDT — Watchdog timer on page 405 for more information.

18.6.6 Brown-out reset

The brown-out reset generator puts the system in reset state if the supply voltage drops below the brownout reset (BOR) threshold.

Refer to section *Power fail comparator* on page 97 for more information.

18.7 Retained registers

A retained register is a register that will retain its value in System OFF mode and through a reset, depending on reset source. See individual peripheral chapters for information of which registers are retained for the various peripherals.



18.8 Reset behavior

Reset source	Reset target CPU	Peripherals	GPIO	Debug ^a	SWJ-DP	RAM	WDT	Retained registers	RESETREAS
CPU lockup ⁴	х	х	х						
Soft reset	X	x	Х						
Wakeup from System OFF mode reset	х	х		x ⁵		x ⁶			
Watchdog reset ⁷	Х	x	Х	Х		х	х	х	
Pin reset	х	x	х	x		x	х	х	
Brownout reset	Х	X	Х	х	x	x	х	Х	х
Power on reset	х	х	x	х	х	х	X	х	х

Note: The RAM is never reset, but depending on reset source, RAM content may be corrupted.

18.9 Registers

Table 19: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40000000	POWER	POWER	Power Control	

Table 20: Register Overview

Register	Offset	Description	
TASKS_CONSTLAT	0x078	Enable constant latency mode	
TASKS_LOWPWR	0x07C	Enable low power mode (variable latency)	
EVENTS_POFWARN	0x108	Power failure warning	
EVENTS_SLEEPENTER	0x114	CPU entered WFI/WFE sleep	
EVENTS_SLEEPEXIT	0x118	CPU exited WFI/WFE sleep	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
RESETREAS	0x400	Reset reason	
RAMSTATUS	0x428	RAM status register	Deprecated
SYSTEMOFF	0x500	System OFF register	
POFCON	0x510	Power failure comparator configuration	
GPREGRET	0x51C	General purpose retention register	
GPREGRET2	0x520	General purpose retention register	
RAMON	0x524	RAM on/off register (this register is retained)	Deprecated
RAMONB	0x554	RAM on/off register (this register is retained)	Deprecated
DCDCEN	0x578	DC/DC enable register	
RAM[0].POWER	0x900	RAM0 power control register	
RAM[0].POWERSET	0x904	RAM0 power control set register	
RAM[0].POWERCLR	0x908	RAM0 power control clear register	
RAM[1].POWER	0x910	RAM1 power control register	
RAM[1].POWERSET	0x914	RAM1 power control set register	
RAM[1].POWERCLR	0x918	RAM1 power control clear register	
RAM[2].POWER	0x920	RAM2 power control register	

^a All debug components excluding SWJ-DP. See *Debug and trace* on page 70 chapter for more information about the different debug components in the system.

⁴ Reset from CPU lockup is disabled if the device is in debug interface mode. CPU lockup is not possible in System OFF.

⁵ The Debug components will not be reset if the device is in debug interface mode.

RAM is not reset on wakeup from OFF mode, but depending on settings in the RAM registers parts, or the whole RAM, may not be retained after the device has entered System OFF mode.

Watchdog reset is not available in System OFF.



Register	Offset	Description
RAM[2].POWERSET	0x924	RAM2 power control set register
RAM[2].POWERCLR	0x928	RAM2 power control clear register
RAM[3].POWER	0x930	RAM3 power control register
RAM[3].POWERSET	0x934	RAM3 power control set register
RAM[3].POWERCLR	0x938	RAM3 power control clear register
RAM[4].POWER	0x940	RAM4 power control register
RAM[4].POWERSET	0x944	RAM4 power control set register
RAM[4].POWERCLR	0x948	RAM4 power control clear register
RAM[5].POWER	0x950	RAM5 power control register
RAM[5].POWERSET	0x954	RAM5 power control set register
RAM[5].POWERCLR	0x958	RAM5 power control clear register
RAM[6].POWER	0x960	RAM6 power control register
RAM[6].POWERSET	0x964	RAM6 power control set register
RAM[6].POWERCLR	0x968	RAM6 power control clear register
RAM[7].POWER	0x970	RAM7 power control register
RAM[7].POWERSET	0x974	RAM7 power control set register
RAM[7].POWERCLR	0x978	RAM7 power control clear register

18.9.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					СВА
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	POFWARN			Write '1' to Enable interrupt for POFWARN event
					See EVENTS_POFWARN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	SLEEPENTER			Write '1' to Enable interrupt for SLEEPENTER event
					See EVENTS_SLEEPENTER
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	SLEEPEXIT			Write '1' to Enable interrupt for SLEEPEXIT event
					See EVENTS_SLEEPEXIT
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

18.9.2 INTENCLR

Address offset: 0x308 Disable interrupt

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Bit number Reset 0x00000000 Id RW Field Value Id Value A RW POFWARN Write '1' to Disable interrupt for POFWARN event See EVENTS_POFWARN Clear 1 Disable Disabled 0 Read: Disabled Enabled Read: Enabled



Bit	numbe	er		33	1 30	29	28	27	26	25	24	23 :	22	21	. 20	19	18	3 1	7 10	5 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																													С	В			Α	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	C	0	() () () () (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue							Des	scr	ipti	ion																			
В	RW	SLEEPENTER										Wri	ite	'1'	to [Disa	able	e ir	ter	rup	ot fo	or S	LEE	PEN	ITER	eve	ent							
												See	<i>E</i>	VEN	VTS_	SL	EEF	PEN	ITEI	?														
			Clear	1								Disa	ab	le																				
			Disabled	0								Rea	ad:	Dis	sabl	ed																		
			Enabled	1								Rea	ad:	En	able	ed																		
С	RW	SLEEPEXIT										Wri	ite	'1'	to [Disa	able	e ir	ter	rup	ot fo	or S	LEE	PEX	IT e	ven	t							
												See	<i>E</i>	VEN	VTS_	SL	EEF	PEX	ΊΤ															
			Clear	1								Disa	ab	le																				
			Disabled	0								Rea	ad:	Dis	sabl	ed																		
			Enabled	1								Rea	ad:	En	able	ed																		

18.9.3 RESETREAS

Address offset: 0x400

Reset reason

Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing '1' to it. If none of the reset sources are flagged, this indicates that the chip was reset from the on-chip reset generator, which will indicate a power-on-reset or a brownout reset.

Reset Doctor Do	Bit n	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW RESETPIN Reset from pin-reset detected NotDetected 0 Not detected Detected 1 Detected B RW DOG Reset from watchdog detected NotDetected 0 Not detected Detected 1 Detected NotDetected 0 Not detected Detected 1 Detected E RW OFF Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO NotDetected 1 Detected F RW LPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from be	Id				H G F E D C B A
A RW RESETPIN NotDetected 0 Not detected Detected 1 Detected B RW DOG NotDetected 0 Not detected NotDetected 1 Detected NotDetected 0 Not detected Detected 1 Detected NotDetected 1 Detected C RW SREQ NotDetected 0 Not detected Detected 1 Detected NotDetected 1 Detected Detected 1 Detected Detected 1 Detected Detected 1 Detected NotDetected 1 Detected Detected 1 Detected NotDetected 0 Not detected Detected 1 Detected Detected 1 Detected Reset from CPU lock-up detected Not detected Detected 1 Detected E RW OFF Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO NotDetected 0 Not detected Detected 1 Detected F RW LPCOMP NotDetected 0 Not detected NotDetected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 1 Detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode	Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Not Detected 0 Not detected 1 Det	Id	RW Field	Value Id	Value	Description
B RW DOG Reset from watchdog detected NotDetected 0 Not detected Detected 1 Detected C RW SREQ Reset from soft reset detected NotDetected 0 Not detected Detected 1 Detected Detected 1 Detected Detected 1 Detected Detected 1 Detected NotDetected 1 Detected NotDetected 0 Not detected Reset from CPU lock-up detected NotDetected 1 Detected Not Detected NotDetected 1 Detected Not Detected Not detected Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO NotDetected 1 Detected F RW LPCOMP NotDetected 0 Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode	Α	RW RESETPIN			Reset from pin-reset detected
Reset from watchdog detected NotDetected Detected Det			NotDetected	0	Not detected
Not Detected 0 Not detected Detected 1 Detected C RW SREQ Reset from soft reset detected Not Detected 0 Not detected Detected 1 Detected Detected 1 Detected Not Detected 0 Not detected Detected 1 Detected Detected 0 Not detected Detected 1 Detected E RW OFF Reset from CPU lock-up detected NotDetected 1 Detected E Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO Not Detected 1 Detected F RW LPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected F Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			Detected	1	Detected
Detected 1 Detected Reset from soft reset detected Not detected Not detected Detected 1 Detected Detected Detected 1 Detected Not Detected Not Detected 0 Not detected Detected Detected 1 Detected E RW OFF Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO Not Detected 1 Detected F RW LPCOMP RW LPCOMP NotDetected 0 Not detected Detected 1 Detected Not Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Not Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode	В	RW DOG			Reset from watchdog detected
C RW SREQ NotDetected Detected Detected Detected Detected Detected Detected Detected Detected NotDetected NotDetected Detected Detected NotDetected Detected Detected Detected E RW OFF RW OFF NotDetected Detected Detected Detected Detected Detected NotDetected NotDetected Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO NotDetected Detected Detected F RW LPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected Detected Not detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not detected Detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			NotDetected	0	Not detected
NotDetected 0 Not detected Detected 1 Detected Detected 1 Detected Reset from CPU lock-up detected NotDetected 0 Not detected Detected 1 Detected E RW OFF RW LOCKUP Reset from CPU lock-up detected NotDetected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO NotDetected 0 Not detected Detected 1 Detected F RW LPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Not Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			Detected	1	Detected
Detected 1 Detected Detected 0 NotDetected 0 Not detected E RW OFF Reset from CPU lock-up detected NotDetected 1 Detected E RW OFF Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO NotDetected 0 Not detected Detected 1 Detected F RW LPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not Detected 1 Detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode	С	RW SREQ			Reset from soft reset detected
D RW LOCKUP NotDetected NotDetected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO NotDetected Detected 1 Detected Not detected Detected Procedular of the striggered from ANADETECT signal from LPCOMP NotDetected NotDetected Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected Detected Not detected Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not detected Detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			NotDetected	0	Not detected
NotDetected 0 Not detected E RW OFF RW OFF RW LPCOMP NotDetected 0 NotDetected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO Not detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			Detected	1	Detected
E RW OFF NotDetected 0 Not Detected 1 Detected NotDetected 0 Not detected Detected 1 Detected F RW LPCOMP NotDetected 0 NotDetected 1 Detected NotDetected 0 Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode	D	RW LOCKUP			Reset from CPU lock-up detected
Reset due to wake up from System OFF mode when wakeup is triggered from DETECT signal from GPIO NotDetected 0 Not detected Detected 1 Detected F RW LPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			NotDetected	0	Not detected
triggered from DETECT signal from GPIO NotDetected 0 Not detected Detected 1 Detected F RW LPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not Detected 1 Detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			Detected	1	Detected
NotDetected 0 Not detected Detected 1 Detected F RW LPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode	Ε	RW OFF			Reset due to wake up from System OFF mode when wakeup is
F RW LPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected Detected Detected 1 Detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP Not detected Detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode					triggered from DETECT signal from GPIO
Reset due to wake up from System OFF mode when wakeup is triggered from ANADETECT signal from LPCOMP NotDetected 0 Not detected Detected 1 Detected Reset due to wake up from System OFF mode when wakeup is triggered from EPCOMP Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			NotDetected	0	Not detected
triggered from ANADETECT signal from LPCOMP Not Detected Detected Detected Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			Detected	1	Detected
NotDetected 0 Not detected Detected 1 Detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode	F	RW LPCOMP			Reset due to wake up from System OFF mode when wakeup is
Detected 1 Detected G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode					triggered from ANADETECT signal from LPCOMP
G RW DIF Reset due to wake up from System OFF mode when wakeup is triggered from entering into debug interface mode			NotDetected	0	Not detected
triggered from entering into debug interface mode			Detected	1	Detected
**	G	RW DIF			Reset due to wake up from System OFF mode when wakeup is
NotDetected 0 Not detected					triggered from entering into debug interface mode
			NotDetected	0	Not detected
Detected 1 Detected			Detected	1	Detected
H RW NFC Reset due to wake up from System OFF mode by NFC field	Н	RW NFC			Reset due to wake up from System OFF mode by NFC field
detect					detect
NotDetected 0 Not detected			NotDetected	0	Not detected
Detected 1 Detected			Detected	1	Detected



18.9.4 RAMSTATUS (Deprecated)

Address offset: 0x428 RAM status register

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM1.S0, RAM block 1 is equivalent to a block comprising RAM2.S0 and RAM3.S0, RAM block 2 is equivalent to a block comprising RAM4.S0 and RAM5.S0 and RAM block 3 is equivalent to a block comprising RAM6.S0 and RAM7.S0. A RAM block field will indicate ON as long as any of the RAM sections associated with a block are on.

Bit r	umbe	er		31	30 29	9 2	8 27	7 26	5 25	24	23 2	2 2	21 2	0 1	19 1	18	17 1	16	15 1	14 :	13 :	L2 1	1 1	9	8	7	6	5	4	3 2	1	0
Id																														ОС	В	Α
Rese	t 0x0	0000000		0	0 0	(0 0	0	0	0	0	0	0 0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tior	1																		
Α	R	RAMBLOCK0									RAN	1 bl	ock	0 i	s or	1 0	r off	f/p	owe	rin	g u	0										
			Off	0							Off																					
			On	1							On																					
В	R	RAMBLOCK1									RAN	1 bl	ock	1 i	s or	1 0	r off	f/p	owe	rin	g u	0										
			Off	0							Off																					
			On	1							On																					
С	R	RAMBLOCK2									RAN	1 bl	ock	2 i	s or	1 0	r off	f/p	owe	rin	g u	0										
			Off	0							Off																					
			On	1							On																					
D	R	RAMBLOCK3									RAN	1 bl	ock	3 i	s or	1 0	r off	f/p	owe	rin	g u	0										
			Off	0							Off																					
			On	1							On																					

18.9.5 SYSTEMOFF

Address offset: 0x500 System OFF register

Bitı	numb	er		31	1 30	29	28	27 2	6 2	25 2	4 2	3 2	2 2:	1 2	0 19	9 18	3 17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																																Α
Res	et 0x0	0000000		0	0	0	0	0 () (0 0) () (0) (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue						D	esc	ript	tior	1																	
Α	W	SYSTEMOFF									Е	nab	le S	yst	em	OF	mo	ode														
			Enter	1							Е	nab	le S	yst	em	OF	mo	ode														

18.9.6 POFCON

Address offset: 0x510

Power failure comparator configuration

Bit r	numbe	r		31	30	29 .	28 2	7 2	26 2	5 2	4 2	23 2	2 2:	1 20) 19	9 18	3 17	16	15	14	13 :	L2 1	1 10	9	8	7	6	5	4 3	3 2	1	0
Id																													ВЕ	3 B	В	Α
Res	et 0x0	0000000		0	0	0	0 (0	0 0) ()	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Val	lue							Desc	ript	ion																		
Α	RW	POF									Е	nab	ole o	r di	isab	le p	oow	er f	ailu	re c	omį	oara	tor									
			Disabled	0							[Disal	ble																			
			Enabled	1							E	nab	ole																			
В	RW	THRESHOLD									F	owe	er fa	ailur	re c	om	par	ator	thr	esh	old	sett	ing									
			V17	4							S	Set t	hre	shol	ld t	o 1.	7 V															
			V18	5							S	Set t	hre	shol	ld t	o 1.	.8 V															
			V19	6							S	Set t	hre	shol	ld t	o 1.	.9 V															
			V20	7							S	Set t	hre	shol	ld t	o 2.	.0 V															
			V21	8							S	Set t	hre	shol	ld t	o 2.	1 V															
			V22	9							S	Set t	hre	shol	ld t	o 2.	2 V															
			V23	10							S	Set t	hre	shol	ld t	o 2.	.3 V															



Bit number	31 30 29 28 3	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		B B B A
Reset 0x00000000	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
V24	11	Set threshold to 2.4 V
V25	12	Set threshold to 2.5 V
V26	13	Set threshold to 2.6 V
V27	14	Set threshold to 2.7 V
V28	15	Set threshold to 2.8 V

18.9.7 GPREGRET

Address offset: 0x51C

General purpose retention register

Bi	t numb	er		31 :	30 29	9 2	8 27	7 26	25	24	23 2	22 2	1 2	0 19	9 18	17	16	15	14 1	13 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																									Α	Α	Α	A	4 A	Α	. A
Re	eset Ox	00000000		0	0 0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	ue						Des	crip	tior	1																	
Α	RW	GPREGRET									Gen	nera	l pu	rpo	se r	eter	tior	ı re	giste	er											

This register is a retained register

18.9.8 GPREGRET2

Address offset: 0x520

General purpose retention register

Bit	numbe	er		31 30 29 28 27	7 26 25 24 23 22 21 20 19	9 18 17 16 15 14	13 12 11 10	9 8	7	6 5	4	3 2	2 1 0
Id									Α	А А	Α	A A	A A A
Res	et 0x0	0000000		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0	0 0	0	0 0	0	0 0	0 0
Id	RW	Field	Value Id	Value	Description								
Α	RW	GPREGRET			General purpos	se retention regis	ster						

This register is a retained register

18.9.9 RAMON (Deprecated)

Address offset: 0x524

RAM on/off register (this register is retained)

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM0.S1 and RAM block 1 is equivalent to a block comprising RAM1.S0 and RAM1.S1. For new designs it is recommended to use the POWER.RAM-0.POWER and its sibling registers instead.

В	it numb	er		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
lo	ł				D C B A
R	eset 0x	00000003		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
le	l RW	Field	Value Id	Value	Description
Α	RW	ONRAM0			Keep RAM block 0 on or off in system ON Mode
			RAM0Off	0	Off
			RAM0On	1	On
В	RW	ONRAM1			Keep RAM block 1 on or off in system ON Mode
			RAM1Off	0	Off
			RAM10n	1	On
C	RW	OFFRAM0			Keep retention on RAM block 0 when RAM block is switched off
			RAM0Off	0	Off
			RAM0On	1	On
D	RW	OFFRAM1			Keep retention on RAM block 1 when RAM block is switched off
			RAM1Off	0	Off



Bit number	31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		D C B
Reset 0x00000003	0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value	Description
RAM1On	1	On

18.9.10 RAMONB (Deprecated)

Address offset: 0x554

RAM on/off register (this register is retained)

Since this register is deprecated the following substitutions have been made: RAM block 2 is equivalent to a block comprising RAM2.S0 and RAM2.S1 and RAM block 3 is equivalent to a block comprising RAM3.S0 and RAM3.S1. For new designs it is recommended to use the POWER.RAM-0.POWER and its sibling registers instead.

																											_				_		
Bit r	umbe	r		31	30 29	9 2	28 27	7 21	6 25	24	23	22	21 2	0 1	19 1	L8 :	17	16	15	14	13	12	11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id																	D	С														В	Α
Rese	t 0x0	0000003		0	0 0) (0 0	0	0	0	0	0	0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	1	1
Id	RW	Field	Value Id	Va	lue						Des	cri	ptio	ı																			
Α	RW	ONRAM2									Kee	рR	AM	blc	ock :	2 о	n o	r o	ff in	sy:	ter	n O	NΝ	/lod	e								
			RAM2Off	0							Off																						
			RAM2On	1							On																						
В	RW	ONRAM3									Kee	рR	AM	blc	ock 3	3 о	n o	r o	ff in	sy:	ter	n O	N N	/lod	e								
			RAM3Off	0							Off																						
			RAM3On	1							On																						
С	RW	OFFRAM2									Kee	рr	eten	tio	n oı	n R	ΑN	1 bl	ock	2 v	/he	n R	AΜ	blo	ck	is sv	wite	che	d of	f			
			RAM2Off	0							Off																						
			RAM2On	1							On																						
D	RW	OFFRAM3									Kee	рr	eten	tio	n oı	n R	ΑN	1 bl	ock	3 v	/he	n R	ΑM	blo	ck	is sv	wit	che	d of	f			
			RAM3Off	0							Off																						
			RAM3On	1							On																						

18.9.11 DCDCEN

Address offset: 0x578 DC/DC enable register

E	it n	umbe	er		31 30	29	28	27	26	25	24	23	22 2	21 2	20 :	19 1	8 1	.7 1	6 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
1	t																																Α
F	ese	t 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () () () () (0	0	0	0	0	0	0	0	0	0 0
ı	t	RW	Field	Value Id	Value	!						De	scrip	otio	n																		
P		RW	DCDCEN									Ena	able	or (disa	ble	DC	/DC	со	nve	rte	r											
				Disabled	0							Dis	able	:																			
				Enabled	1							Ena	able																				

18.9.12 RAM[0].POWER

Address offset: 0x900

RAM0 power control register

Bitı	numbe	er		31	L 30	29	28	27	26	25	24	23	22	21	20	19	18	3 1	7 1	6 1	5 14	4 13	3 12	2 13	10	9	8	7	6	5	4	3	2	1 0
Id																		0) (ВА
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	(0) 1	. 1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ipti	on																			
Α	RW	SOPOWER										Ke	ер І	RAI	VI s	ect	ion	S0	01	l or	OF	F in	Sy	ter	n O	N m	ode	2.						
												RA	M s	sect	ior	ns a	re	alw	ays	re	ain	ed	wh	en (ON,	but	car	als	so b	e				
												ret	ain	ed	wh	en	OF	F d	epe	nde	ent	on	the	set	ting	s in	S0	RET	ENT	ΠΟΙ	N.			
												ΑII	RA	Ms	ec	tior	ns v	vill	be	OFI	in	Sys	ten	ı Ol	F n	nod	e.							
			Off	0								Off																						



Bitı	number			31 30 2	29 28 2	7 26 25	24 23	3 22 21	1 20	19 18	3 17 1	16 15	14 13	3 12 1	1 10	9 8	7	6 5	4	3 2	1 0
Id											D	С									ВА
Res	et 0x0000FFF	F		0 0	0 0 0	0 0	0 0	0 0	0	0 0	0	0 1	1 1	. 1 :	l 1	1 1	1	1 1	1	1 1	1 1
Id	RW Field	,	Value Id	Value			D	escript	ion												
			On	1			0	n													
В	RW S1PO	VER					Ke	eep RA	M se	ction	S1 O	N or (OFF in	Syste	m ON	mod	е.				
							R	AM sec	ctions	s are a	alway	s reta	ained	when	ON, b	ut ca	n also	o be			
							re	etained	l whe	n OFF	dep	ende	nt on	the se	ttings	in S1	RETE	NTIC	N.		
							Α	II RAM	secti	ions w	vill be	OFF	in Sys	tem C	FF mo	de.					
			Off	0			0	ff													
			On	1			0	n													
С	RW SORET	ENTION					Ke	eep ret	entic	on on	RAM	secti	on S0	when	RAM	secti	on is	in O	FF		
			Off	0			0	ff													
			On	1			0	n													
D	RW S1RET	ENTION					Ke	eep ret	entic	on on	RAM	secti	on S1	when	RAM	secti	on is	in O	FF		
			Off	0			0	ff													
			On	1			0	n													

18.9.13 RAM[0].POWERSET

Address offset: 0x904

RAM0 power control set register

When read, this register will return the value of the POWER register.

Bitı	numbe	er		31	30 2	9 2	28 27	7 26	5 25	24	23	22	21	20	19	18	17	16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																	D	С															ВА
Res	et 0x0	000FFFF		0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue						De	scr	ipti	on																			
Α	W	SOPOWER									Ke	ер І	RAN	1 se	ecti	on	S0	of F	RAN	10 c	on c	or o	ff in	Sys	ten	n O	Νn	nod	le				
			On	1							On	1																					
В	W	S1POWER									Ke	ер	RAN	1 se	ecti	on	S1	of F	RAN	10 c	on c	or o	ff in	Sys	ten	n O	N n	nod	le				
			On	1							On	1																					
С	W	SORETENTION									Ke	ер	rete	ntio	on	on	RA	M s	ect	ion	S0	whe	ff in System O		n is	5							
											sw	itch	ned	off																			
			On	1							On	1												in System ON mode									
D	W	S1RETENTION									Ke	ер	rete	ntio	on	on	RA	M s	ect	ion	S1	whe	r off in System ON mode when RAM section is										
											sw	itch	ned	off							1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												
			On	1							On	1																					

18.9.14 RAM[0].POWERCLR

Address offset: 0x908

RAM0 power control clear register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		3	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																		D	С														В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	٧	alue	•						De	scr	ipti	on																			
Α	W	SOPOWER										Ke	ер І	RAN	VI se	ctio	on S	0 c	f R	ΑM	0 о	n o	r of	f in	Sys	ster	n O	Νn	nod	е				
			Off	1								Of	f																					
В	W	S1POWER										Ke	ер І	RAN	VI se	ctio	n S	51 c	f R	ΑM	0 о	n o	r of	f in	Sys	ster	n O	N n	nod	е				
			Off	1								Of	f																					
С	W	SORETENTION										Ke	ер	rete	n F	RAN	1 se	ectio	on S	50 v	whe	n R	RAN	1 se	ctio	n is	6							
												sw	escription eep RAM section S0 of RAM0 on or off in System ON ments eep RAM section S1 of RAM0 on or off in System ON ments eep RAM section S1 of RAM0 on or off in System ON ments eep retention on RAM section S0 when RAM section is witched off eep retention on RAM section S1 when RAM section is																					
			Off	1								Of	ep RAM section S0 of RAM0 on or off in System ON m f ep RAM section S1 of RAM0 on or off in System ON m f ep retention on RAM section S0 when RAM section is vitched off f																					
D	W	S1RETENTION										Ke	D C O O O O O O O O O O O O I I I I I I I																					
												sw	itch	ned	off																			



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C B A
Reset 0x0000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value	Description
	Off	1	Off

18.9.15 RAM[1].POWER

Address offset: 0x910

RAM1 power control register

Bit	numbe	er		31	30	29 2	28 2	27 2	26 2	5 2	4 23	3 22	2 21	20	19	18	17	16	15	14 :	13 1	2 11	10	9	8	7	5 5	5 4	3	2	1)
Id																	D	С													В	1
Res	et 0x0	000FFFF		0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	1	1	1 1	. 1	1	1	1	1	1 :	l 1	1	1	1	Ĺ
Id	RW	Field	Value Id	Va	lue						De	escr	ripti	on																		
Α	RW	SOPOWER									Ke	ер	RAN	VI se	ectio	on S	60 C)N c	or O	FF i	n Sy	sten	n ON	۱m	ode							
											В.			ion		اء ما			o+o		l wh	an C	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	+		مادد						
																					the		-			EIE	NII	UN.				
													AIVI S	ect	ions	S WI	II b	e O	FF I	n Sy	ster	n OF	ŀ m	ode	2.							
			Off	0							Of																					
			On	1							Or																					
В	RW	S1POWER									Ke	ep	RAN	VI se	ectio	on S	51 C)N c	or O	FF i	n Sy	sten	n ON	l m	ode.							
											R/	MA	sect	tion	s ar	e al	lwa	ys r	eta	ined	l wh	en C	ON, Ł	out	can	also	be					
											re	tair	ned	whe	en C	FF	dep	en	den	t or	the	set	tings	s in	S1R	ETE	NTI	ON.				
											Al	I RA	AM s	ect	ions	s wi	ill b	e O	FF i	n Sy	ster	n OF	Fm	ode	<u>.</u>							
			Off	0							Of	ff																				
			On	1							Or	n																				
С	RW	SORETENTION									Ke	ер	rete	enti	on c	on F	RAN	1 se	ctic	n S	0 wh	ien l	RAM	l se	ctio	n is	in C	FF				
			Off	0							Of	ff																				
			On	1							Or	n																				
D	RW	S1RETENTION											rete	entic	on c	on F	RAN	1 se	ctic	n S	1 wh	ien I	RAM	l se	ctio	n is	in C	FF				
			Off	0							Of		,,,,					,-		_												
			On	1							Or																					
				-							Oi																					

18.9.16 RAM[1].POWERSET

Address offset: 0x914

RAM1 power control set register

When read, this register will return the value of the POWER register.

Bit n	umbe	r		31	30	29	28	27	26 2	25 2	24	23 2	22 2	21 2	0 1	19 1	8 2	17 :	16	15	14 :	L3 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																		D	С													В	Α
Rese	t 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0 (0 (0	0 (0	0	0	1	1	1	1 1	L 1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	W	SOPOWER										Kee	p RA	٩M	sec	tio	n S	0 o	f RA	M:	1 or	or	off	in S	yste	m C)N	nod	le				
			On	1								On																					
В	W	S1POWER										Kee	p RA	AΜ	sec	tio	n S	1 o	f RA	RAM1 on or off in System ON mode RAM1 on or off in System ON mode section SO when RAM section is													
			On	1								On						17 16 15 14 13 12 11 10 9 8 7 6 5 4 D C 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 50 of RAM1 on or off in System ON mode RAM section S0 when RAM section is RAM section S1 when RAM section is															
С	W	SORETENTION										Kee	p re	ten	tio	n oı	n R	ΑM	l se	ctic	n S	0 w	hen	RA	M se	ecti	on i	s					
											:	swit	tche	d o	ff																		
			On	1								On																					
D	W	S1RETENTION										Kee	p re	ten	tio	n oı	n R	ΑM	l se	ctic	n S	1 w	hen	RA	M se	B A 1 1 1 1 1 1 1 1 1 1 1 ttem ON mode tem ON mode							
											:	swit	tche	d o	ff																		
			On	1								On																					

18.9.17 RAM[1].POWERCLR

Address offset: 0x918



RAM1 power control clear register

When read, this register will return the value of the POWER register.

Bitı	numbe	er		31	30 2	29 2	28 2	7 20	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id								7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 D C D O O O O O O O O O O O O 1 1 1 1 1 1 1							E	3 A																	
Res	et 0x0	0000FFFF		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 1
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																			
Α	W	SOPOWER									Κe	еер	RAN	∕l se	ect	ion	S0	of F	RAN	11 (on c	or o	ff in	Sys	ten	n O	N n	nod	e				
			Off	1							Of	ff																					
В	W	S1POWER									Κe	еер	RAN	∕l se	ect	ion	S1	of F	RAN	11 (on c	or o	ff in	Sys	ten	n Ol	N n	nod	e				
			Off	1							Of	ff																					
С	W	SORETENTION									Κe	eep	rete	enti	on	on	RA	M s	ecti	ion	S0	whe	en R	AM	se	ctio	n is	5					
											sv	vitc	hed	off																			
			Off	1							Of	ff																					
D	W	S1RETENTION									Ke	еер	rete	enti	on	on	RA	M s	ecti	ion	S1	whe	en R	AM	se	ctio	n is	;					
											sv	vitc	hed	off																			
			Off	1							Of	ff																					

18.9.18 RAM[2].POWER

Address offset: 0x920

RAM2 power control register

Bit	numbe	er		RAM sections are retained when OF All RAM sections of Off 1 On Keep RAM sections are retained when OF All RAM sections are retained when OF All RAM sections of Off 1 On Keep retention or Off 1 On Keep retention or Off 1 On Keep retention or Off				18	17	16	15	14	13 1	2 11	1 10	9	8	7	6	5 4	4 3	2	1	0									
Id						00000												D	С													В	Α
Res	et 0x0	000FFFF		0	0	0						0	0	0	0	0	0	0	0	1	1	1 :	l 1	1	1	1	1	1	1 :	1 1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	SOPOWER										Kee	рR	RAIV	1 se	ctio	n S	60 C)N	or C)FF i	in Sy	ster	n Ol	N m	ode							
												RAN	VI S	ecti	ons	s are	e al	lwa	vs r	eta	ine	d wh	en (ON.	but	can	also	b be	2				
																								_									
			Off	0								Off																					
			On	1								On																					
В	RW	S1POWER										Kee	рR	RAIV	1 se	ctio	n S	51 C)N c	or C)FF i	in Sy	ster	n Ol	N m	ode							
												RAN	Λs	ecti	ons	are	la د	lwa	vs r	eta	ine	d wh	en (NC	but	can	also	n he	2				
																														_			
			Off	0								Off									·												
			On	1								On																					
С	RW	SORETENTION										Kee	рr	ete	ntic	on o	n F	RAN	1 se	ctic	n S	0 wl	nen	RAN	1 se	ctio	n is	in (OFF				
			Off	0								Off																					
			On	1								On																					
D	RW	S1RETENTION										Kee	p r	ete	ntic	on o	n R	RAN	1 se	ctic	on S	1 wl	nen	RAN	1 se	ctio	n is	in (OFF				
			Off	0								Off																					
			On	1								On																					
			Keep RAM section S0 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTIO All RAM sections will be OFF in System OFF mode. Off On 1 On Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTIO All RAM sections will be OFF in System OFF mode. Off On 1 On Keep retention on RAM section S0 when RAM section is in OF OFF ON The Company of the Compa																														

18.9.19 RAM[2].POWERSET

Address offset: 0x924

RAM2 power control set register

When read, this register will return the value of the POWER register.

Bit	numb	er		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000FFFF		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 &$
Id	RW	Field	Value Id	Value	Description
Α	W	SOPOWER			Keep RAM section SO of RAM2 on or off in System ON mode
			On	1	On



Bit r	numbe	er		31	. 30	29	28 2	27 :	26 :	25 2	24 2	23 2	22 2	21 2	0 1	9 1	.8 1	.7 :	16 1	L5 1	L4 1	3 12	11	10	9	8	7	6	5 -	4 3	2	1	0
Id																		D	С													В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0 (0 () (0 (0	0	0	1	1 1	1	1	1	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Va	alue							Des	crip	tior	า																		
В	W	S1POWER									ŀ	Kee	p RA	٩M	sec	tio	n S:	L of	RA	M2	on	or c	ff in	Sys	ten	10 r	۱m	ode	è				
			On	1							(Эn																					
С	W	SORETENTION									ŀ	Kee	p re	ten	tio	n or	n R	٩M	sec	ctio	n SC	wh	en R	AM	sec	ction	ı is						
											5	wit	che	d o	ff																		
			On	1							(Эn	D C O O O O O O O O 1 1 1 scription ep RAM section S1 of RAM2 on o ep retention on RAM section S0 v itched off ep retention on RAM section S1 v itched off																				
D	W	S1RETENTION									ŀ																						
											5	O O O O O O O O O I I I I I I I I I ODESCRIPTION Ceep RAM section S1 of RAM2 on or off in System Con Ceep retention on RAM section S0 when RAM section S0 when RAM section S0 when RAM section S0 when RAM section S1 when RAM s2 w																					
			On	1							(Эn						O O 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1															

18.9.20 RAM[2].POWERCLR

Address offset: 0x928

RAM2 power control clear register

When read, this register will return the value of the POWER register.

Bit	numbe	er		31 3	0 29	28	27 2	26 2	5 24	1 23	22	21 2	20 1	19 1	8 1	7 1	6 1	5 1	4 13	12	11	10	9	8 7	' 6	5 5	5 4	3	2	1	0
Id															[) (В	Α
Re	et 0x0	000FFFF		0 (0	0	0	0 0	0	0	0	0	0	0 () (0) :	1 1	. 1	1	1	1	1	1 1	. 1	L 1	1 1	. 1	1	1	1
Id	RW	Field	Value Id	Valu	e					De	scri	ptio	n																		
Α	W	SOPOWER								Ke	ер Г	RAM	sec	ctio	n SC	of	RA	M2	on (or of	f in	Syst	em	ON	mo	ode					
			Off	1						Of	f																				
В	W	S1POWER								Ke	ер Ғ	RAM	sec	ctio	n S1	of	RA	M2	on o	or of	f in	Syst	em	ON	mo	ode					
			Off	1						Of	f																				
С	W	SORETENTION								Ke	ep r	eter	ntio	n or	n R/	M	sec	tior	S0	whe	n R	AM	sec	tion	is						
										SW	itch	ed o	ff																		
			Off	1						Of	f																				
D	W	S1RETENTION								Ke	ep r	eter	ntio	n or	n R/	M/	sec	tior	S1	whe	n R	AM	sec	tion	is						
										SW	itch	ed o	ff																		
			Off	1						Of	f																				

18.9.21 RAM[3].POWER

Address offset: 0x930

RAM3 power control register

Bit r	number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Res	et 0x0000FFFF		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 &$
Id	RW Field	Value Id	Value	Description
Α	RW SOPOWER			Keep RAM section SO ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in SORETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
В	RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in S1RETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
С	RW SORETENTION			Keep retention on RAM section SO when RAM section is in OFF
		Off	0	Off
		On	1	On



Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	3 12	11	10	9	8	7	6	5	4	3	2	1	C
Id																		D	С															В	Δ
Re	set 0x	0000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
D	RW	S1RETENTION										Ke	ep r	ete	ntio	on d	on I	RAI	√l s	ect	ion	S1	wh	en I	RAN	1 se	ctio	n i	in	OF	F				
			Off	0								Off	f																						
			On	1								On																							

18.9.22 RAM[3].POWERSET

Address offset: 0x934

RAM3 power control set register

When read, this register will return the value of the POWER register.

Bitı	numbe	er		31	30 :	29 :	28 2	27 2	26 2	5 2	24 2	3 22	2 21	20	19	18	17	16	15	14	13 :	12 1	.1 1	0 9	9 8	3 .	7	6 5	5 4	3	2	1 0
Id																	D	С														ВА
Res	et 0x0	000FFFF		0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0	1	1	1	1	1 1	L 1	1 :	ι :	1	1 :	1	1	1	1 1
ld	RW	Field	Value Id	Va	lue						C	esci	ripti	on																		
Α	W	SOPOWER									K	еер	RAN	∕l se	ectio	n S	60 c	f R	ΑM	10 8	n or	off	in S	yst	em	ON	l m	ode				
			On	1							C	n																				
В	W	S1POWER									K	еер	RAN	∕l se	ectio	on S	51 c	f R	ΑM	10 8	or	off	in S	yst	em	ON	l m	ode				
			On	1							C	n																				
С	W	SORETENTION									K	еер	rete	enti	on c	n F	RAN	1 se	ectio	on S	0 w	her	RA	Ms	ect	ion	ı is					
											S	witc	hed	off																		
			On	1							C	n																				
D	W	S1RETENTION									K	еер	rete	enti	on c	n F	RAN	1 se	ectio	on S	1 w	her	RA	Ms	ect	ion	ı is					
											S	witc	hed	off																		
			On	1							C	n																				

18.9.23 RAM[3].POWERCLR

Address offset: 0x938

RAM3 power control clear register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	1 30	29	28	27	26	25	24 2	23 2	22 2	21 2	0 1	19 1	18 :	17	16	15	14 1	3 1	2 1:	1 10	9	8	7	6	5	4 3	2	1	0
Id																		D	С													В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	1	1	1 1	l 1	1	1	1	1	1	1	1 :	. 1	1	1
Id	RW	Field	Value Id	Va	alue							Des	crip	otio	n																		
Α	W	SOPOWER									ŀ	(ee	рR	AM	sec	ctio	n S	0 о	f RA	MA	3 on	or (off i	n Sy	ster	n O	Νn	node	e				
			Off	1							(Off																					
В	W	S1POWER									ŀ	Keep	рR	AM	sec	ctio	n S	1 o	f RA	AM:	3 on	or (off i	n Sy	ster	n O	N n	node	е				
			Off	1							(Off																					
С	W	SORETENTION									ŀ	(ee	p re	eten	tio	n o	n R	ΑN	1 se	ctic	n S) wł	nen	RAN	∕l se	ctio	n is						
											5	wit	che	ed o	ff																		
			Off	1							(Off																					
D	W	S1RETENTION									ŀ	Kee	p re	eten	tio	n o	n R	ΑN	1 se	ctic	n S	L wł	nen	RAN	∕l se	ctio	n is						
											5	wit	che	ed o	ff																		
			Off	1							(Off																					

18.9.24 RAM[4].POWER

Address offset: 0x940

RAM4 power control register



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C
Reset 0x0000FFFF		0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW SOPOWER			Keep RAM section SO ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in SORETENTION.
			All RAM sections will be OFF in System OFF mode.
	Off	0	Off
	On	1	On
B RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in S1RETENTION.
			All RAM sections will be OFF in System OFF mode.
	Off	0	Off
	On	1	On
C RW SORETENTION			Keep retention on RAM section SO when RAM section is in OFF
	Off	0	Off
	On	1	On
D RW S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
	Off	0	Off
	On	1	On

18.9.25 RAM[4].POWERSET

Address offset: 0x944

RAM4 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30 2	9 2	28 27	7 2	6 25	24	23 2	22	21 2	0 1	9 1	8 1	17 1	16 1	L5 1	L4 1	3 1	2 11	1 10	9	8	7	6	5	4	3 2	1	. 0
Id																	D (С													В	Α
Res	et 0x0	000FFFF		0	0	0	0 0	0	0	0	0	0	0 ()	0 (0	0 (0	1	1 :	L 1	. 1	1	1	1	1	1	1	1	1 1	. 1	. 1
Id	RW	Field	Value Id	Va	lue						Des	cri	ptior	1																		
Α	W	SOPOWER									Kee	рR	RAM	sec	tior	n S(of O	RA	M4	on	or (off i	n Sy	ste	n O	Νn	nod	e				
			On	1							On																					
В	W	S1POWER									Kee	рR	RAM	sec	tior	n Si	1 of	RA	M4	on	or o	off i	n Sy	ste	n O	Νn	nod	е				
			On	1							On																					
С	W	SORETENTION									Kee	p r	eten	tio	n or	n R	ΑM	sec	ctio	n SC) wh	en	RAN	∕l se	ctic	n is	5					
											swit	tch	ed o	ff																		
			On	1							On																					
D	W	S1RETENTION									Kee	p r	eten	tio	n or	n R	AM	sec	ctio	n S1	wh	en	RAN	∕l se	ctic	n is	5					
											swit	tch	ed o	ff																		
			On	1							On																					

18.9.26 RAM[4].POWERCLR

Address offset: 0x948

RAM4 power control clear register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31 3	29	28	27 2	26 2	5 2	4 23	3 22	2 21	L 20	19	18	17	16	15	14	13	12 1	1 1	9	8	7	6	5	4	3	2 :	1 0
Id																D	С													ı	ВА
Res	et 0x0	0000FFFF		0 0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	1	1	1	1	L 1	. 1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Valu	е					D	esc	ript	ion																		
Α	W	SOPOWER								Ke	eep	RA	M s	ecti	on	SO c	of R	ΑM	4 o	n or	off	in S	yste	m C)N r	noc	le				
			Off	1						0	ff																				
В	W	S1POWER								K	eep	RA	M s	ecti	on	S1 c	of R	AM	4 o	n or	off	in S	yste	m C)N r	noc	le				



Bit	numbe	er		31	L 30	29	28	3 27	26	5 25	5 2	4 2	3 2	22	21	20	19	18	3 1	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 9	9 8	7	6	5	4	3	2	1	0
Id																			D	(В	Α
Res	et 0x0	0000FFFF		0	0	0	0	0	0	0	C) (0	0	0	0	0	0	0	0	1	. :	L :	L	1 :	ι :	L 1	L 1	. 1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	alue							D)es	cri	ptic	on																				
			Off	1								C	Off																							
С	W	SORETENTION										K	ee	p r	ete	nti	on	on	RA	M:	sec	tio	n SC) w	hen	RA	Ms	ect	ion	is						
												S	wit	tch	ed	off																				
			Off	1								C	Off																							
D	W	S1RETENTION										K	ee	p r	ete	nti	on	on	RA	M:	sec	tio	ո S1	w	hen	RA	Ms	ect	ion	is						
												S	wit	tch	ed	off																				
			Off	1								C	Off																							

18.9.27 RAM[5].POWER

Address offset: 0x950

RAM5 power control register

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	SOPOWER			Keep RAM section SO ON or OFF in System ON mode.
					RAM sections are always retained when ON, but can also be
					retained when OFF dependent on the settings in SORETENTION.
					All RAM sections will be OFF in System OFF mode.
			Off	0	Off
			On	1	On
В	RW	S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
					RAM sections are always retained when ON, but can also be
					retained when OFF dependent on the settings in S1RETENTION.
					All RAM sections will be OFF in System OFF mode.
			Off	0	Off
			On	1	On
С	RW	SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
			Off	0	Off
			On	1	On
D	RW	S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
			Off	0	Off
			On	1	On

18.9.28 RAM[5].POWERSET

Address offset: 0x954

RAM5 power control set register

When read, this register will return the value of the POWER register.

Bitı	numbe	er		3:	1 30	29	28	8 27	7 20	6 25	5 2	4 2	23 :	22	21	20	19	9 1	8 1	7 1	.6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																			[) (С															В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	(0	0	0	0	0	0	C) () (0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	V	alue	•						0	Des	cri	pti	on																					
Α	W	SOPOWER										K	(ee	p F	RAN	VI s	ect	ior	SC	of	RA	M	5 01	ı o	r of	f in	Sys	stei	n O	N r	noc	le					
			On	1								C	Ͻn																								
В	W	S1POWER										K	(ee	p F	RAN	VI s	ect	ior	S1	of	R/	M	01	10	r of	f in	Sys	ste	n O	N r	noc	le					
			On	1								C	Ͻn																								
С	W	SORETENTION										K	(ee	p r	ete	enti	ion	on	R/	١M	se	ctic	n S	0 v	vhe	n R	AN	1 se	ctic	n i	S						
												S	wit	tch	ed	off	f																				
			On	1								C	Ͻn																								



Bit r	numbe	r		3	1 30	29	28	8 2	7 26	5 25	5 24	4 2	3 2	2 2	1 2	0 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																			D	С															ВА
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0) (0 () (0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	٧	alu	е						D	esc	rip	tio	n																			
D	W	S1RETENTION										K	eep	re	ten	tio	n o	n R	ΑN	1 se	cti	on !	51 ۱	vhe	n R	ΑM	se	ctic	n is	5					
												S١	vit	che	d o	ff																			
			On	1								0	n																						

18.9.29 RAM[5].POWERCLR

Address offset: 0x958

RAM5 power control clear register

When read, this register will return the value of the POWER register.

numbe	er		31	30 2	29 :	28 2	27 2	26 2	25 2	24 2	3 2	2 2:	1 20	19	9 18	3 17	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
																D	(В	Α
et 0x0	0000FFFF		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0) 1	. 1	1	1	1	1	1	1	1	1	1	1	1 1	1	1
RW	Field	Value Id	Va	lue						0	esc	ript	ion																			
W	SOPOWER									k	Сеер	RA	M s	ect	ion	S0	of	RAN	1 15	on (or o	ff in	Sys	ten	n OI	۱m	node	e				
		Off	1							C	Off																					
W	S1POWER									k	Сеер	RA	M s	ect	ion	S 1	of	RAN	1 15	on (or o	ff in	Sys	ten	n OI	N m	node	е				
		Off	1							C	Off																					
W	SORETENTION									K	Сеер	ret	ent	ion	on	RA	M:	sect	ior	S0	wh	en R	AM	se	ctio	n is						
										S	wito	chec	d of	f																		
		Off	1							C	Off																					
W	S1RETENTION									K	Сеер	ret	ent	ion	on	RA	M:	sect	ior	S1	wh	en R	AM	se	ctio	n is						
										S	wito	chec	d of	f																		
		Off	1							C	Off																					
	et 0x0 RW W W	W S1POWER W SORETENTION	et 0x0000FFFF RW Field Value Id W SOPOWER Off W S1POWER Off W SORETENTION Off W S1RETENTION	et 0x0000FFFF 0 RW Field Value Id Va W SOPOWER Off 1 W S1POWER Off 1 W SORETENTION Off 1	et 0x0000FFFF 0 0 0 RW Field Value Id Value W SOPOWER Off 1 W S1POWER Off 1 W SORETENTION Off 1	et 0x0000FFF	et 0x0000FFFF	et 0x0000FFFF	et 0x00000FFFF	et 0x0000FFFF	et 0x0000FFFF	Note	No No No No No No No No	No No No No No No No No	Note Note	## Ox0000FFFF O O O O O O O O O	et 0x0000FFFF	Note	Note	RW Field Value Id Value Valu	Note Note	RW Field Value Id Value Valu	RW Field Value Id Value Valu	et 0x0000FFFF 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	et 0x0000FFFF 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	et 0x0000FFFF 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	et 0x0000FFFF 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	et 0x0000FFFF 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	The control of the co	END ON THE CONTROL OF STREET THE CONTROL OF	END ON	Red

18.9.30 RAM[6].POWER

Address offset: 0x960

RAM6 power control register

D.:			24 20 20 20 27 27	25 24 22 22 24 20 40 40 47 46 45 44 42 42 44 40 0 0 7 6 5 4 2 2
	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Res	et 0x0000FFFF		0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
Id	RW Field	Value Id	Value	Description
Α	RW SOPOWER			Keep RAM section SO ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in SORETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
В	RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in S1RETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
С	RW SORETENTION			Keep retention on RAM section SO when RAM section is in OFF
		Off	0	Off
		On	1	On
D	RW S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
		Off	0	Off
		On	1	On



18.9.31 RAM[6].POWERSET

Address offset: 0x964

RAM6 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30	29	28 2	7 2	6 2	5 24	1 2	3 22	21	20	19	9 18	3 1	7 10	5 15	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																	D) C														В	3 A
Res	et OxO	0000FFFF		0	0	0	0 (0 (0 0	0	C	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 :	l 1	1
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																			
Α	W	SOPOWER									K	еер	RAN	VI se	ect	ion	S0	of	RAN	1 6	on d	or o	ff ir	Sys	ten	n Ol	N m	nod	e				
			On	1							0	n																					
В	W	S1POWER									K	еер	RAN	VI se	ect	ion	S1	of	RAN	16	on d	or o	ff ir	Sys	ten	n O	N m	nod	e				
			On	1							0	n																					
С	W	SORETENTION									K	еер	rete	enti	on	on	RA	M	ect	ion	S0	wh	en f	RAM	se	ctio	n is						
											S١	witc	hed	off	;																		
			On	1							0	n																					
D	W	S1RETENTION									K	еер	rete	enti	on	on	RA	M	ect	ion	S 1	wh	en f	RAM	se	ctio	n is						
											S١	witc	hed	off																			
			On	1							0	n																					

18.9.32 RAM[6].POWERCLR

Address offset: 0x968

RAM6 power control clear register

When read, this register will return the value of the POWER register.

Bitı	numbe	er		31	30 2	9 :	28 2	27 2	26 2	5 2	24	23 2	2 2	21 2	0 1	19 1	.8	17	16	15	14	13	L2 1	111	.0 9) ;	3 7	7 (6 !	5	4 3	3 2	2 1	. 0
Id																		D	С														В	3 A
Res	et 0x0	000FFFF		0	0	0	0	0	0 ()	0	0 (0	0 ()	0 (0	0	0	1	1	1	1	1 :	1 1	1	1 :	ι :	1	1	1 :	1 1	l 1	. 1
Id	RW	Field	Value Id	Va	lue							Desc	rip	tior	1																			
Α	W	SOPOWER										Keep	R C	AM	seo	ctio	n S	0 о	f R	AΜ	o a	n or	off	in S	yste	em	ON	m	ode	:				
			Off	1								Off																						
В	W	S1POWER										Keep	R C	AM	sec	ctio	n S	1 o	f R	ΑM	o 0	or	off	in S	yste	em	ON	m	ode	:				
			Off	1								Off																						
С	W	SORETENTION										Keep	re	eten	tio	n or	n R	ΑN	1 se	ctio	on S	0 w	her	RA	M s	ec	tion	is						
												swite	che	ed o	ff																			
			Off	1								Off																						
D	W	S1RETENTION										Keep	re	eten	tio	n or	n R	ΑN	1 se	ctio	on S	1 w	her	RA	M s	ec	tion	is						
												swite	che	ed o	ff																			
			Off	1								Off																						

18.9.33 RAM[7].POWER

Address offset: 0x970

RAM7 power control register

Bit number		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 :	17	16 :	15 1	L4 1	.3 1	2 1:	. 10	9	8	7	6	5	4	3 2	2 1	1 0
Id																D	С													E	ВА
Reset 0x0000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1 :	1	1	1	1	1	1	1	1	1 1	L 1	1 1
Id RW Field	Value Id	Va	lue							Des	scri	ptic	n																		
A RW SOPOWER										Kee	ep F	RAIV	l se	ctic	n S	0 0	N o	r O	FF i	n Sy	ster	10 n	l m	ode							
										RAI	M s	ecti	ons	are	e al	way	/s re	etai	nec	wh	en (ON,	out	can	als	o b	e				
										reta	aine	ed v	vhe	n O	FF (dep	end	len	t on	the	set	ting	s in	SOR	ETI	ENT	101	۱.			
										ΑII	RAI	M se	ecti	ons	wil	l be	OF	Fir	ı Sy	stei	n Ol	Fm	ode	<u>.</u>							
	Off	0								Off	f																				
	On	1								On																					
B RW S1POWER										Kee	ep F	RAIV	l se	ctic	n S	1 0	N o	r O	FF i	n Sy	ster	10 n	N m	ode							



Bit r	number			31	30 2	9 :	28 2	7 2	6 25	24	23 22	212	0 1	19 18	3 1	7 16	15	14	13 1	2 11	10	9	8	7	6	5	4 3	3 2	1	0
Id															C) С													В	Α
Res	et 0x0000FF	FF		0	0	0	0 0) (0 0	0	0 0	0 0)	0 0	C	0	1	1	1 1	. 1	1	1	1	1	1	1	1 :	l 1	1	1
Id	RW Field		Value Id	Va	lue						Desci	riptior	1																	
											RAM	sectio	ns	are	alw	ays	reta	ine	d wh	en C	N, b	out	can	als	o be	е				
											retair	ned wl	her	n OF	F d	epei	nde	nt o	n the	set	ings	in	S1R	ETE	NT	ION	١.			
											All RA	AM sed	ctic	ons v	vill	be 0	OFF	in S	/ster	n OF	Fm	ode	2.							
			Off	0							Off																			
			On	1							On																			
С	RW SORE	TENTION									Keep	reten	tio	n on	RΑ	M s	ecti	on S	0 wh	en f	RAM	se	ctio	n is	in (OFF				
			Off	0							Off																			
			On	1							On																			
D	RW S1RE	TENTION									Keep	reten	tio	n on	RΑ	M s	ecti	on S	1 wh	ien f	RAM	se	ctio	n is	in (OFF				
			Off	0							Off																			
			On	1							On																			

18.9.34 RAM[7].POWERSET

Address offset: 0x974

RAM7 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	. 30	29	28 2	27 :	26 2	25 2	24 2	3 22	21	20	19	18	17	16	15	14	13 1	12 1	.1 1	0 9	8 (7	6	5	4	3	2	1 0
Id																	D	С														ВА
Res	et 0x0	000FFFF		0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	1	1	1	1 :	1 1	L 1	. 1	. 1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																		
Α	W	SOPOWER									K	еер	RAN	VI se	ecti	on S	50 c	f R	ΑM	7 or	or	off	in S	yste	em	ON	mo	de				
			On	1							C	n																				
В	W	S1POWER									K	еер	RAN	VI se	ecti	on S	51 c	f R	AM	7 or	or	off	in S	yste	em	ON	mo	de				
			On	1							C	n																				
С	W	SORETENTION									K	еер	rete	enti	on (on f	RAN	1 se	ectio	on S	0 w	hen	RA	M s	ect	ion	is					
											S	witc	hed	off																		
			On	1							C	n																				
D	W	S1RETENTION									K	еер	rete	enti	on (on f	RAN	1 se	ectio	on S	1 w	hen	RA	M s	ect	ion	is					
											S	witc	hed	off																		
			On	1							C	n																				

18.9.35 RAM[7].POWERCLR

Address offset: 0x978

RAM7 power control clear register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30	29 :	28 2	7 2	26 2	5 2	4 2	3 22	21	20	19	18	17	16	15	14	13	12 :	L1 1	.0 9	9	8	7 6	5	4	3	2	1 0
Id																	D	С														ВА
Rese	et 0x0	0000FFFF		0	0	0	0 (0	0 0	0)	0 0	0	0	0	0	0	0	1	1	1	1	1	1 :	1	1	1 1	. 1	. 1	1	1	1 1
Id	RW	Field	Value Id	Va	lue						0	escr	ipti	on																		
Α	W	SOPOWER									k	Сеер	RAN	∕l se	ecti	on	S0 (of R	AM	7 o	n or	off	in S	syst	em	0	l mc	de				
			Off	1							C	Off																				
В	W	S1POWER									K	Сеер	RAN	∕l se	ecti	on	S1 (of R	AM	7 o	n or	off	in S	Syst	em	0	l mo	de				
			Off	1							C	Off																				
С	W	SORETENTION									K	Сеер	rete	enti	on	on	RAI	VI s	ecti	on S	0 w	hei	n RA	M:	sec	tior	is					
											S	witc	hed	off																		
			Off	1							C	Off																				
D	W	S1RETENTION									K	Сеер	rete	enti	on	on	RAI	VI s	ecti	on S	1 w	hei	n RA	M:	sec	tior	is					
											S	witc	hed	off																		
			Off	1							C	Off																				



18.10 Electrical Specification

18.10.1 Current consumption, sleep

Symbol	Description	Min.	Тур.	Max.	Units
I _{OFF}	System OFF current, no RAM retention		0.7		μΑ
I _{ON}	System ON base current, no RAM retention		1.2		μΑ
I _{RAM}	Additional RAM retention current per 4 KB RAM section		20		nA

18.10.2 Device startup times

Symbol	Description	Min.	Тур.	Max.	Units
t _{POR}	Time in Power on Reset after VDD reaches 1.7 V for all supply				
	voltages and temperatures. Dependent on supply rise time. $^{\rm 8}$				
t _{POR,10us}	VDD rise time 10us		1		ms
t _{POR,10ms}	VDD rise time 10ms		9		ms
t _{POR,60ms}	VDD rise time 60ms		23		ms
t_{PINR}	If a GPIO pin is configured as reset, the maximum time taken				
	to pull up the pin and release reset after power on reset.				
	Dependent on the pin capacitive load (C) ⁹ : t=5RC, R = 13kOhm				
t _{PINR,500nF}	C = 500nF			32.5	ms
t _{PINR,10uF}	C = 10uF			650	ms
t _{R2ON}	Time from reset to ON (CPU execute)				
$t_{R2ON,NOTCONF} \\$	If reset pin not configured	tPOR			ms
t _{R2ON,CONF}	If reset pin configured	tPOR +			ms
		tPINR			
t _{OFF2ON}	Time from OFF to CPU execute		16.5		μs
t _{IDLE2CPU}	Time from IDLE to CPU execute		3.0		μs
t _{EVTSET,CL1}	Time from HW event to PPI event in Constant Latency System		0.0625		μs
	ON mode				
t _{EVTSET,CL0}	Time from HW event to PPI event in Low Power System ON		0.0625		μs
	mode				

18.10.3 Power fail comparator

μΑ
V
%
mV
V
V

A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

⁹ To decrease maximum time a device could hold in reset, a strong external pullup resistor can be used.

To save power, POF will not operate nor consume in System OFF, or while HFCLK is not running, even if left enabled by software



19 CLOCK — Clock control

The clock control system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

Listed here are the main features for CLOCK:

- · 64 MHz on-chip oscillator
- 64 MHz crystal oscillator, using external 32 MHz crystal
- 32.768 kHz +/-250 ppm RC oscillator
- · 32.768 kHz crystal oscillator
- · 32.768 kHz synthesized from high frequency oscillator
- · Firmware (FW) override control of oscillator activity for low latency start up
- · Automatic oscillator and clock control, and distribution for ultra-low power

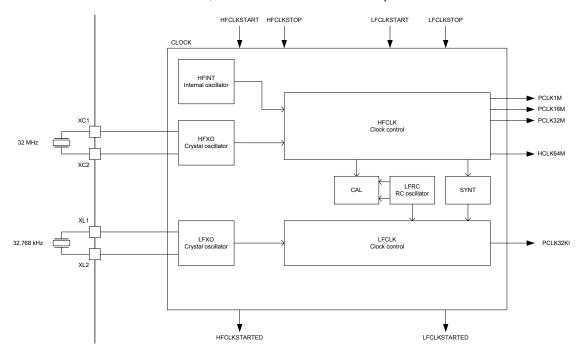


Figure 16: Clock control

19.1 HFCLK clock controller

The HFCLK clock controller provides the following clocks to the system.

- HCLK64M: 64 MHz CPU clock
- PCLK1M: 1 MHz peripheral clock
- · PCLK16M: 16 MHz peripheral clock
- PCLK32M: 32 MHz peripheral clock

The HFCLK controller supports the following high frequency clock (HFCLK) sources:

- 64 MHz internal oscillator (HFINT)
- 64 MHz crystal oscillator (HFXO)

For illustration, see Figure 16: Clock control on page 98.



When the system requests one or more clocks from the HFCLK controller, the HFCLK controller will automatically provide them. If the system does not request any clocks provided by the HFCLK controller, the controller will enter a power saving mode.

These clocks are only available when the system is in ON mode. When the system enters ON mode, the internal oscillator (HFINT) clock source will automatically start to be able to provide the required HFCLK clock(s) for the system.

The HFINT will be used when HFCLK is requested and HFXO has not been started. The HFXO is started by triggering the HFCLKSTART task and stopped using the HFCLKSTOP task. A HFCLKSTARTED event will be generated when the HFXO has started and its frequency is stable.

The HFXO must be running to use the RADIO, NFC module or the calibration mechanism associated with the 32.768 kHz RC oscillator.

19.1.1 64 MHz crystal oscillator (HFXO)

The 64 MHz crystal oscillator (HFXO) is controlled by a 32 MHz external crystal

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet.

Figure 17: Circuit diagram of the 64 MHz crystal oscillator on page 99 shows how the 32 MHz crystal is connected to the 64 MHz crystal oscillator.

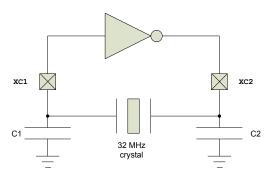


Figure 17: Circuit diagram of the 64 MHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

 $C2' = C2 + C_{pcb2} + C_{pin}$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. For more information, see *Reference circuitry* on page 539. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the xc1 and xc2 pins. See table *64 MHz crystal oscillator (HFXO)* on page 105. The load capacitors C1 and C2 should have the same value.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance, and drive level must comply with the specifications in table 64 MHz crystal oscillator (HFXO) on page 105. It is recommended to use a crystal with lower than maximum load capacitance and/or shunt capacitance. A low load capacitance will reduce both start up time and current consumption.



19.2 LFCLK clock controller

The system supports several low frequency clock sources.

As illustrated in *Figure 16: Clock control* on page 98, the system supports the following low frequency clock sources:

- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz crystal oscillator (LFXO)
- 32.768 kHz synthesized from HFCLK (LFSYNT)

The LFCLK clock controller and all of the LFCLK clock sources are always switched off when in OFF mode.

The LFCLK clock is started by first selecting the preferred clock source in register *LFCLKSRC* on page 104 and then triggering the LFCLKSTART task. If the LFXO is selected as the clock source, the LFCLK will initially start running from the 32.768 kHz LFRC while the LFXO is starting up and automatically switch to using the LFXO once this oscillator is running. The LFCLKSTARTED event will be generated when the LFXO has been started.

The LFCLK clock is stopped by triggering the LFCLKSTOP task.

It is not allowed to write to register *LFCLKSRC* on page 104 when the LFCLK is running.

A LFCLKSTOP task will stop the LFCLK oscillator. However, the LFCLKSTOP task can only be triggered after the STATE field in register *LFCLKSTAT* on page 104 indicates a 'LFCLK running' state.

The synthesized 32.768 kHz clock depends on the HFCLK to run. If high accuracy is required for the LFCLK running off the synthesized 32.768 kHz clock, the HFCLK must be generated from the HFCLK crystal oscillator.

19.2.1 32.768 kHz RC oscillator (LFRC)

The default source of the low frequency clock (LFCLK) is the 32.768 kHz RC oscillator (LFRC).

The LFRC frequency will be affected by variation in temperature. The LFRC oscillator can be calibrated to improve accuracy by using the HFXO as a reference oscillator during calibration. See Table *Low frequency RC oscillator (LFRC)* on page 106 for details on the default and calibrated accuracy of the LFRC oscillator. The LFRC oscillator does not require additional external components.

19.2.2 Calibrating the 32.768 kHz RC oscillator

After the 32.768 kHz RC oscillator is started and running, it can be calibrated by triggering the CAL task. In this case, the HFCLK will be temporarily switched on and used as a reference.

A DONE event will be generated when calibration has finished. The calibration mechanism will only work as long as HFCLK is generated from the HFCLK crystal oscillator, it is therefore necessary to explicitly start this crystal oscillator before calibration can be started, see HFCLKSTART task.

19.2.3 Calibration timer

The calibration timer can be used to time the calibration interval of the 32.768 kHz RC oscillator.

The calibration timer is started by triggering the CTSTART task and stopped by triggering the CTSTOP task. The calibration timer will always start counting down from the value specified in CTIV and generate a CTTO timeout event when it reaches 0. The Calibration timer will stop by itself when it reaches 0.

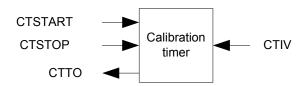


Figure 18: Calibration timer



Due to limitations in the calibration timer, only one task related to calibration, that is, CAL, CTSTART and CTSTOP, can be triggered for every period of LFCLK.

19.2.4 32.768 kHz crystal oscillator (LFXO)

For higher LFCLK accuracy (when better than +/- 250 ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used.

The 32.768 kHz crystal oscillator requires an external quartz crystal to be connected to the xl1 and xl2 pins in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet, see *Low frequency crystal oscillator (LFXO)* on page 106. The xl1 and xl2 share pins with the GPIO.

Figure 19: Circuit diagram of the 32.768 kHz crystal oscillator on page 101 shows LFXO circuitry.

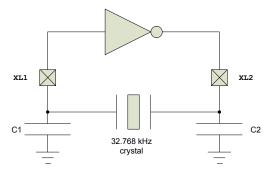


Figure 19: Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

 $C2' = C2 + C_{pcb2} + C_{pin}$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. For more information, see *Reference circuitry* on page 539. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the XC1 and XC2 pins. The load capacitors C1 and C2 should have the same value.

19.2.5 32.768 kHz synthesized from HFCLK (LFSYNT)

LFCLK can also be synthesized from the HFCLK clock source. The accuracy of LFCLK will then be the accuracy of the HFCLK.

Using the LFSYNT clock avoids the requirement for a 32.768 kHz crystal, but increases average power consumption as the HFCLK will need to be requested in the system.

19.3 Registers

Table 21: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40000000	CLOCK	CLOCK	Clock control		



Table 22: Register Overview

Register	Offset	Description
TASKS_HFCLKSTART	0x000	Start HFCLK crystal oscillator
TASKS_HFCLKSTOP	0x004	Stop HFCLK crystal oscillator
TASKS_LFCLKSTART	0x008	Start LFCLK source
TASKS_LFCLKSTOP	0x00C	Stop LFCLK source
TASKS_CAL	0x010	Start calibration of LFRC oscillator
TASKS_CTSTART	0x014	Start calibration timer
TASKS_CTSTOP	0x018	Stop calibration timer
EVENTS_HFCLKSTARTED	0x100	HFCLK oscillator started
EVENTS_LFCLKSTARTED	0x104	LFCLK started
EVENTS_DONE	0x10C	Calibration of LFCLK RC oscillator complete event
EVENTS_CTTO	0x110	Calibration timer timeout
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
HFCLKRUN	0x408	Status indicating that HFCLKSTART task has been triggered
HFCLKSTAT	0x40C	HFCLK status
LFCLKRUN	0x414	Status indicating that LFCLKSTART task has been triggered
LFCLKSTAT	0x418	LFCLK status
LFCLKSRCCOPY	0x41C	Copy of LFCLKSRC register, set when LFCLKSTART task was triggered
LFCLKSRC	0x518	Clock source for the LFCLK
CTIV	0x538	Calibration timer interval
		(retained register, same reset behaviour as RESETREAS)
TRACECONFIG	0x55C	Clocking options for the Trace Port debug interface

19.3.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit I	numbe	r		31	. 30	29	28 2	27 2	26 2	25 2	24 2	23	22	21	20 :	19	18	17	16	15	14	13	12	11 1	0 9	9 (7	6	5	4 D	_	_	1 0 B A
	et OxO	0000000		0	0	0	0	0	0	0	0	n	٥	0	0	n	٥	0	0	0	0	0	n	0 (. (. (0	0	0		0		0 O
Id		Field	Value Id		ilue			Ĭ		•			scri				Ĭ		Ĭ	Ť	Ť							Ŭ	Ŭ	Ŭ			
Α	RW	HFCLKSTARTED									١	۷r	rite '	1' t	o Eı	nab	le i	nte	rru	pt f	or I	HFC	LKS	TAR	TEC	ev	ent						
												See	e <i>EV</i>	'FN'	TS	HFC	'IK	STA	RTI	FD													
			Set	1									able		.5			J . , .															
			Disabled	0									ad: [able	d																	
			Enabled	1							F	Rea	ad: E	Ena	ble	d																	
В	RW	LFCLKSTARTED									١	Wr	rite '	1' t	o Eı	nab	le i	nte	rru	pt f	or l	-FCI	.KS	ΓAR	ΓED	eve	ent						
											9	See	e <i>EV</i>	'EN'	TS I	LFC	LKS	TA	RTE	D													
			Set	1									able																				
			Disabled	0							F	Rea	ad: [Disa	able	d																	
			Enabled	1							F	Rea	ad: E	Ena	ble	d																	
С	RW	DONE									١	۷r	rite '	1' t	o Eı	nab	le i	nte	rru	pt f	or I	100	IE e	ven	t								
											5	See	e <i>EV</i>	'EN	TS I	DOI	NE																
			Set	1									able		_																		
			Disabled	0							F	Rea	ad: [Disa	able	d																	
			Enabled	1							F	Rea	ad: E	Ena	ble	b																	
D	RW	стто									١	۷r	rite '	1' t	o Eı	nab	le i	nte	rru	pt f	or (CTT	O e	vent									
											5	See	e <i>EV</i>	'EN	TS (СТТ	0																
			Set	1									able		Ī																		
			Disabled	0							F	Rea	ad: [Disa	able	d																	
			Enabled	1							F	Rea	ad: E	Ena	ble	t																	



19.3.2 INTENCLR

Address offset: 0x308 Disable interrupt

Bit r	iumbe	er		31	30 2	29 2	28 27	7 26	25	24 2	23 2	22 21	1 2	0 19	18	3 17	7 16	15	5 14	13	12	11	10	9	8	7	6 5	5 4	3	2	1	0
Id																												0) С		В	Α
Res	et 0x0	0000000		0	0 (0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0
Id	RW	Field	Value Id	Va	lue						Des	cript	ion	1																		
Α	RW	HFCLKSTARTED								١	Wri	te '1'	' to	Disa	able	e in	terr	upt	t for	HF	CLK	STA	RTE	ED 6	ever	nt						
										9	See	EVE	NTS	S_HI	FCLI	KST	AR	TED)													
			Clear	1						[Disa	able																				
			Disabled	0						F	Rea	ıd: Di	sab	oled																		
			Enabled	1						F	Rea	ıd: En	nab	led																		
В	RW	LFCLKSTARTED								١	Wri	te '1'	' to	Disa	able	e in	terr	upt	t for	LF	CLK	STA	RTE	D e	ven	t						
										9	See	EVE	NTS	S_LF	CLK	ST	ART	ED														
			Clear	1						[Disa	able																				
			Disabled	0						F	Rea	ıd: Di	sab	oled																		
			Enabled	1						F	Rea	ıd: En	nab	led																		
С	RW	DONE								١	Wri	te '1'	' to	Disa	able	e in	terr	upt	t for	DC	NE	eve	nt									
										9	See	EVE	NTS	S_D	ONE																	
			Clear	1						[Disa	able																				
			Disabled	0						F	Rea	ıd: Di	sab	oled																		
			Enabled	1						F	Rea	id: En	nab	led																		
D	RW	СТТО								١	Wri	te '1'	' to	Dis	able	e in	terr	upt	t for	CT	то	eve	nt									
										9	See	EVE	NTS	s_ <i>C</i> 1	то																	
			Clear	1						[Disa	able																				
			Disabled	0						F	Rea	ıd: Di	sab	oled																		
			Enabled	1						F	Rea	ıd: En	nab	led																		

19.3.3 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

Bit n	umbe	r		33	1 30	29	28	27	26	25	24	23	22 2	21 2	20 :	19 :	18 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 ()
Id																																		A	4
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 ()
Id	RW	Field	Value Id	V	alue)						De	scrip	tio	n																				
Α	R	STATUS										HF	CLKS	TAI	RT 1	task	tri	gge	rec	d or	no	t													
			NotTriggered	0								Tas	k no	ot tr	rigg	ere	d																		
			Triggered	1								Tas	k tri	gge	erec	t																			

19.3.4 HFCLKSTAT

Address offset: 0x40C

HFCLK status

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	5 15	5 14	13	3 12	11	. 10	9	8	7	6	5	4	3	2	1 0
Id																			В															Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	llue							De	scr	ipti	on																			
Α	R	SRC										So	urc	e of	f HF	CLI	<																	
			RC	0								64	MI	Hz i	nte	rna	los	cill	ato	r (F	IFIN	IT)												
			Xtal	1								64	МІ	Hz c	rys	tal	osc	illa	tor	(HF	XO)												
В	R	STATE										HF	CL	〈 sta	ate																			
			NotRunning	0								HF	CL	(nc	t ru	ınn	ing																	
			Running	1								HF	CL	(ru	nni	ng																		



19.3.5 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

Bitı	numb	er		33	1 30	29	28	3 27	7 26	25	5 24	23	22	21	20	19	18	17	16	15	14	13 :	L2 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																																	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	2						De	scr	ipti	on																		
Α	R	STATUS										LFC	CLK	STA	RT	tas	k tr	igge	erec	d or	not	:											
			NotTriggered	0								Tas	sk r	not	trig	ger	ed																
			Triggered	1								Tas	sk t	rigg	gere	d																	

19.3.6 LFCLKSTAT

Address offset: 0x418

LFCLK status

Bit	numbe	er		31 3	0 29	28	3 27	26 2	5 2	24 2	3 2	2 21	20	19	18	17	16	15 1	L4 1	3 12	2 11	10	9	8 7	' E	5	4	3	2	1 0
Id																	В													А А
Res	et 0x0	0000000		0 (0	0	0	0 (0	0 (0 (0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	e					D	eso	cript	ion																	
Α	R	SRC								S	our	rce o	f LF	CLK																
			RC	0						3	2.7	'68 k	Hz I	RC o	scil	lato	r													
			Xtal	1						3	2.7	'68 k	Hz	cryst	tal	oscil	lato	or												
			Synth	2						3	2.7	'68 k	Hz s	ynt	hes	ized	fro	m F	HFC	_K										
В	R	STATE								L	FCL	K sta	ate																	
			NotRunning	0						L	FCL	K nc	t ru	ınniı	ng															
			Running	1						L	FCL	K ru	nniı	ng																

19.3.7 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set when LFCLKSTART task was triggered

Bi	t nı	umbe	r		31	30 2	29 2	28 2	27 :	26	25	24	23	22	21	20	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id																																		A	A A
R	ese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0
Id		RW	Field	Value Id	Val	ue							Des	cri	ptic	n																			
Α		R	SRC										Clo	ck s	our	ce																			
				RC	0								32.	768	kH	z R	C os	cill	lato	or															
				Xtal	1								32.	768	kH	z cr	yst	al c	sci	llat	or														
				Synth	2								32.	768	kH	z sy	nth	nesi	ized	d fr	om	HF	CLK												

19.3.8 LFCLKSRC

Address offset: 0x518

Clock source for the LFCLK

Bit	t nı	ımbe	r		31 30 29 28 27	5 24 23 22 21 20 19	18 17 16	5 15 :	14 13 1	2 11 1	.0 9	8	7	6	5 4	1 3	2	1 0
Id																		A A
Re	set	0x0	0000000		0 0 0 0 0	0 0 0 0 0 0	0 0 0	0	0 0	0 0	0 0	0	0	0	0 (0	0	0 0
Id		RW	Field	Value Id	Value	Description												
Α		RW	SRC			Clock source												
				RC	0	32.768 kHz RC o	scillator											
				Xtal	1	32.768 kHz cryst	al oscilla	tor										
				Synth	2	32.768 kHz synth	nesized f	rom l	HFCLK									



19.3.9 CTIV

Address offset: 0x538

Calibration timer interval

(retained register, same reset behaviour as RESETREAS)

Bit r	numbe	er		31 3	30 29	28	27 2	6 2	25 24	4 23	3 22	21	20 1	9 1	8 17	16	15 :	l4 13	3 12	11	10 9	8	7	6	5	4	3 2	1	0
Id																								Α	Α	A	4 A	Α	Α
Res	et 0x0	0000000		0	0 0	0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0 0	0	0	0 0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	ıe					D	escri	ptic	n																
Α	RW	CTIV								C	alibra	atio	n tim	er i	nter	val i	n m	ultip	le of	0.2	sec	onc	ls. R	ang	e:				
										0.	25 s	ecor	nds t	o 3:	1.75	sec	ond:	S.											

19.3.10 TRACECONFIG

Address offset: 0x55C

Clocking options for the Trace Port debug interface

This register is a retained register. Reset behavior is the same as debug components.

Bit r	numbe	r		31	30 29	9 28	3 27	26	25 2	4 23	22	21 2	0 1	L9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3 2	1	0
Id															- 1	3 E	3													Α	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0 0	0	0	0 (0	0 0) (0) () (0) (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue					De	scri	ptio	n																		
Α	RW	TRACEPORTSPEED								Sp	eed	of T	rac	e Po	rt (cloc	k. N	lot	e th	at t	he '	TRA	CEC	LK p	oin '	will					
										ou	tput	t this	clo	ock o	ivit	ded	by	tw	0.												
			32MHz	0						32	МН	lz Tra	ace	Por	t cl	ock	(TF	RAC	ECL	K =	16	МН	z)								
			16MHz	1						16	МН	lz Tra	ace	Por	t cl	ock	(TF	RAC	ECL	K =	8 N	ИHz)								
			8MHz	2						8 N	ЛHz	Trac	e F	ort	clo	ck (TRA	ACE	CLK	= 4	M	Hz)									
			4MHz	3						4 N	ЛHz	Trac	e F	ort	clo	ck (TRA	ACE	CLK	= 2	M	Hz)									
В	RW	TRACEMUX								Pin	mı	ıltipl	exi	ng o	f tı	ace	sig	na	s.												
			GPIO	0						GP	IOs	mult	tipl	exec	o b	nto	all	tra	се-р	ins											
			Serial	1						SW	/ 0 n	nulti	ple	xed	on	to P	0.1	8,	GPIC) m	ulti	ple	ĸed	ont	o ot	her	•				
										tra	ce p	oins																			
			Parallel	2						TR.	ACE	CLK	and	d TR	AC	EDA	TA	mι	lltip	lex	ed c	ntc	P0.	20,	P0.	18,					
										P0	16,	P0.1	.5 a	and I	P0.	14.															

19.4 Electrical Specification

19.4.1 64 MHz internal oscillator (HFINT)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFINT}	Nominal output frequency		64		MHz
f _{TOL_HFINT}	Frequency tolerance		<±1.5	<±6	%
I _{HFINT}	Run current		60		μΑ
I _{START_HFINT}	Average startup current		I_HFINT		μΑ
t _{START_HFINT}	Startup time		3		us

19.4.2 64 MHz crystal oscillator (HFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFXO}	Nominal output frequency		64		MHz
f _{XTAL_HFXO}	External crystal frequency		32		MHz
f _{TOL_HFXO}	Frequency tolerance requirement for 2.4 GHz proprietary radio			±60	ppm
	applications				
f _{TOL_HFXO_BLE}	Frequency tolerance requirement, Bluetooth low energy			±40	ppm
	applications				



Symbol	Description	Min.	Тур.	Max.	Units
C_{L_HFXO}	Load capacitance			12	pF
C _{0_HFXO}	Shunt capacitance			7	pF
R _{S_HFXO_7PF}	Equivalent series resistance C0 = 7 pF			60	ohm
R _{S_HFXO_5PF}	Equivalent series resistance C0 = 5 pF			80	ohm
R _{S_HFXO_3PF}	Equivalent series resistance C0 = 3 pF			100	ohm
P _{D_HFXO}	Drive level			100	uW
C _{PIN_HFXO}	Input capacitance XC1 and XC2		4		pF
I _{STBY_X32M}	Core standby current ¹¹		50		μΑ
I _{HFXO}	Run current		250		μΑ
I _{START_HFXO}	Average startup current, first 1 ms		0.4		mA
t _{START_HFXO}	Startup time		0.36		ms

19.4.3 Low frequency crystal oscillator (LFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFXO}	Crystal frequency		32.768		kHz
f _{TOL_LFXO_BLE}	Frequency tolerance requirement for BLE stack			±250 ¹²	ppm
f _{TOL_LFXO_ANT}	Frequency tolerance requirement for ANT stack			±50	ppm
C _{L_LFXO}	Load capacitance			12.5	pF
C _{0_LFXO}	Shunt capacitance			2	pF
R _{S_LFXO}	Equivalent series resistance			100	kohm
P_{D_LFXO}	Drive level			1	uW
C _{pin}	Input capacitance on XL1 and XL2 pads		4		pF
I _{LFXO}	Run current for 32.768 kHz crystal oscillator		0.25		μΑ
t _{START_LFXO}	Startup time for 32.768 kHz crystal oscillator		0.25		S

19.4.4 Low frequency RC oscillator (LFRC)

Symbol	Description	Min.	Тур.	Max.	Units
f_{NOM_LFRC}	Nominal frequency		32.768		kHz
f _{TOL_LFRC}	Frequency tolerance			±2	%
f _{TOL_CAL_LFRC}	Frequency tolerance for LFRC after calibration 13			±250	ppm
I _{LFRC}	Run current for 32.768 kHz RC oscillator		0.6	1	μΑ
t _{START_LFRC}	Startup time for 32.768 kHz RC oscillator		600		us

19.4.5 Synthesized low frequency clock (LFSYNT)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFSYNT}	Nominal frequency		32.768		kHz
f _{TOL_LFSYNT}	Frequency tolerance in addition to HFLCK tolerance ¹⁴		8		ppm
I _{LFSYNT}	Run current for synthesized 32.768 kHz		100		μΑ
t _{START_LFSYNT}	Startup time for synthesized 32.768 kHz		100		us

¹¹ Current drawn if HFXO is forced on through for instance using the low latency power mode.

¹² Value valid for calibration intervals ≤8 s and temperature variation within ±0.5°C. Decrease calibration interval as needed to keep temperature variation within ±0.5°C between calibrations.

Constant temperature within ±0.5 °C and calibration performed at least every 8 seconds

¹⁴ Frequency tolerance will be derived from the HFCLK source clock plus the LFSYNT tolerance



20 GPIO — General purpose input/output

The general purpose input/output (GPIO) is organized as one port with up to 32 I/Os (dependent on package) enabling access and control of up to 32 pins through one port. Each GPIO can be accessed individually.

GPIO has the following user-configurable features:

- Up to 32 GPIO
- 8 GPIO with Analog channels for SAADC, COMP or LPCOMP inputs
- Configurable output drive strength
- · Internal pull-up and pull-down resistors
- · Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- · One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- · All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register

The GPIO Port peripheral implements up to 32 pins, PIN0 through PIN31. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- · Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- · Analog input (for selected pins)

The PIN_CNF registers are retained registers. See *POWER* chapter for more information about retained registers.

20.1 Pin configuration

Pins can be individually configured, through the SENSE field in the PIN_CNF[n] register, to detect either a high level or a low level on their input.

When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal, and the default behaviour, as defined by the DETECTMODE register, is that the DETECT signal from all pins in the GPIO Port are combined into a common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals, see *Figure 20: GPIO Port and the GPIO pin details* on page 108. This mechanism is functional in both ON and OFF mode.



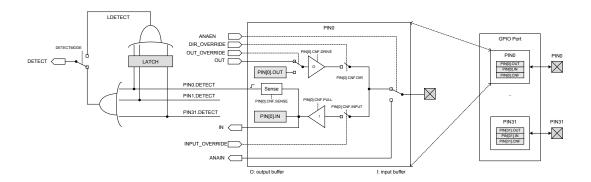


Figure 20: GPIO Port and the GPIO pin details

Figure 20: GPIO Port and the GPIO pin details on page 108 illustrates the GPIO port containing 32 individual pins, where PINO is illustrated in more detail as a reference. All the signals on the left side of the illustration are used by other peripherals in the system, and therefore, are not directly available to the CPU.

Make sure that a pin is in a level that cannot trigger the sense mechanism before enabling it. Detect will go high immediately if the sense condition configured in the PIN_CNF registers is met when the sense mechanism is enabled. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism. See *GPIOTE* — *GPIO* tasks and events on page 154.

See the following peripherals for more information about how the DETECT signal is used:

- POWER: uses the DETECT signal to exit from System OFF.
- GPIOTE: uses the DETECT signal to generate the PORT event.

When a pin's PINx.DETECT signal goes high, a flag will be set in the LATCH register, e.g. when the PIN0.DETECT signal goes high, bit 0 in the LATCH register will be set to '1'.

The LATCH register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the LATCH register will not be affected by a PINx.DETECT signal being set low.

If the CPU performs a clear operation on a bit in the LATCH register when the associated PINx.DETECT signal is high, the bit in the LATCH register will not be cleared.

The LDETECT signal will be set high when one or more bits in the LATCH register are '1'. The LDETECT signal will be set low when all bits in the LATCH register are successfully cleared to '0'.

If one or more bits in the LATCH register are '1' after the CPU has performed a clear operation on the LATCH registers, a rising edge will be generated on the LDETECT signal, this is illustrated in *Figure 21*: DETECT signal behavior on page 109.

Important: The CPU can read the LATCH register at any time to check if a SENSE condition has been met on one or more of the the GPIO pins even if that condition is no longer met at the time the CPU queries the LATCH register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change the behaviour of the GPIO port's DETECT signal from the default behaviour described above to instead be derived directly from the LDETECT signal, see *Figure 20: GPIO Port and the GPIO pin details* on page 108. *Figure 21: DETECT signal behavior* on page 109 illustrates the DETECT signals behaviour for these two alternatives.



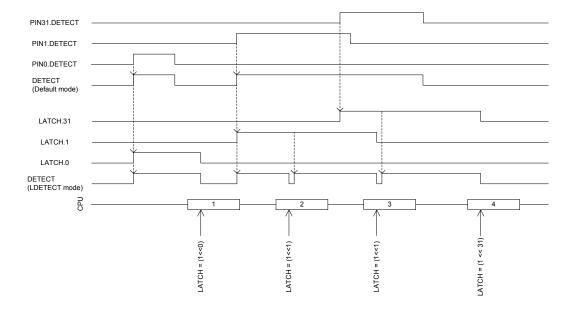


Figure 21: DETECT signal behavior

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see *Figure 20: GPIO Port and the GPIO pin details* on page 108. Inputs must be connected in order to get a valid input value in the IN register and for the sense mechanism to get access to the pin.

Other peripherals in the system can attach themselves to GPIO pins and override their output value and configuration, or read their analog or digital input value, see *Figure 20: GPIO Port and the GPIO pin details* on page 108.

Selected pins also support analog input signals, see ANAIN in *Figure 20: GPIO Port and the GPIO pin details* on page 108. The assignment of the analog pins can be found in *Pin assignments*.

Important: When a pin is configured as digital input, care has been taken in the nRF52 design to minimize increased current consumption when the input voltage is between V_{IL} and V_{IH} . However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between V_{IL} and V_{IH} for a long period of time.

20.2 Notes on usage and restrictions

20.2.1 GPIO located near the radio

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the Radio power supply and antenna pins.

Table 23: GPIO recommended usage on page 109 identifies some GPIO that have recommended usage guidelines to maximize radio performance in an application.

Table 23: GPIO recommended usage

Pin	GPIO	Recommended usage
27	P0.22	Low drive, low frequency I/O only.
28	P0.23	
29	P0.24	
37	P0.25	
38	P0.26	
39	P0.27	
40	P0.28	
41	P0.29	
42	P0.30	



Pin	GPIO	Recommended usage
43	P0.31	

20.2.2 NFC antenna pins

Two physical pins can be configured either as NFC antenna pins (factory default), or as GPIOs P0.09 and P0.10.

When configured as NFC antenna pins, the GPIOs on those pins will automatically be set to DISABLE state and a protection circuit will be enabled preventing the chip from being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2 V.

For information on how to configure these pins as normal GPIOs, see *NFCT* and *UICR* chapters. Note that the device will not be protected against strong NFC field damage if the pins are configured as GPIO and an NFC antenna is connected to the device. The pins will always be configured as NFC pins during power-on reset until the configuration is set according to the UICR register.

These two pins will have some limitations when configured as GPIO. The pin capacitance will be higher on these pins, and there is some current leakage between the two pins if they are driven to different logical values. To avoid leakage between the pins when configured as GPIO, these GPIOs should always be at the same logical value whenever entering one of the device power saving modes. See *Electrical specification*.

20.3 Registers

Table 24: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x50000000	GPIO	GPIO	General purpose input and output		Deprecated
0x50000000	GPIO	P0	General purpose input and output		

Table 25: Register Overview

Register	Offset	Description
OUT	0x504	Write GPIO port
OUTSET	0x508	Set individual bits in GPIO port
OUTCLR	0x50C	Clear individual bits in GPIO port
IN	0x510	Read GPIO port
DIR	0x514	Direction of GPIO pins
DIRSET	0x518	DIR set register
DIRCLR	0x51C	DIR clear register
LATCH	0x520	Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE
		registers
DETECTMODE	0x524	Select between default DETECT signal behaviour and LDETECT mode
PIN_CNF[0]	0x700	Configuration of GPIO pins
PIN_CNF[1]	0x704	Configuration of GPIO pins
PIN_CNF[2]	0x708	Configuration of GPIO pins
PIN_CNF[3]	0x70C	Configuration of GPIO pins
PIN_CNF[4]	0x710	Configuration of GPIO pins
PIN_CNF[5]	0x714	Configuration of GPIO pins
PIN_CNF[6]	0x718	Configuration of GPIO pins
PIN_CNF[7]	0x71C	Configuration of GPIO pins
PIN_CNF[8]	0x720	Configuration of GPIO pins
PIN_CNF[9]	0x724	Configuration of GPIO pins
PIN_CNF[10]	0x728	Configuration of GPIO pins
PIN_CNF[11]	0x72C	Configuration of GPIO pins
PIN_CNF[12]	0x730	Configuration of GPIO pins
PIN_CNF[13]	0x734	Configuration of GPIO pins
PIN_CNF[14]	0x738	Configuration of GPIO pins
PIN_CNF[15]	0x73C	Configuration of GPIO pins
PIN_CNF[16]	0x740	Configuration of GPIO pins



Register	Offset	Description
PIN_CNF[17]	0x744	Configuration of GPIO pins
PIN_CNF[18]	0x748	Configuration of GPIO pins
PIN_CNF[19]	0x74C	Configuration of GPIO pins
PIN_CNF[20]	0x750	Configuration of GPIO pins
PIN_CNF[21]	0x754	Configuration of GPIO pins
PIN_CNF[22]	0x758	Configuration of GPIO pins
PIN_CNF[23]	0x75C	Configuration of GPIO pins
PIN_CNF[24]	0x760	Configuration of GPIO pins
PIN_CNF[25]	0x764	Configuration of GPIO pins
PIN_CNF[26]	0x768	Configuration of GPIO pins
PIN_CNF[27]	0x76C	Configuration of GPIO pins
PIN_CNF[28]	0x770	Configuration of GPIO pins
PIN_CNF[29]	0x774	Configuration of GPIO pins
PIN_CNF[30]	0x778	Configuration of GPIO pins
PIN_CNF[31]	0x77C	Configuration of GPIO pins

20.3.1 OUT

Address offset: 0x504

Write GPIO port

VVI	пе	aPIO port																																	
Bitı	numbe	er		31	30	29	28	27	26	25	24	23	3 22	21	20	0 19	9 1	8 1	7 1	6 1	.5 :	14	13 :	12 :	11	10	9	8	7	6	5	4	3	2	1 (
Id				f	е	d	С	b	а	Z	Υ	Х	W	٧	L	J T	. 5	R)	Р	О	N I	M	L	K	J	I	Н	G	F	Ε	D	С	В
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	C	0	C) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (
ld	RW	Field	Value Id	Va	lue							D	escri	pti	on	1																			
Α	RW	PIN0										PC	0.0 p	in																					
			Low	0								Pi	in dri	vei	r is	lov	V																		
			High	1								Pi	in dri	vei	r is	hig	gh																		
В	RW	PIN1										PC	0.1 p	in																					
			Low	0								Pi	in dri	vei	r is	lov	V																		
			High	1								Pi	in dri	vei	r is	hig	gh																		
С	RW	PIN2										PC	0.2 p	in																					
			Low	0								Pi	in dri	vei	r is	lov	V																		
			High	1								Pi	in dri	vei	r is	hig	gh																		
D	RW	PIN3										PC	0.3 p	in																					
			Low	0								Pi	in dri	vei	r is	lov	V																		
			High	1								Pi	in dri	vei	r is	hig	gh																		
Е	RW	PIN4										PC	0.4 p	in																					
			Low	0								Pi	in dri	vei	r is	lov	V																		
			High	1								Pi	in dri	vei	r is	hig	gh																		
F	RW	PIN5										PC	0.5 p	in																					
			Low	0								Pi	in dri	vei	r is	lov	V																		
			High	1								Pi	in dri	vei	r is	hig	gh																		
G	RW	PIN6										PC	0.6 p	in																					
			Low	0								Pi	in dri	vei	r is	lov	V																		
			High	1								Pi	in dri	vei	r is	hig	gh																		
Н	RW	PIN7										PC	0.7 p	in																					
			Low	0									in dri																						
			High	1									in dri		r is	hi _ξ	gh																		
I	RW	PIN8											0.8 p																						
			Low	0									in dri																						
			High	1									in dri		r is	hig	gh																		
J	RW	PIN9											0.9 p																						
			Low	0									in dri																						
			High	1									in dri			hig	gh																		
K	RW	PIN10											0.10																						
			Low	0									in dri																						
			High	1								Pi	in dri	vei	r is	hig	gh																		



Bit r	numbe	er		31 30	29 2	28 27	7 26 2	25 24	1 23	22 21	20	19 18	3 17	16	15 1	4 13	12	11 1	0 9	8	7	6 5	5 4	3	2	1 0
Id										wv																
Rese	et 0x0	0000000		0 0	0	0 0	0	0 0	0	0 0	0	0 0	0	0	0 (0	0	0 (0 0	0	0	0 (0 0	0	0	0 0
Id	RW	Field	Value Id	Value					De	scription	on															
L	RW	PIN11							P0.	.11 pin																
			Low	0					Pin	driver	is lo	ow														
			High	1					Pin	n driver	is h	nigh														
M	RW	PIN12							P0.	.12 pin																
			Low	0					Pin	n driver	is lo	ow														
			High	1					Pin	n driver	is h	nigh														
N	RW	PIN13							P0.	.13 pin																
			Low	0					Pin	n driver	is lo	ow														
			High	1						n driver		nigh														
0	RW	PIN14								.14 pin																
			Low	0						n driver																
_			High	1						driver		nigh														
Р	RW	PIN15								.15 pin																
			Low	0						n driver																
0	DIA	DINI16	High	1						driver		ııgh														
Q	ĸW	PIN16	Low	0						.16 pin		ov.:														
			Low High	0						n driver n driver																
R	D\A/	PIN17	nigii	1						.17 pin		ııgıı														
N	rvv	PIN17	Low	0						.17 piii driver		014/														
			High	1						driver																
S	RW/	PIN18	111611	-						.18 pin		''B''														
,		11110	Low	0						driver		οw														
			High	1						n driver																
Т	RW	PIN19	6	_						.19 pin																
			Low	0						n driver		ow														
			High	1						n driver																
U	RW	PIN20	•							.20 pin																
			Low	0					Pin	n driver	is lo	ow														
			High	1					Pin	n driver	is h	nigh														
٧	RW	PIN21							P0.	.21 pin																
			Low	0					Pin	n driver	is lo	ow														
			High	1					Pin	n driver	is h	nigh														
W	RW	PIN22							P0.	.22 pin																
			Low	0					Pin	n driver	is lo	ow														
			High	1					Pin	n driver	is h	nigh														
Χ	RW	PIN23							P0.	.23 pin																
			Low	0					Pin	n driver	is lo	ow														
			High	1					Pin	n driver	is h	nigh														
Υ	RW	PIN24								.24 pin																
			Low	0						n driver																
			High	1						n driver		nigh														
Z	RW	PIN25								.25 pin																
			Low	0						n driver																
	B	DINIAG	High	1						driver		nigh														
а	RW	PIN26								.26 pin																
			Low	0						n driver																
L	DV44	DINI27	High	1						driver		ııgh														
b	KW	PIN27	Low	0						.27 pin		01::														
			Low	0						n driver																
	DVA	DINIDO	High	1						driver		ııgn														
С	ĸW	PIN28	Low	0						.28 pin		014														
			Low	1						n driver																
d	D/V/	PIN29	High	_						n driver .29 pin		ıığı1														
u	11.00	THVZJ							۲0.	.29 piri																



Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	Х	W	٧	U	Т	S	R	Q	Р	0	N N	1 L	K	J	1	Н	G	F	Ε	ОС	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
			Low	0								Pir	dri	ver	is l	ow																	
			High	1								Pir	dri	ver	is h	nigh	1																
е	RW	PIN30										PO	.30	pin																			
			Low	0								Pir	dri	iver	is l	ow																	
			High	1								Pir	dri	iver	is h	nigh	ı																
f	RW	PIN31										P0	.31	pin																			
			Low	0								Pir	dri	iver	is l	ow																	
			High	1								Pir	dri	iver	is h	nigh	1																

20.3.2 OUTSET

Address offset: 0x508

Set individual bits in GPIO port

Read: reads value of OUT register.

	reads value of Ot	<u> </u>																												
Bit numb	er									23 22																				1
Id										X W																				В
Reset 0x	00000000		0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0
ld RW	/ Field	Value Id	Val	ue						Descri	ptio	n																		
A RW	PIN0								F	P0.0 p	in																			
		Low	0						F	Read:	pin	driv	/er i	is Ic	wc															
		High	1						F	Read:	pin	driv	/er i	is h	igh															
		Set	1						١	Write:	wri	ting	ga'	1' s	sets	the	e pi	n h	gh;	wri	ting	a '0	' ha	s no	eff	ect				
B RW	PIN1								F	P0.1 p	in																			
		Low	0						F	Read:	pin	driv	/er i	is Ic	ow															
		High	1						F	Read:	pin	driv	/er i	is h	igh															
		Set	1						١	Write:	wri	ting	ga'	1' s	sets	the	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				
C RW	PIN2								F	P0.2 p	in																			
		Low	0						F	Read:	pin	driv	/er i	is Ic	wc															
		High	1						F	Read:	pin	driv	/er i	is h	igh															
		Set	1						١	Write:	wri	ting	g a '	1' s	sets	the	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				
D RW	PIN3								F	P0.3 p	in																			
		Low	0						F	Read:	pin	driv	/er i	is Ic	ow															
		High	1						F	Read:	pin	driv	/er i	is h	igh															
		Set	1						١	Write:	wri	ting	ga'	1' s	sets	the	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				
E RW	PIN4								F	P0.4 p	in																			
		Low	0						F	Read:	pin	driv	/er i	is Ic	wc															
		High	1						F	Read:	pin	driv	/er i	is h	igh															
		Set	1						١	Write:	wri	ting	ga'	1' s	sets	the	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				
F RW	PIN5								F	P0.5 p	in																			
		Low	0						F	Read:	pin	driv	/er i	is Ic	wc															
		High	1						F	Read:	pin	driv	/er i	is h	igh															
		Set	1						١	Write:	wri	ting	ga'	1' s	ets	the	e pi	n hi	igh;	wri	ting	a '0	' ha	s no	eff	ect				
G RW	PIN6								F	P0.6 p	in																			
		Low	0						F	Read:	pin	driv	/er i	is Ic	ow															
		High	1						F	Read:	pin	driv	/er i	is h	igh															
		Set	1							Write:					-	the	e pi	n hi	igh;	wri	ting	a '0	' ha	s no	eff	ect				
H RW	PIN7									P0.7 p									<i>,</i>		J									
		Low	0							Read:		driv	/er i	is Id	ow															
		High	1							Read:																				
		Set	1							Write:					-	the	e pi	n h	gh:	wri	ting	a '0	' ha	s no	eff	ect				
I RW	PIN8									P0.8 p			-				۲.		J .,		-0	,								
	- ···- -	Low	0							Read:		driv	/er i	is Ir	าพ															
		High	1							Read:																				
		LIIRII	1						ı	nedu:	hili	uriv	rei I	1)	ıığıı															



Bit n	umbe	r		31 30 29 28 27	7 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id						X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	t 0x0	0000000		0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value		Description
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
J	RW	PIN9				P0.9 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
K	RW	PIN10				P0.10 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
L	RW	PIN11				P0.11 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
	DIA	DINIA 2	Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
М	RW	PIN12	Laur	0		P0.12 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high Write: writing a '1' sets the pin high; writing a '0' has no effect
N	B/V	PIN13	Set	1		P0.13 pin
IN	IVV	LINITO	Low	0		Read: pin driver is low
			High	1		Read: pin driver is low
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
0	RW	PIN14	Jet	1		P0.14 pin
Ū			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
Р	RW	PIN15				P0.15 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
Q	RW	PIN16				P0.16 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
R	RW	PIN17				P0.17 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
S	RW	PIN18				P0.18 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
			Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
Т	RW	PIN19				P0.19 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
	B	DINIZO	Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
U	кW	PIN20	Laur	0		P0.20 pin
			Low	0		Read: pin driver is low
			High	1		Read: pin driver is high
V	DVA	DINI21	Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect
٧	KVV	PIN21	Low	0		P0.21 pin
			Low	0		Read: pin driver is low
			High Set	1		Read: pin driver is high Write: writing a '1' sets the nin high: writing a '0' has no effect
W	R\A/	PIN22	Set	1		Write: writing a '1' sets the pin high; writing a '0' has no effect P0.22 pin
vv	11.44	1 11444	Low	0		Read: pin driver is low
				J		



Bit r	numbe	r		31 30	29	28	27 2	6 2	25 24	1 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id											X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0(000000									0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW		Value Id	Value							Description
			High	1							Read: pin driver is high
			Set	1							Write: writing a '1' sets the pin high; writing a '0' has no effect
Χ	RW	PIN23									P0.23 pin
			Low	0							Read: pin driver is low
			High	1							Read: pin driver is high
			Set	1							Write: writing a '1' sets the pin high; writing a '0' has no effect
Υ	RW	PIN24		_							P0.24 pin
•			Low	0							Read: pin driver is low
			High	1							Read: pin driver is high
			Set	1							Write: writing a '1' sets the pin high; writing a '0' has no effect
Z	RW	PIN25		-							P0.25 pin
_		20	Low	0							Read: pin driver is low
			High	1							Read: pin driver is high
			Set	1							Write: writing a '1' sets the pin high; writing a '0' has no effect
а	RW	PIN26	Sec	-							P0.26 pin
ŭ		20	Low	0							Read: pin driver is low
			High	1							Read: pin driver is high
			Set	1							Write: writing a '1' sets the pin high; writing a '0' has no effect
b	RW	PIN27		_							P0.27 pin
			Low	0							Read: pin driver is low
			High	1							Read: pin driver is high
			Set	1							Write: writing a '1' sets the pin high; writing a '0' has no effect
С	RW	PIN28									P0.28 pin
			Low	0							Read: pin driver is low
			High	1							Read: pin driver is high
			Set	1							Write: writing a '1' sets the pin high; writing a '0' has no effect
d	RW	PIN29									P0.29 pin
			Low	0						F	Read: pin driver is low
			High	1							Read: pin driver is high
			Set	1						١	Write: writing a '1' sets the pin high; writing a '0' has no effect
e	RW	PIN30								F	P0.30 pin
			Low	0							Read: pin driver is low
			High	1							Read: pin driver is high
			Set	1							Write: writing a '1' sets the pin high; writing a '0' has no effect
f	RW	PIN31									P0.31 pin
			Low	0							Read: pin driver is low
			High	1							Read: pin driver is high
			Set	1							Write: writing a '1' sets the pin high; writing a '0' has no effect
											•

20.3.3 OUTCLR

Address offset: 0x50C

Clear individual bits in GPIO port Read: reads value of OUT register.

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 1	.9 1	8 1	7 1	5 15	5 14	13	12	11	10	9	8	7	6	5 4	1 3	2	1 0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	۷	U -	Т :	S F	R C	Į P	0	Ν	М	L	K	J	L	Н	G	F E	D	С	В А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	scrip	otio	n																	
Α	RW	PIN0									P0.	0 pi	n																			
			Low	0							Rea	ad: p	oin d	driv	er is	lov	٧															
			High	1								Rea	ad: p	oin d	driv	er is	hig	gh														
			Clear	1								Wr	ite:	writ	ing	a '1	l' se	ts t	he p	oin	low	wr	iting	; a '	0' h	ıas ı	10 6	effe	ct			
В	RW	PIN1										P0.	1 pi	n																		



Bit n	iumbe	r		31 30	29 2	28 27	7 26 :	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d	c b	а	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000		0 0	0	0 0	0	0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value					Description
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
		2112	Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
С	RW	PIN2	Laur	0					P0.2 pin
			Low	0					Read: pin driver is low Read: pin driver is high
			High Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
D	RW	PIN3	Cicai	-					P0.3 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
Е	RW	PIN4							P0.4 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
F	RW	PIN5							P0.5 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
G	RW	PIN6							P0.6 pin
			Low	0					Read: pin driver is low
			High Clear	1					Read: pin driver is high
Н	R\M	PIN7	Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect P0.7 pin
"	11.00	1 1147	Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
ı	RW	PIN8							P0.8 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
J	RW	PIN9							P0.9 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
K	RW	PIN10							P0.10 pin
			Low	0					Read: pin driver is low
			High Clear	1					Read: pin driver is high Write: writing a '1' sets the pin low; writing a '0' has no effect
L	RW	PIN11	Clear	1					P0.11 pin
_			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
М	RW	PIN12							P0.12 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
N	RW	PIN13							P0.13 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
0	RW	PIN14							P0.14 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect



Bit n	numbe	er		31 30	29 2	28 27	7 26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000		0 0	0	0 0	0 (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	:				Description
Р	RW	PIN15							P0.15 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
Q	RW	PIN16							P0.16 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
R	RW	PIN17							P0.17 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
S	RW	PIN18							P0.18 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
Т	RW	PIN19							P0.19 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
U	RW	PIN20							P0.20 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
V	RW	PIN21		•					P0.21 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
\A/	D\A/	PIN22	Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
W	KVV	PINZZ	Low	0					P0.22 pin
			Low	1					Read: pin driver is low
			High Clear	1					Read: pin driver is high Write: writing a '1' sets the pin low; writing a '0' has no effect
Y	RW	PIN23	Cicai	_					P0.23 pin
^	11.44	111125	Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
Υ	RW	PIN24	Cicui	-					P0.24 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
Z	RW	PIN25							P0.25 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
a	RW	PIN26	oleu.	-					P0.26 pin
-		-	Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
b	RW	PIN27							P0.27 pin
			Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			Clear	1					Write: writing a '1' sets the pin low; writing a '0' has no effect
С	RW	PIN28							P0.28 pin
	-		Low	0					Read: pin driver is low
			High	1					Read: pin driver is high
			•						,



	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Value Id	Value Description
Clear	1 Write: writing a '1' sets the pin low; writing a '0' has no effect
	P0.29 pin
Low	0 Read: pin driver is low
High	1 Read: pin driver is high
Clear	1 Write: writing a '1' sets the pin low; writing a '0' has no effect
	P0.30 pin
Low	0 Read: pin driver is low
High	1 Read: pin driver is high
Clear	1 Write: writing a '1' sets the pin low; writing a '0' has no effect
	P0.31 pin
Low	0 Read: pin driver is low
High	1 Read: pin driver is high
Clear	1 Write: writing a '1' sets the pin low; writing a '0' has no effect
	Clear Low High Clear Low High Clear Low High Clear

20.3.4 IN

Address offset: 0x510 Read GPIO port

Low			то рож																												
Note		numb	er																												
Ide Rev Field Value Id Value Description A R PIND ————————————————————————————————————																															
A							0 (0 0	0	0	0					0	0	0	0	0	0	0 0	0	0	0	0	0 () (0	0	0 0
	Id			Value Id	Va	lue									1																
	Α	R	PIN0									PC).0 pin	1																	
B				Low	0							Piı	n inpu	ut is	low	V															
Low				High	1							Piı	n inpu	ut is	hig	h															
C	В	R	PIN1									PC).1 pin	1																	
C R PIN2 Low 0 Pin input is low Low 1 Pin input is low Pin input is high Pin input is high D R PIN3 Low 0 Pin input is high E R PIN4 Low 0 Pin input is low E Pin PIN5 Low 0 Pin input is low F Pin Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input is low Pin input				Low	0							Piı	n inpu	ut is	low	V															
Low 1				High	1							Piı	n inpu	ut is	hig	h															
Pin	С	R	PIN2									PC).2 pin	1																	
D R PIN3 Low 0 Pin input is low E R PIN4 1 Pin input is high E R PIN4 Low 0 Pin input is low F R PIN5 Low 0 Pin input is high F R PIN5 Low 0 Pin input is low G R PIN6 Low 0 Pin input is low G PIN5 Low 0 Pin input is low G PIN5 Low 0 Pin input is low H PIN5 PIN7 PIN9 PIN input is low H PIN5 PIN9 PIN input is low PIN input is low H PIN5 PIN9 PIN input is low PIN input is low H PIN5 PIN5 PIN input is low PIN input is low H PIN5 PIN5 PIN5 PIN input is low PIN5 PIN5 PIN5 PIN5 PIN5				Low	0							Piı	n inpu	ut is	low	V															
Low				High	1							Piı	n inpu	ut is	hig	h															
High 1	D	R	PIN3									PO).3 pin	1																	
E R PIN4 Low 0 Pin input is low F R PIN5 Pin input is high F R PIN5 Low 0 Pin input is low G R PIN6 Low 0 Pin input is high G R PIN7 Low 0 Pin input is low H R PIN7 Low 0 Pin input is low I R PIN8 Low 0 Pin input is low I R PIN8 Low 0 Pin input is low I R PIN9 Low 0 Pin input is low J R PIN9 Low 0 Pin input is high J R PIN9 PIN9 PIN input is low H PIN input is low PIN input is low PIN input is low PIN input is low PIN input is low PIN input is low PIN input input is low PIN input is low PIN input is low				Low	0							Piı	n inpu	ut is	low	V															
Low 1				High	1							Piı	n inpu	ut is	hig	h															
Fig. R PIN5 Low Defining the shigh Po.5 pin	Ε	R	PIN4									PC).4 pin	1																	
F R PIN5 Low 0 Pin input is low G R PIN6 Low 0 Pin input is high G R PIN7 Low 0 Pin input is low H R PIN7 Low 0 Pin input is low I R PIN8 Low 0 Pin input is high I R PIN9 Low 0 Pin input is low J R PIN9 Low 0 Pin input is high J R PIN9 Low 0 Pin input is high K R PIN9 Low 0 Pin input is low High 1 Pin input is low Pin input is high				Low	0							Piı	n inpu	ut is	low	V															
Low Din input is low Pin input is low Pin input is low Pin input is high				High	1							Piı	n inpu	ut is	hig	h															
Final Fina	F	R	PIN5									PO).5 pin	1																	
G R PIN6 Low 0 Pin input is low H High 1 Pin input is high H PIN7 Low 0 Pin input is low I High 1 Pin input is high I PIN8 Low 0 Pin input is low I Pin input is low Pin input is high J PIN9 Low 0 Pin input is high J Pin input is low Pin input is low F PIN10 Pin input is high				Low	0							Piı	n inpu	ut is	low	V															
Low 0 Pin input is low Pin input is low Pin input is low Pin input is low Pin input is high P0.7 pin P0.7 pin P0.8 pin input is high P0.8 pin input is high P0.8 pin input is low Pin input is high P0.9 pin input is low P0.9 pin input is high P0.9 pin input				High	1							Piı	n inpu	ut is	hig	h															
H R PIN7 Formula (Decomption) Pin input is high I R PIN8 Formula (Decomption) Pin input is low I R PIN8 Formula (Decomption) Pin input is low I Pin input is low Pin input is high J PIN9 Formula (Decomption) Po.9 pin K PIN10 Formula (Decomption) Pin input is high K PIN10 Formula (Decomption) Pin input is high	G	R	PIN6									PC).6 pin	1																	
H R PIN7 Low 0 Pin input is low I Pin input is high Pin input is high I Pin input is low Pin input is low I Pin input is low Pin input is high J Pin input is high Pin input is low I Pin input is low Pin input is low Pin input is high Pin input is high K Pin input is high Pin input is high				Low	0							Piı	n inpu	ut is	low	V															
Low O Pin input is low Pin input is high Pin input is high PO.8 pin PO.8 pin Low O Pin input is low Pin input is high Pin input is high J PNP Low O Pin input is low K PNP Low O Pin input is low Fin input is high Pin input is high Pin input is high				High	1							Piı	n inpu	ut is	hig	h															
I R PIN8 Low 0 Pin input is high J R PIN9 Low 0 Pin input is low J R PIN9 PO.9 pin Low 0 Pin input is low High 1 Pin input is low K R PIN10 Pin input is high	Н	R	PIN7									PO). 7 pin	1																	
I R PIN8 Low 0 Pin input is low I High 1 Pin input is high J R PIN9 Low 0 Pin input is low I High 1 Pin input is low F Pin input is high Pin input is high				Low	0							Piı	n inpu	ut is	low	V															
Low 0 Pin input is low Pin input is high Pin input is high Punch input is high Punch input is low Low 0 Pin input is low High 1 Pin input is high K R PIN10 Function Punch input is high				High	1							Piı	n inpu	ut is	hig	h															
J R PIN9 Foliable PO.9 pin Low 0 Pin input is low High 1 Pin input is high K R PIN10 Foliable Po.10 pin	1	R	PIN8									PC).8 pin	1																	
J R PIN9 P0.9 pin Low 0 Pin input is low High 1 Pin input is high K R PIN10 P0.10 pin				Low	0							Piı	n inpu	ut is	low	V															
Low 0 Pin input is low High 1 Pin input is high K R PIN10 P0.10 pin				High	1							Piı	n inpu	ut is	hig	h															
High 1 Pin input is high K R PIN10 P0.10 pin	J	R	PIN9									PC).9 pin	1																	
K R PIN10 P0.10 pin				Low	0							Pi	n inpu	ut is	low	V															
				High	1							Piı	n inpu	ut is	hig	h															
Low 0 Pin input is low	K	R	PIN10									PC).10 p	in																	
				Low	0							Piı	n inpu	ut is	low	V															



Bit r	numbe	er		31 30	29 28	27 2	6 25	24	23 22 :	21 2	20 19	18 :	17 1	6 1	5 14	13	12 1	11 10	9	8	7	6 5	4	3	2 1	0
Id									x w																	
Res	et 0x0	0000000		0 0	0 0	0 (0 0	0	0 0	0	0 0	0	0 (0 0	0	0	0	0 0	0	0	0	0 0	0	0	0	0
Id	RW	Field	Value Id	Value					Descri	ptio	n															
			High	1					Pin inp	ut is	high															
L	R	PIN11							P0.11 p																	
			Low	0					Pin inp																	
			High	1					Pin inp		high															
М	R	PIN12		_					P0.12 p																	
			Low	0					Pin inp																	
N	R	PIN13	High	1					Pin inp		nign															
IN	N	LINTO	Low	0					P0.13 p		low															
			High	1					Pin inp																	
0	R	PIN14	111611	-					P0.14 p		, <u>6</u>															
Ū			Low	0					Pin inp		low															
			High	1					Pin inp																	
Р	R	PIN15	<u> </u>						P0.15 p																	
			Low	0					Pin inp		low															
			High	1					Pin inp																	
Q	R	PIN16							P0.16 p	oin																
			Low	0					Pin inp	ut is	low															
			High	1					Pin inp	ut is	high															
R	R	PIN17							P0.17 p	oin																
			Low	0					Pin inp	ut is	low															
			High	1					Pin inp	ut is	high															
S	R	PIN18							P0.18 p	oin																
			Low	0					Pin inp	ut is	low															
			High	1					Pin inp	ut is	high															
Т	R	PIN19							P0.19 p	oin																
			Low	0					Pin inp	ut is	low															
			High	1					Pin inp		high															
U	R	PIN20							P0.20 p																	
			Low	0					Pin inp																	
.,		DINI24	High	1					Pin inp		high															
V	R	PIN21	Low	0					P0.21 p		· lau															
			Low High	1					Pin inp Pin inp																	
W	R	PIN22	iligii	1					P0.22 p		iligii															
**	11	1111/22	Low	0					Pin inp		low															
			High	1					Pin inp																	
Х	R	PIN23	6	-					P0.23 p		,															
			Low	0					Pin inp		low															
			High	1					Pin inp																	
Υ	R	PIN24							P0.24 p																	
			Low	0					Pin inp		low															
			High	1					Pin inp	ut is	high															
Z	R	PIN25							P0.25 p	oin																
			Low	0					Pin inp	ut is	low															
			High	1					Pin inp	ut is	high															
а	R	PIN26							P0.26 p	oin																
			Low	0					Pin inp	ut is	low															
			High	1					Pin inp	ut is	high															
b	R	PIN27							P0.27 p	oin																
			Low	0					Pin inp																	
			High	1					Pin inp		high															
С	R	PIN28							P0.28 p																	
			Low	0					Pin inp																	
			High	1					Pin inp	ut is	high															



Bitı	numbe	er		31	30	29	28	27	26	25	24 2	23 2	2 21	. 20	19	18	17	16	15	14 1	.3 12	2 11	10	9	8	7	6	5	4 3	2	1	0
Id				f	e	d	С	b	а	Z	Υ	X V	V V	U	Т	S	R	Q	Р	0 1	N M	l L	K	J	1	Н	G	F	E [) C	В	Α
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						ı	Desc	ripti	ion																		
d	R	PIN29									ı	0.2	9 pir	ı																		
			Low	0							ı	Pin i	nput	is l	ow																	
			High	1							ı	Pin i	nput	is l	nigh																	
е	R	PIN30									ı	0.3	0 pir	1																		
			Low	0							ı	Pin i	nput	is l	ow																	
			High	1							ı	Pin i	nput	is	nigh																	
f	R	PIN31									ı	0.3	1 pir	1																		
			Low	0							ı	Pin i	nput	is l	ow																	
			High	1							ı	Pin i	nput	is	nigh																	

20.3.5 DIR

Address offset: 0x514 Direction of GPIO pins

Rit i	numbe	er.		31 30	29	28	27 .	26.2	5 2/	1 2	3 22 2	21	20 1	Q 1	Ω 1 ⁻	7 1	3 19	. 1/	13	12	11	10	Q	ρ.	7	6 5	. 1	3	2	1 (
Id	Turribo	-1									3 22 2 (W '																			
	at 0v0	0000000									0 0																			
Id		Field	Value Id	Value		Ů	٠	•	0 0		escrip					, ,	Ů	Ů	Ů	Ü	Ü	Ü	٠	•	•			Ü	Ü	
A		PINO									0.0 pir		•••																	
			Input	0							in set		innu	ıt																
			Output	1							in set																			
В	RW/	PIN1	Catpat	_							0.1 pir		outp	Juc																
		11112	Input	0							in set		innu	ıt																
			Output	1							in set																			
С	R\M/	PIN2	Output	1							0.2 pir		outp	Jut																
C	11.00	FIIVZ	Input	0							in set		innu	+																
			Output	1							in set																			
D	D\A/	PIN3	Output	1							0.3 pir		outp	Jut																
U	NVV	riivo	Innut	0																										
			Input	1							in set																			
_	DVA	DINIA	Output	1							in set		outp	υι																
Ε	KVV	PIN4	la accept	^							0.4 pir																			
			Input	0							in set																			
-	DIA	DINE	Output	1							in set		outp	out																
F	RW	PIN5		•							0.5 pir																			
			Input	0							in set																			
			Output	1							in set		outp	out																
G	RW	PIN6		_							0.6 pir		_																	
			Input	0							in set																			
			Output	1							in set		outp	out																
Н	RW	PIN7		_							0.7 pir		_																	
			Input	0							in set																			
			Output	1							in set		outp	out																
I	RW	PIN8									0.8 pir																			
			Input	0							in set																			
			Output	1							in set		outp	out																
J	RW	PIN9									0.9 pir																			
			Input	0							in set																			
			Output	1						Р	in set	as	outp	out																
K	RW	PIN10								Р	0.10 p	in																		
			Input	0						Р	in set	as	inpu	it																
			Output	1						Р	in set	as	outp	ut																
L	RW	PIN11								Р	0.11 p	in																		
			Input	0						P	in set	as	inpu	it																
			Output	1						Р	in set	as	outp	out																



Bit r	numbe	er		31 30	29 28	27	26 2	5 24	23 22 21	1 20	19 1	8 17	16 1	15 14	1 13	12 1:	1 10	9	8 7	6	5	4 3	2	1 (
Id									x w v															ВА
Rese	et 0x0	0000000		0 0	0 0	0	0 0	0 0	0 0 0	0	0 (0	0	0 0	0	0 0	0	0	0 0	0	0	0 0	0	0 0
Id	RW	Field	Value Id	Value					Descript	ion														
М	RW	PIN12							P0.12 pir	n														
			Input	0					Pin set a	s inp	out													
			Output	1					Pin set a	s out	tput													
N	RW	PIN13							P0.13 pir	n														
			Input	0					Pin set a	s inp	out													
			Output	1					Pin set a	s out	tput													
0	RW	PIN14							P0.14 pir	n														
			Input	0					Pin set a	s inp	out													
			Output	1					Pin set a	s out	tput													
Р	RW	PIN15							P0.15 pir	n														
			Input	0					Pin set a	s inp	out													
			Output	1					Pin set a	s out	tput													
Q	RW	PIN16							P0.16 pir	n														
			Input	0					Pin set a	s inp	ut													
			Output	1					Pin set a	s out	tput													
R	RW	PIN17							P0.17 pir	n														
			Input	0					Pin set a	s inp	out													
			Output	1					Pin set a	s out	tput													
S	RW	PIN18							P0.18 pir	n														
			Input	0					Pin set a	s inp	out													
			Output	1					Pin set a	s out	tput													
Т	RW	PIN19							P0.19 pir	n														
			Input	0					Pin set a		out													
			Output	1					Pin set a															
U	RW	PIN20	•						P0.20 pir		•													
			Input	0					Pin set a		out													
			Output	1					Pin set a															
V	RW	PIN21							P0.21 pir															
			Input	0					Pin set a		out													
			Output	1					Pin set a															
W	RW	PIN22							P0.22 pir															
			Input	0					Pin set a		out													
			Output	1					Pin set a															
Х	RW	PIN23							P0.23 pir		-p													
			Input	0					Pin set a		nut													
			Output	1					Pin set a															
Υ	RW	PIN24	Julput	-					P0.24 pir		cpuc													
•			Input	0					Pin set a		nut													
			Output	1					Pin set a															
Z	RW	PIN25	Оперия	-					P0.25 pir		cpuc													
_		11125	Input	0					Pin set a		nut													
			Output	1					Pin set a															
a	RW/	PIN26	Catput	-					P0.26 pir		tput													
u		11120	Input	0					Pin set a		nut													
			Output	1					Pin set a															
b	R\M	PIN27	Output	-					P0.27 pir		tput													
J	11.44	1 1/44/	Input	0					Pin set a		ni it													
			Output	1					Pin set a															
	D\A/	PIN28	Catput						P0.28 pir		tput													
С	r/ VV	FIINZO	Innut	0							+													
			Input	0					Pin set a															
لہ	Dist	DINIO	Output	1					Pin set a		ıput													
d	KW	PIN29	lanc.	0					P0.29 pir															
			Input	0					Pin set a															
		DINIO	Output	1					Pin set a		tput													
е	кW	PIN30							P0.30 pir	n														



Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcba Z	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Reset 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
	Input	0	Pin set as input
	Output	1	Pin set as output
f RW PIN31			P0.31 pin
	Input	0	Pin set as input
	Output	1	Pin set as output

20.3.6 DIRSET

Address offset: 0x518

DIR set register

Read: reads value of DIR register.

	numbe	er			\$\frac{1}{2}\$ 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					X W V U T S R Q P O N M L K J I H G F E D C B A
		0000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld		Field	Value Id	Value	Description
Α	RW	PIN0			Set as output pin 0
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
_	5144	B1414	Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect
В	KW	PIN1			Set as output pin 1
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect
С	RW	PIN2			Set as output pin 2
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect
D	RW	PIN3			Set as output pin 3
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect
E	RW	PIN4			Set as output pin 4
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect
F	RW	PIN5			Set as output pin 5
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect
G	RW	PIN6			Set as output pin 6
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect
Н	RW	PIN7			Set as output pin 7
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect
ı	RW	PIN8			Set as output pin 8
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect
J	RW	PIN9			Set as output pin 9
			Input	0	Read: pin set as input
			put	~	nead, p.n. sec do input



Bit r	numbe	er		31 30 2	29 28 2	27 26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value				Description
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
K	RW	PIN10		_				Set as output pin 10
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
	D\A/	PIN11	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
L	LVV	FINIT	Input	0				Set as output pin 11 Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
М	RW	PIN12		_				Set as output pin 12
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
N	RW	PIN13						Set as output pin 13
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
0	RW	PIN14						Set as output pin 14
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Р	RW	PIN15						Set as output pin 15
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
_	D\A/	PIN16	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Q	IV V V	PINIO	Input	0				Set as output pin 16 Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
R	RW	PIN17						Set as output pin 17
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
S	RW	PIN18						Set as output pin 18
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Т	RW	PIN19						Set as output pin 19
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
U	RW	PIN20		_				Set as output pin 20
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
\/	D\A/	DINI21	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
V	IVVV	PIN21	Input	0				Set as output pin 21 Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
W	RW	PIN22		_				Set as output pin 22
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Х	RW	PIN23						Set as output pin 23



Bit	number		31	30	29	28 :	27 26	5 2	25 24	1 2	3 22 21 20	19	18 1	7 1	.6 1	L5 1	4 :	13 1	2 1	1 10) 9	8	7	6	5	4	3	2 :	1 0
Id			f	e	d	С	b a		ΖY		x w v u	Т	S R	۲ (Q	Р (C	N N	ИΙ	_ K	J	-1	Н	G	F	Ε	D	C E	ВА
Res	set 0x00000000		0	0	0	0	0 0		0 0		0 0 0	0	0 0) (0 (0	0	0 (0 (0	0	0	0	0	0	0	0	0 (0 0
Id	RW Field	Value Id	Val	ue						0	escription																		
		Input	0							F	lead: pin set	t as i	nput	t															
		Output	1							F	lead: pin set	t as o	outp	ut															
		Set	1							٧	Vrite: writin	ng a '	1' se	ts	pin	to	out	put	; wr	itin	g a	'0' h	as ı	no e	ffe	t			
Υ	RW PIN24									S	et as output	ıt pin	24																
		Input	0							F	lead: pin set	t as i	nput	t															
		Output	1							F	lead: pin set	t as o	outp	ut															
		Set	1							٧	Vrite: writin	ng a '	1' se	ts	pin	to	out	put	; wr	itin	g a	'0' h	as ı	no e	ffe	t			
Z	RW PIN25									S	et as output	ıt pin	25																
		Input	0							F	lead: pin set	t as i	nput	t															
		Output	1							F	lead: pin set	t as o	outp	ut															
		Set	1							٧	Vrite: writin	ng a '	1' se	ts	pin	to	out	put	; wr	itin	g a	'0' h	as ı	no e	ffe	ct			
а	RW PIN26									S	et as output	ıt pin	26																
		Input	0							F	lead: pin set	t as i	nput	t															
		Output	1							F	lead: pin set	t as o	outp	ut															
		Set	1							٧	Vrite: writin	ng a '	1' se	ts	pin	to	out	put	; wr	itin	g a	'0' h	as ı	no e	ffe	ct			
b	RW PIN27									S	et as output	ıt pin	27																
		Input	0							F	lead: pin set	t as i	nput	t															
		Output	1							F	lead: pin set	t as o	outp	ut															
		Set	1							٧	Vrite: writin	ng a '	1' se	ts	pin	to	out	put	; wr	itin	g a	'0' h	as ı	no e	ffe	ct			
С	RW PIN28									S	et as output	ıt pin	28																
		Input	0							F	lead: pin set	t as i	nput	t															
		Output	1							F	lead: pin set	t as o	outp	ut															
		Set	1							٧	Vrite: writin	ng a '	1' se	ts	pin	to	out	put	; wr	itin	g a	'0' h	as ı	no e	ffe	t			
d	RW PIN29									S	et as output	ıt pin	29																
		Input	0							F	lead: pin set	t as i	nput	t															
		Output	1							F	lead: pin set	t as o	outp	ut															
		Set	1							٧	Vrite: writin	ng a '	1' se	ts	pin	to	out	put	; wr	itin	g a	'0' h	as ı	10 6	ffe	ct			
е	RW PIN30									S	et as output	ıt pin	30																
		Input	0							F	lead: pin set	t as i	nput	t															
		Output	1							F	lead: pin set	t as o	outp	ut															
		Set	1							٧	Vrite: writin	ng a '	1' se	ts	pin	to	out	put	; wr	itin	g a	'0' h	as ı	no e	ffe	t			
f	RW PIN31									S	et as output	ıt pin	31																
		Input	0							F	lead: pin set	t as i	nput	t															
		Output	1							F	lead: pin set	t as o	outp	ut															
		Set	1							٧	Vrite: writin	ng a '	1' se	ts	pin	to	out	put	; wr	itin	g a	'0' h	as ı	no e	ffe	ct			

20.3.7 DIRCLR

Address offset: 0x51C DIR clear register

Read: reads value of DIR register.

Bit number		31	30 2	9 2	8 27	26 2	25 2	4 23	3 22 :	21 2	0 19	9 18	17	16 :	15 1	4 13	12	11 1	.0 9	8	7	6	5	4 3	2	1 0
Id		f	e d	d c	b b	a i	ZΥ	ΥX	W	Vι	J T	S	R	Q	Р (O N	М	L	K J	- 1	Н	G	F	E 0	С	ВА
Reset 0x0000	0000	0	0 (0	0 0	0	0 0	0 0	0	0 (0 0	0	0	0	0 (0 0	0	0	0 0	0	0	0	0	0 0	0	0 0
Id RW Fie	ld Value Id	Va	lue					D	escrip	otio	n															
A RW PI	0							Se	et as i	npu	t pir	n 0														
	Input	0						Re	ead: p	oin s	et a	s inp	out													
	Output	1						Re	ead: p	oin s	et a	s ou	tput													
	Clear	1						W	/rite:	writ	ing a	a '1'	sets	pin	to i	npu	t; wr	iting	a '0)' ha	s no	eff	ect			
B RW PI	1							Se	et as i	npu	t pir	1														
	Input	0						Re	ead: p	oin s	et a	s inp	out													
	Output	1						Re	ead: p	oin s	et a	s ou	tput													
	Clear	1						W	/rite:	writ	ing a	a '1'	sets	pin	to i	npu	t; wr	iting	a '0)' ha	s no	eff	ect			



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCE
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
С	RW PIN2		Set as input pin 2
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
_		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
D	RW PIN3		Set as input pin 3
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
_		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
E	RW PIN4		Set as input pin 4
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
_	DIA DINE	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
F	RW PIN5	la acce.	Set as input pin 5
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
	DIAL DIALG	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
G	RW PIN6	la acce	Set as input pin 6
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
	DIA/ DIAI7	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Н	RW PIN7	la acce.	Set as input pin 7
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
	DIA/ DINIG	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
I	RW PIN8	lanut	Set as input pin 8
		Input	0 Read: pin set as input
		Output Clear	1 Read: pin set as output Write: writing a '1' sets pin to input; writing a '0' has no effect
J	RW PIN9	Clear	
J	NV PINS	Innut	Set as input pin 9 O Read: pin set as input
		Input Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
K	RW PIN10	Cicai	Set as input pin 10
K	NW FINIO	Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
L	RW PIN11	Cicai	Set as input pin 11
-	IVVV FINIT	Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
М	RW PIN12	Cicai	Set as input pin 12
141	NW THEE	Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	·
N	RW PIN13	Clear	
N	IVAA LIIATO	Innut	Set as input pin 13 O Read: pin set as input
		Input Output	1 Read: pin set as input 1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
0	RW PIN14	Cicdi	Set as input pin 14
J	WAN I HATH	Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
D	RW PIN15	Clear	
۲	VAN LIINTO	Innut	Set as input pin 15 O Read: pin set as input
		Input	
		Output	1 Read: pin set as output



	umbe	r		31 30	29 28	3 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
		000000				0	0 (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
_			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
Q	RW	PIN16		_					Set as input pin 16
			Input	0					Read: pin set as input
			Output	1					Read: pin set as output
_			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
R	RW	PIN17							Set as input pin 17
			Input	0					Read: pin set as input
			Output	1					Read: pin set as output
_	DVA	DINIAO	Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
S	KW	PIN18		•					Set as input pin 18
			Input	0					Read: pin set as input
			Output	1					Read: pin set as output
_	D\A/	DINIAG	Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
Т	RW	PIN19	la acce	0					Set as input pin 19
			Input	0					Read: pin set as input
			Output	1					Read: pin set as output
	D\A/	DINIZO	Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
U	KVV	PIN20	lanut	0					Set as input pin 20
			Input	0					Read: pin set as input
			Output	1					Read: pin set as output
V	D\A/	PIN21	Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect Set as input pin 21
V	IV V V	FINZI	Input	0					Read: pin set as input
			Output	1					Read: pin set as output
			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
W	R\M/	PIN22	Cicai	1					Set as input pin 22
**	11.00	1 11422	Input	0					Read: pin set as input
			Output	1					Read: pin set as output
			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
Х	RW	PIN23	Cicai	_					Set as input pin 23
		25	Input	0					Read: pin set as input
			Output	1					Read: pin set as output
			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
Υ	RW	PIN24		=					Set as input pin 24
-			Input	0					Read: pin set as input
			Output	1					Read: pin set as output
			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
Z	RW	PIN25							Set as input pin 25
			Input	0					Read: pin set as input
			Output	1					Read: pin set as output
			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
a	RW	PIN26							Set as input pin 26
			Input	0					Read: pin set as input
			Output	1					Read: pin set as output
			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
b	RW	PIN27							Set as input pin 27
			Input	0					Read: pin set as input
			Output	1					Read: pin set as output
			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
С	RW	PIN28							Set as input pin 28
-		-	Input	0					Read: pin set as input
			Output	1					Read: pin set as output
			Clear	1					Write: writing a '1' sets pin to input; writing a '0' has no effect
d	RW	PIN29		_					Set as input pin 29
_			Input	0					Read: pin set as input
			,	-					p



Bit number		31	30	29	28	27	26 2	25 2	24 2	23 2	22 2	1 2	20 1	.9 1	8 1	7 1	6 15	5 14	1 13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id		f	e	d	С	b	а	Z	Υ	X١	W١	/	U .	Т :	S F	2 (Q P	С	N	М	L	K	J	L	Н	G	F	E D	С	В	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0 ()	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0
Id RW Field	Value Id	Val	lue							Des	crip	tio	n																		
	Output	1							F	Rea	d: p	in s	set a	as o	utp	ut															
	Clear	1							١	Wri	te: v	vrit	ting	a ':	1' se	ets p	oin t	o ir	nput	; w	ritin	g a	'0' I	has	no	effe	ct				
e RW PIN30									9	Set	as ir	npu	ıt pi	n 3	0																
I	Input	0							F	Rea	d: p	in s	set a	as ii	npu	t															
	Output	1							F	Rea	d: p	in s	set a	as o	utp	ut															
	Clear	1							١	Wri	te: v	vrit	ting	a ':	1' se	ets p	oin t	o ir	nput	; w	ritin	g a	'0' I	nas	no	effe	ct				
f RW PIN31									9	Set	as ir	npu	ıt pi	n 3	1																
I	Input	0							F	Rea	d: p	in s	set a	as ii	npu	t															
	Output	1							F	Rea	d: p	in s	set a	as o	utp	ut															
	Clear	1							١	Wri	te: v	vrit	ting	a ':	1' se	ets p	oin t	o ir	nput	; w	ritin	g a	'0' I	nas	no	effe	ct				

20.3.8 LATCH

Address offset: 0x520

Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers

Id	umbe	er			311					4 2 2	1 11 1																2	1
																												2 1
Rese																												СВ
		0000000				0 0	0	0	0 0					0	0	0	0	0	0	0 (0	0	0	0 0	0	0	0 (0 0
ld		Field	Value Id	Va	ue						escrip															_		
A	RW	PIN0									atus							net	crite	eria	set I	n Pil	N_C	NFO.	EN:	ÞΕ		
				_							giste																	
			NotLatched	0							iteria					net												
			Latched	1							riteria																	
В	RW	PIN1									atus							net	crite	eria	set i	n Pil	N_C	NF1.	SENS	SE		
											giste																	
			NotLatched	0							riteria					net												
			Latched	1							riteria																	
С	RW	PIN2									atus							net	crite	eria	set i	n PII	N_C	NF2.	SENS	SE		
											giste																	
			NotLatched	0							riteria					net												
			Latched	1							riteria																	
D	RW	PIN3									atus							net	crite	eria	set i	n PII	N_C	NF3.:	SENS	SE		
											giste																	
			NotLatched	0							riteria					net												
			Latched	1							riteria																	
E	RW	PIN4									atus							net	crite	eria	set i	n PII	N_C	NF4.	SENS	SE		
											giste																	
			NotLatched	0							iteria					net												
			Latched	1							riteria																	
F	RW	PIN5									atus							net	crite	eria	set i	n PII	N_C	NF5.	SENS	SE		
										re	giste	r. W	rite	'1' t	to cl	ear												
			NotLatched	0						Cr	riteria	has	not	t be	en r	net												
			Latched	1							riteria																	
G	RW	PIN6									atus							net	crite	eria	set i	n Pli	N_C	NF6.	SENS	SE		
										re	giste	r. W	rite	'1' t	to cl	ear												
			NotLatched	0						Cr	riteria	has	not	t be	en r	net												
			Latched	1						Cr	iteria	has	bee	en r	net													
Н	RW	PIN7								St	atus	on w	vhet	ther	PIN	17 h	as n	net	crite	eria	set i	n Pli	N_C	NF7.	SENS	SE		
										re	giste	r. W	rite	'1' t	to cl	ear												
			NotLatched	0						Cr	riteria	has	not	t be	en r	net												
			Latched	1						Cr	riteria	has	bee	en r	net													
I	RW	PIN8								St	atus	on w	vhet	ther	PIN	18 h	as n	net	crite	eria	set i	n Pli	N_C	NF8.	SENS	SE		
										re	giste	r. W	rite	'1' t	to cl	ear												
			NotLatched	0						Cr	iteria	has	not	t be	en r	net												



Bit n	umbe	r		31 30	29 28	27 2	26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a Z	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	t 0x0	0000000		0 0	0 0	0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Latched	1					Criteria has been met
J	RW	PIN9							Status on whether PIN9 has met criteria set in PIN_CNF9.SENSE
									register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
K	RW	PIN10							Status on whether PIN10 has met criteria set in
			National and	0					PIN_CNF10.SENSE register. Write '1' to clear.
			NotLatched Latched	0					Criteria has not been met Criteria has been met
L	B/W	PIN11	Lattrieu	1					Status on whether PIN11 has met criteria set in
-	11.00	FINII							PIN_CNF11.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
М	RW	PIN12							Status on whether PIN12 has met criteria set in
									PIN_CNF12.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
N	RW	PIN13							Status on whether PIN13 has met criteria set in
									PIN_CNF13.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
0	RW	PIN14							Status on whether PIN14 has met criteria set in
									PIN_CNF14.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
Р	RW	PIN15							Status on whether PIN15 has met criteria set in
			Not atched	0					PIN_CNF15.SENSE register. Write '1' to clear. Criteria has not been met
			NotLatched Latched	0					Criteria has not been met
Q	RW	PIN16	Laterieu	1					Status on whether PIN16 has met criteria set in
٩		111110							PIN_CNF16.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
R	RW	PIN17							Status on whether PIN17 has met criteria set in
									PIN_CNF17.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
S	RW	PIN18							Status on whether PIN18 has met criteria set in
									PIN_CNF18.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
Т	RW	PIN19							Status on whether PIN19 has met criteria set in
									PIN_CNF19.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
	D\A/	DINIZO	Latched	1					Criteria has been met
U	IV VV	PIN20							Status on whether PIN20 has met criteria set in PIN_CNF20.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
V	RW	PIN21							Status on whether PIN21 has met criteria set in
									PIN_CNF21.SENSE register. Write '1' to clear.
			NotLatched	0					Criteria has not been met
			Latched	1					Criteria has been met
W	RW	PIN22							Status on whether PIN22 has met criteria set in
									PIN_CNF22.SENSE register. Write '1' to clear.



Bit	numbe	er		31 30	2 (9 2	28 2	27	26	25	24	2:	3 22 21	1 2	0 19	9 1	8 1	7 :	16	15	5 1	4	13 :	12	13	1 10) 9	8	7	(5 5	5 4	1 :	3 :	2	1
Id													(w v																							
Res	et 0x0	0000000		0 0	(0	0	0	0	0	0	0	0 0) (0 0)	0)	0	0	(0	0	0	0	0	0	0	0	() () () () ()	0
Id	RW	Field	Value Id	Value									escript																							
			NotLatched	0								Cı	riteria l	has	s no	t b	een	m	et																	
			Latched	1									riteria l																							
Х	RW	PIN23										St	tatus oi	n v	vhet	the	r Pl	N2	:3	has	s n	ne	t cri	ite	ria	set	: in									
												ΡI	IN_CNF	23	B.SEI	NS	E re	gis	te	r. \	۷r	ite	'1'	to	cl	ear										
			NotLatched	0									riteria l					-																		
			Latched	1									riteria l																							
Υ	RW	PIN24		_									tatus oi						4	ha	s n	ne	t cri	itei	ria	set	in									
													IN_CNF																							
			NotLatched	0									riteria l					-					_		٠.											
			Latched	1									riteria l						-																	
Z	RW/	PIN25	Euterieu	-									tatus oi						5	ha	s n	ne	t cri	itei	ria	set	in									
_		111423											IN_CNF																							
			NotLatched	0									riteria l					-							Ci	cui										
			Latched	1									riteria l						-																	
а	R\M/	PIN26	Laterica	-									tatus oi						6	ha	c n	nΔ	t cri	tοι	ria	cot	in									
а	11.00	FINZO											IN_CNF																							
			NotLatched	0									riteria l					-			, v i	110	. 1	ιυ	CI	Cai	•									
			Latched	1									riteria i						CL																	
h	D\A/	PIN27	Laterieu	1									tatus oi						7	hai	c n	na	t cri	ito	ria	cot	in									
D	IV V V	PIIV27																																		
			NotLatched	0									IN_CNF riteria l					-			/V I	ite	: 1	ιυ	CI	eai										
			Latched	1									riteria i riteria l						eı																	
	D\A/	PIN28	Laterieu	1																h a .			+ ori	+												
С	KVV	PIINZ8											tatus oi																							
			Note to be a	0									IN_CNF					-			/v r	ITE	. 1	το	CI	ear	•									
			NotLatched	0									riteria l						et																	
_	DVA	DINIZO	Latched	1									riteria l							L																
а	KW	PIN29											tatus oi																							
			No. of the Land	•									IN_CNF					-			۸vr	ΊŢ€	1.	το	CI	ear										
			NotLatched	0									riteria l						et																	
			Latched	1									riteria l																							
е	RW	PIN30											tatus oi																							
				_									IN_CNF					-			٧r	ite	1'	to	cl	ear										
			NotLatched	0									riteria l						et																	
			Latched	1									riteria l																							
f	RW	PIN31											tatus oi																							
													IN_CNF								٧r	ite	'1'	to	cl	ear	•									
			NotLatched	0									riteria l						et																	
			Latched	1								Cı	riteria l	has	s be	en	me	t																		

20.3.9 DETECTMODE

Address offset: 0x524

Select between default DETECT signal behaviour and LDETECT mode

Bit nu	ımbe	r		31	. 30	29	28	27	26 2	25 2	24 2	23 2	22 2	1 2	0 19	9 18	3 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2	1	0
d																																	Α
Rese	0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0
d	RW	Field	Value Id	Va	lue							Des	crip	tior	1																		
A	RW	DETECTMODE									9	Sele	ct b	etw	/eer	n de	fau	lt D	ETE	CT :	sign	al be	ehav	iou	and	d LC	ETE	СТ					
											r	noc	le																				
			Default	0							[DET	ECT	dir	ectl	у со	nne	ecte	d to	PI	N DI	TEC	T się	gnal	S								
			LDETECT	1							ι	Jse	the	lat	che	d LC	ETE	CT	beh	avi	our												
	d Reset d	d Reset 0x00 d RW	teset 0x00000000 d RW Field	d RW Field Value Id RW DETECTMODE Default	d Reset 0x00000000 0 0 d RW Field Value Id Value	RW DETECTMODE Default O	Reset 0x00000000	Reset 0x000000000	Reset 0x00000000	Reset 0x000000000	RW DETECTMODE Default Default Description Default Description Descript	RW DETECTMODE Default Defaul	RW DETECTMODE Default Defaul	RW DETECTMODE Default Default Description DETECT directly connection Description DETECT directly connection Description DETECT directly connection Description Description DETECT directly connection Description DETECT directly connection Description DETECT directly connection Description Description DETECT directly connection Description Description DETECT directly connection Description DETECT directly connection Description Description DETECT directly connection Description Descript	RW DETECTMODE Default Default Default Default Description DETECT directly connected Description DETECT directly connected Description DETECT directly connected Description Description DETECT directly connected Description DETECT directly connected Description Description DETECT directly connected Description DETECT directly connected Description Description	RW DETECTMODE Default Defaul	RW DETECTMODE Default Defaul	RW DETECTMODE Default Defaul	RW DETECTMODE Default Default Default Default Detect to PIN DETECT	Reset 0x000000000	Reset 0x000000000	Reset 0x000000000	RW DETECTMODE Default DETECT directly connected to PIN DETECT signals	Reset 0x000000000	RW DETECTMODE Default Defaul	Reset 0x00000000000000000000000000000000000	Reset 0x00000000000000000000000000000000000	Reset 0x00000000000000000000000000000000000	Reset 0x00000000000000000000000000000000000				



20.3.10 PIN_CNF[0]

Address offset: 0x700

Configuration of GPIO pins

Bit r	umb	er		31 30	29	28	27	26 2	25 2	24 2	23 :	22 21	20	19	18	17	16	15	14	13 :	L2 1	.1 10) 9	8	7	6	5	4	3	2	1 0
Id																Ε	Ε					D) [D					С	C I	ВА
Res	et OxC	00000002		0 0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 :	1 (
Id	RW	Field	Value Id	Value	•					0	Des	scriptio	on																		
Α	RW	DIR								F	Pin	direct	ion	ı. Saı	ne	phy	/sic	al r	egis	ter	as [DIR r	egi	ster							
			Input	0						C	Cor	nfigure	pi	n as	an	inp	ut p	in													
			Output	1						C	Cor	nfigure	pi	n as	an	out	put	pir	n												
В	RW	INPUT								C	Cor	nnect o	or c	lisco	nne	ect i	inp	ut b	ouff	er											
			Connect	0						C	Cor	nnect i	npı	ut bı	ıffe	r															
			Disconnect	1						0	Disc	conne	ct i	nput	bu	ıffeı	•														
С	RW	PULL								P	Pull	l confi	gur	atio	n																
			Disabled	0						Ν	١o	pull																			
			Pulldown	1						P	Pull	l dowr	or	n pin																	
			Pullup	3						F	Pull	l up or	n pi	n																	
D	RW	DRIVE								0	Dri	ve con	fig	urati	on																
			S0S1	0						S	taı	ndard	'0',	, stai	nda	rd '	1'														
			H0S1	1						H	lig	h drive	e '0	', sta	nd	ard	'1'														
			S0H1	2						S	itai	ndard	'0',	, higl	n dr	rive	'1'														
			H0H1	3						H	lig	h drive	e '0	', hi	gh '	driv	e '1	L'''													
			DOS1	4						0	Disc	conne	ct '	0' st	and	lard	'1'	(nc	orm	ally	use	d fo	r w	irec	l-or						
										C	on	nectio	ns)																	
			D0H1	5								conne nectic			gh	driv	/e '	1' (ı	nor	mal	ly u	sed	for	wire	ed-c	or					
			SOD1	6								ndard mectic			on	nec	t '1	' (n	orn	nally	us (ed fo	or v	vire	d-ar	nd					
			H0D1	7							_	h drive			coı	nne	ct '	1' (ı	nor	mal	ly u	sed	for	wire	ed-a	ınd					
E	RW	SENSE										sensir		•	nan	ism															
			Disabled	0								abled	-																		
			High	2						S	en	se for	hig	gh le	vel																
			Low	3								se for		-																	

20.3.11 PIN_CNF[1]

Address offset: 0x704

Di+ r	numbe	or.		21	30 2	ດ າ	0 7	7 2	ב אם	: 2.	1 22	22	21	20	10	10	17	16	10	11	10 1	2 1	1 10		8	7	6	5	Δ	3 2	1	0
	iuiiibe	: 1		31	30 2	<i>3</i>	.0 2 .	/ 21	0 23) 24	4 23	22	21	20	19	10			13	14	15 1	2 1.			Ŭ	′	O	J		_	1	U
Id																	Е	Ε					D	D	D					C C	В	Α
Res	et OxO	0000002		0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	1	0
Id	RW	Field	Value Id	Va	lue						De	scri	iptic	on																		
Α	RW	DIR									Pir	n dir	recti	ion.	Saı	ne	ph	ysic	al r	egis	ter	as D	IR r	egis	ter							
			Input	0							Co	nfig	gure	pir	as	an	inp	ut p	oin													
			Output	1							Co	nfig	gure	pir	as	an	out	put	t pir	า												
В	RW	INPUT									Co	nne	ect o	r d	isco	nn	ect	inp	ut k	ouff	er											
			Connect	0							Co	nne	ect ii	npu	t bu	ıffe	er															
			Disconnect	1							Dis	cor	nnec	t ir	put	bu	ıffe	r														
С	RW	PULL									Pu	II co	onfig	gura	atio	n																
			Disabled	0							No	pu	II																			
			Pulldown	1							Pu	II do	own	on	pin																	
			Pullup	3							Pu	ll up	o on	pir	ı																	
D	RW	DRIVE									Dr	ive	conf	figu	rati	on																
			S0S1	0							Sta	anda	ard	'0',	star	nda	rd	'1'														
			H0S1	1							Hig	gh d	Irive	'0'	, sta	and	ard	'1'														



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E DDD CCBA
Reset 0x00000002		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	S0H1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
			connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
			connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
			connections)
E RW SENSE			Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

20.3.12 PIN_CNF[2]

Address offset: 0x708

Configuration of GPIO pins

Bit n	umba			21.2	0.20	9 28 2	77 20	: זר	24	าว	22.2	1 2	0 1	0.10	17	16	10	11	10 1	າ 1	1 1/) 9	8	7	6	5	1 3	2	1	0
Id Bit ni	umbe	r		31 3	0 25	9 28 2	27 26	25	24 .	23 .	22 2	1 2	.0 1	.9 18		E 10	15	14	13 1	2 1			8 D	/	ь	5		. C	_	Ē
	• ^~^	0000002				0		_	_	_							_	_						_	_	^				
		Field	Value Id	Valu		, 0	0 0	U			scrip			U U	U	U	U	U	0 (, ,	, ,	U	U	U	U	U	0 0	U	_	U
Id A	RW		value id	valu	е						dire			Cam	o nh	wei	al r	ogi	tor	nc [ND r	ogi	tor							
A	NVV	DIK	Input	0							nfigu							egi	iei e	15 L	ו אוע	egi	iei							
			Output	1							nfigu							n												
В	D\A/	INPUT	Output								nnec					•	•		or											
Ь	NVV	INPOT	Connect	0							nnec					. 1111	Juti	Juli	eı											
				1																										
_	D\A/	PULL	Disconnect	1							conr				Julie	21														
С	KVV	PULL	Disabled	0							l cor	_	urai	tion																
				0							pull																			
			Pulldown	1							ll dov			pin																
-	D) 4./	DD11/5	Pullup	3							l up																			
D	KW	DRIVE	5054								ve co		_			141														
			SOS1	0							ındaı 																			
			H0S1	1							h dr																			
			SOH1	2							ındaı 			-																
			H0H1	3						_	sh dr			_																
			D0S1	4							conr			star	ıdar	d '1	' (n	orm	ally	use	d fo	r w	ired [.]	-or						
											nnec		•																	
			D0H1	5						Disc	conr	nect	'0'	, hig	h dr	ive	'1' (nor	mall	y u	sed 1	for	wire	d-o	r					
											nnec		•																	
			SOD1	6					:	Stai	ndaı	'd 'C)'. d	lisco	nne	ct ':	1' (n	orn	nally	us	ed fo	or w	ired	-an	d					
										con	nnec	tion	ıs)																	
			H0D1	7						Hig	sh dr	ive '	'0',	disc	onn	ect	'1' (nor	mall	y u	sed	for	wire	d-a	nd					
										con	nnec	tion	ıs)																	
E	RW	SENSE								Pin	sen	sing	me	echa	nisn	n														
			Disabled	0						Disa	able	d																		
			High	2					:	Sen	nse f	or h	igh	leve	el															
			Low	3					:	Sen	nse f	or lo	wc	leve	I															

20.3.13 PIN_CNF[3]

Address offset: 0x70C



Configuration of GPIO pins

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E DDD CCBA
Reset 0x00000002		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value	Description
A RW DIR			Pin direction. Same physical register as DIR register
	Input	0	Configure pin as an input pin
	Output	1	Configure pin as an output pin
B RW INPUT			Connect or disconnect input buffer
	Connect	0	Connect input buffer
	Disconnect	1	Disconnect input buffer
C RW PULL			Pull configuration
	Disabled	0	No pull
	Pulldown	1	Pull down on pin
	Pullup	3	Pull up on pin
D RW DRIVE			Drive configuration
	S0S1	0	Standard '0', standard '1'
	H0S1	1	High drive '0', standard '1'
	S0H1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
			connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
			connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
			connections)
E RW SENSE			Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

20.3.14 PIN_CNF[4]

Address offset: 0x710

Di+ .	numbe			21 20 20 20 27 20 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	iumbe	21		31 30 29 28 27 26 25 24	
Id					E E D D D C C B A
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E E D D D C C B A
Reset 0x00000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
			connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
			connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
			connections)
E RW SENSE			Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

20.3.15 PIN_CNF[5]

Address offset: 0x714

Configuration of GPIO pins

Reset 0x000000002 New Field Value Value	Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
de RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin A RW INPUT Connect Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer C RW PULL Disconnect 1 Disconnect input buffer D Input Disabled 0 No pull down on pin Pull down on pin Pullup 3 Pull up on pin Pull configuration D RW DRIVE SoS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 Disconnect '0', high drive '1' HOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) D DH1 5 Standard '0', disconnect '1' (normally used for wired-and connections) FW SENSE HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) FIN sensing mechanism Disabled Disabl	Id		E E DDD CCBA
RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin Connect of disconnect input buffer Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer CRW PULL Disabled 0 No pull Pulldown 1 Pull own on pin Pullup 3 Pull up on pin Pullup 3 Pull up on pin Pullup 1 Disconfiguration Drive configuration OR RW DRIVE SOS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' Disconnect '0', high drive '1' HOH1 5 Disconnect '0', high drive '1' Disconnect '0', high drive '1' HOH1 5 Disconnect '0', high drive '1' HOH1 5 Disconnect '0', high drive '1' HOH1 5 Disconnect '0', high drive '1' HOH1 7 High drive '0', high drive '1' (normally used for wired-or connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) FOR TRW SENSE Pin sensing mechanism Disabled High 0 Disabled High 2 Sense for high level	Reset 0x00000002		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Input 0 Configure pin as an input pin Output 1 Configure pin as an input pin Output 1 Configure pin as an output pin Connect input buffer Connect input buffer Disconnect input buffer Disconnect input buffer Pull configuration RW PULL Disabled 0 No pull Pull own on pin Pullup 3 Pull up on pin Pullup pon pin Pullup Disconnect 1 High drive '0', standard '1' Soh1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' (normally used for wired-or connections) DOH1 5 DISCONNECT O', high drive '1' (normally used for wired-or connections) FRW SENSE FRW SENSE Pin sensing mechanism Connections) Disabled 0 Disabled 1 Disabled 1 Disabled For high level	Id RW Field	Value Id	Value Description
RW INPUT Connect Conn	A RW DIR		Pin direction. Same physical register as DIR register
RW INPUT Connect Co		Input	0 Configure pin as an input pin
Connect Disconnect 1 Disconnect input buffer Pull configuration Pull Configuration Pull Configuration No pull Pull Configuration No pull Pull Configuration Pull Up on pin Pull Up on pin Drive configuration Sos1 0 Standard '0', standard '1' H051 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 High drive '0', high drive '1' Dos1 4 Disconnect '0', high drive '1' DOS1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) DOH1 5 Standard '0'. disconnect '1' (normally used for wired-or connections) Find Standard '0'. disconnect '1' (normally used for wired-and connections) Find Sense Pin sensing mechanism Disabled High 0 Disabled High 2 Sense for high level		Output	1 Configure pin as an output pin
Disconnect RW PULL Disabled Disab	B RW INPUT		Connect or disconnect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Pullup 3 Pull up on pin Pullup 1 Pull down on pin Pullup 1 Pull down on pin Pullup 0 Pull up on pin Pullup 0 Standard '1' Pullu		Connect	0 Connect input buffer
Disabled 0 No pull Pull down on pin Pull up no pin Pull up on pin Pull up on pin Drive configuration Standard '0', standard '1' H0S1 1 High drive '0', standard '1' H0H1 3 High drive '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DDH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) RW SENSE RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level		Disconnect	1 Disconnect input buffer
Pulldown 1 Pullup 3 Pull down on pin Pullup 3 Pull up on pin Pullup 5 Pull up on pin Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) RW SENSE Disabled 0 Disabled High 2 Sense for high level	C RW PULL		Pull configuration
Pullup 3 Pull up on pin Pullup 5 Pullup on pin Drive configuration Sos1 0 Standard '0', standard '1' HoS1 1 High drive '0', standard '1' SoH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high 'drive '1'' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level		Disabled	0 No pull
Drive configuration SUBSI 0 Standard '0', standard '1' HUS1 1 High drive '0', standard '1' SUBSI 2 Standard '0', high drive '1' HUH1 3 High drive '0', high 'drive '1' DUS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DUH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SUD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HUD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level		Pulldown	1 Pull down on pin
S0S1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1'' D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level		Pullup	3 Pull up on pin
H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1" D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled High 2 Sense for high level	D RW DRIVE		Drive configuration
SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1" DDS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DDH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled High 2 Sense for high level		S0S1	0 Standard '0', standard '1'
H0H1 3 High drive '0', high 'drive '1" DDS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DDH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SDD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled High Sense for high level		H0S1	1 High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level		S0H1	2 Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High Sense for high level		H0H1	3 High drive '0', high 'drive '1"
D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled High 2 Sense for high level		DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled O Disabled High 2 Sense for high level			connections)
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled High 2 Sense for high level		D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
connections) High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled High 2 Sense for high level			connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level		SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
connections) E RW SENSE Disabled High 2 Sense for high level			connections)
RW SENSE Pin sensing mechanism Disabled Disabled High 2 Sense for high level		H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled High 2 Sense for high level			connections)
High 2 Sense for high level	E RW SENSE		Pin sensing mechanism
·		Disabled	0 Disabled
Low 3 Sense for low level		High	2 Sense for high level
		Low	3 Sense for low level

20.3.16 PIN_CNF[6]

Address offset: 0x718



Reset 0x00000002 O 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin Configure pin as an output pin Connect or disconnect input buffer Connect 0 Connect input buffer Connect 1 Disconnect input buffer C RW PULL Pull configuration Disabled 0 No pull Pulldown 1 Pull down on pin Pull up on pin Pull up on pin	1 0
A RW DIR Input O Configure pin as an input pin Output 1 Configure pin as an output pin Connect or disconnect input buffer Connect Disconnect Pull configuration No pull Pulldown 1 Pull down on pin Pull up on pin	
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 1 Disconnect input buffer C RW PULL Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
B RW INPUT Connect or disconnect input buffer Connect Disconnect D	
B RW INPUT Connect or disconnect input buffer Connect of Disconnect input buffer Disconnect of Disconnect input buffer Disconnect input buffer Pull configuration No pull Pull down on pin Pull up on pin	
Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Disconnect 1 Disconnect input buffer C RW PULL Disabled Disabled Pull down on pin Pullup 3 Pull up on pin	
C RW PULL Pull configuration Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	
H0S1 1 High drive '0', standard '1'	
SOH1 2 Standard '0', high drive '1'	
H0H1 3 High drive '0', high 'drive '1"	
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or	
connections)	
D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or	
connections)	
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and	
connections)	
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and	
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	

20.3.17 PIN_CNF[7]

Address offset: 0x71C Configuration of GPIO pins

numb	er		31	. 30	29	28	27	26 2	25 :	24	23 2	22	21 :	20	19 1	18 :	17 :	16	15 1	.4 :	13 :	12 :	l1 1	.0 9	8	7	6	5	4	3	2 :	1 0
																	Е	E					1) C	D					С	C E	3 A
et 0x(00000002		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 1	1 0
RW	Field	Value Id	Va	lue							Des	cri	ptio	n																		
RW	DIR										Pin	dir	ecti	on.	Sar	ne	phy	sic	al re	gis	ter	as	DIR	regi	ster							
		Input	0								Con	fig	ure	pin	as	an i	inpı	ut p	in													
		Output	1								Con	fig	ure	pin	as	an (out	put	pin													
RW	INPUT										Con	ne	ct o	r di	sco	nne	ect i	npı	ut b	uff	er											
		Connect	0								Con	ne	ct ir	npu	t bu	ffe	r															
		Disconnect	1								Disc	on	nec	t in	put	bu	ffer															
RW	PULL										Pull	со	nfig	gura	tioi	1																
		Disabled	0								No p	pul	I																			
		Pulldown	1								Pull	do	wn	on	pin																	
		Pullup	3								Pull	up	on	pir	1																	
RW	DRIVE										Driv	e c	onf	igu	rati	on																
		S0S1	0							:	Star	nda	rd '	0',	star	ıda	rd '	1'														
		H0S1	1								High	n d	rive	'0'	, sta	nd	ard	'1'														
		S0H1	2							:	Star	nda	rd '	0',	high	dr	ive	'1'														
		H0H1	3								High	n di	rive	'0'	, hig	h 'd	driv	e '1	L''													
		DOS1	4								Disc	on	nec	t '0	' sta	nd	ard	'1'	(no	rm	ally	use	ed f	or w	ired	l-or						
											con	nor	rtio	ns)																		
	RW RW	RW Field RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect RW PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Input O Output I Input Output I Input Id Input Id Input Id Input Id Input Id Input Id Id Id Id Id Id Id I	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 THE SOH1 2 HOH1 3 TO T	RW Field Value Id Input O Output I I ID	RW Field Value Id Val	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect Disconnect 1 RW PULL PULL Disabled O Pulldown 1 Pullup 3 RW DRIVE SOS1 O HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 DOS1 4	RW Field Value Id Value RW DIR Input Output 1 Connect Disconnect Disconnect Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 SOS1 HOS1 A TO SO TO	RW Field Value Id Value	RW Field Value Id Val	RW Field Value Id Value	RW Field Value Martin Pin direction. San Pin direction. San	RW Field Value Id Value Valu	RW DIR	RW Field Value Market Pin direction. Same physical	RW Field Value Id Value Pin direction. Same physical reference Pin d	RW Field Value Id Value Pin direction. Same physical register	RW Field Value Id Value Id Value Id Description Pin direction. Same physical register	RW Field Value Id Value Valu	RW Field Value Id Id Id Id Id Id Id I	RW Field	RW Field Value Id Value	RW Field Value Id Value Id Pin direction. Same physical register as DIR regist	RW Field Value Id Val	RW Field Value Id Value	RW Field Value Id Value Valu	RW Field Value Id Value I	RW Field Value Id Val



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E D D D C C B A
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.18 PIN_CNF[8]

Address offset: 0x720

Configuration of GPIO pins

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.19 PIN_CNF[9]

Address offset: 0x724



Bit r	numbe	er		31 3	0 29	9 28	27 2	26 2	5 24	1 23	3 22	21 2	0 1	9 18	17	16	15	14 1	3 12	11	10	9	8	7 (5 5	5 4	3	2	1 0
Id															Ε	Ε					D	D	D				С	С	ВА
Rese	et OxC	0000002		0	0 0	0	0	0 (0 0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	1 0
Id	RW	Field	Value Id	Valu	ie					De	escri	otior	1																
Α	RW	DIR								Pir	n dir	ectic	n. S	Same	ph	ysic	al r	egist	er as	s DI	R re	gist	er						
			Input	0						Co	onfig	ure p	oin a	as an	inp	ut p	oin												
			Output	1						Co	onfig	ure p	oin a	as an	ou	tput	t pir	ı											
В	RW	INPUT								Co	onne	ct or	dis	conr	ect	inp	ut k	uffe	r										
			Connect	0						Co	onne	ct in	put	buff	er														
			Disconnect	1						Di	iscon	nect	inp	ut b	uffe	r													
С	RW	PULL								Pu	ıll co	nfigu	ırat	ion															
			Disabled	0						No	o pul	I																	
			Pulldown	1						Pu	ıll do	wn d	on p	oin															
			Pullup	3						Pu	ıll up	on p	pin																
D	RW	DRIVE								Dr	rive o	onfi	gura	ation	1														
			S0S1	0						Sta	anda	rd 'C)', st	tand	ard	'1'													
			H0S1	1						Hi	igh d	rive '	'0', s	stan	dard	i '1'													
			S0H1	2						Sta	anda	rd 'C)', h	igh c	lrive	'1'													
			H0H1	3						Hi	igh d	rive '	'0', I	high	'dri	ve '	1''												
			DOS1	4						Di	iscon	nect	'0'	stan	dar	d '1'	(no	rma	lly u	sed	for	wir	ed-d	or					
										со	nne	ction	s)																
			D0H1	5						Di	iscon	nect	'0',	, high	n dri	ve '	1' (norm	ally	use	d fo	or w	ired	-or					
										со	nne	tion	s)																
			S0D1	6						Sta	anda	rd 'C)'. d	iscor	nne	t '1	' (n	orma	illy u	used	d for	wii	ed-	and					
										со	nne	ction	s)																
			H0D1	7						Hi	igh d	rive '	'0', d	disco	nne	ect '	1' (norm	ally	use	ed fo	or w	irec	l-an	d				
										со	nne	tion	s)																
Ε	RW	SENSE								Pir	n ser	sing	me	echai	nisn	1													
			Disabled	0						Di	isable	ed																	
			High	2						Se	ense	for h	igh	leve	I														
			Low	3						Se	ense	for Id	ow I	level															

20.3.20 PIN_CNF[10]

Address offset: 0x728 Configuration of GPIO pins

СВА
0 1 0



Bit number		31 30	29 2	28 2	7 2	6 25	5 24	23 2	2 21	20	19 1	8 17	7 16	15	14 1	3 12	11	10	9	8 7	6	5	4	3 2	1	0
Id												Ε	Ε					D	D	D				C C	В	Α
Reset 0x00000002		0 0	0	0 0	0	0	0	0 0	0	0	0 (0	0	0	0 (0	0	0	0	0 0	0	0	0	0 0	1	0
Id RW Field V	alue Id	Value						Desc	riptio	on																
D	0H1	5						Disco	onne	ct '0)', hig	gh di	rive	'1' (norn	nally	use	d fo	wi	red-	or					
								conn	ectio	ns)																
SC	0D1	6						Stan	dard	'0'.	disco	onne	ect '	1' (n	orm	ally ι	ısed	for	wir	ed-a	nd					
								conn	ectio	ns)																
H	0D1	7						High	drive	e '0'	, disc	conn	ect	'1' (norn	nally	use	d fo	r wi	red-	and					
								conn	ectio	ns)																
E RW SENSE								Pin s	ensir	ıg m	nech	anisı	m													
Di	isabled	0						Disal	oled																	
Hi	igh	2						Sens	e for	hig	h lev	el														
Lo	OW	3						Sens	e for	low	leve	el														

20.3.21 PIN_CNF[11]

Address offset: 0x72C

Configuration of GPIO pins

Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d			E E D D D C C B A
Reset 0x00000002		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
d RW Field	Value Id	Value	Description
A RW DIR			Pin direction. Same physical register as DIR register
	Input	0	Configure pin as an input pin
	Output	1	Configure pin as an output pin
B RW INPUT			Connect or disconnect input buffer
	Connect	0	Connect input buffer
	Disconnect	1	Disconnect input buffer
C RW PULL			Pull configuration
	Disabled	0	No pull
	Pulldown	1	Pull down on pin
	Pullup	3	Pull up on pin
D RW DRIVE			Drive configuration
	S0S1	0	Standard '0', standard '1'
	H0S1	1	High drive '0', standard '1'
	SOH1	2	Standard '0', high drive '1'
	H0H1	3	High drive '0', high 'drive '1"
	DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
			connections)
	D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
	SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
			connections)
	H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
			connections)
E RW SENSE			Pin sensing mechanism
	Disabled	0	Disabled
	High	2	Sense for high level
	Low	3	Sense for low level

20.3.22 PIN_CNF[12]

Address offset: 0x730 Configuration of GPIO pins



Reset 0x00000002 O 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin Configure pin as an output pin Connect or disconnect input buffer Connect 0 Connect input buffer Connect 1 Disconnect input buffer C RW PULL Pull configuration Disabled 0 No pull Pulldown 1 Pull down on pin Pull up on pin Pull up on pin	1 0
A RW DIR Input O Configure pin as an input pin Output 1 Configure pin as an output pin Connect or disconnect input buffer Connect Disconnect Pull configuration No pull Pulldown 1 Pull down on pin Pull up on pin	
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 1 Disconnect input buffer C RW PULL Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
B RW INPUT Connect or disconnect input buffer Connect Disconnect D	
B RW INPUT Connect or disconnect input buffer Connect of Disconnect input buffer Disconnect of Disconnect input buffer Disconnect input buffer Pull configuration No pull Pull down on pin Pull up on pin	
Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Disconnect 1 Disconnect input buffer C RW PULL Disabled Disabled Pull down on pin Pullup 3 Pull up on pin	
C RW PULL Pull configuration Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	
H0S1 1 High drive '0', standard '1'	
SOH1 2 Standard '0', high drive '1'	
H0H1 3 High drive '0', high 'drive '1"	
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or	
connections)	
D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or	
connections)	
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and	
connections)	
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and	
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	

20.3.23 PIN_CNF[13]

Address offset: 0x734 Configuration of GPIO pins

Bit r	numb	er		31	30	29	28 :	27 :	26 2	5 2	4 23	22	2 21	20	19	18	17	16	15	14	13	L2 1	1 1	0 9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					[D	D					СС	: В	Α
Res	et OxC	00000002		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0) 1	. 0
Id	RW	Field	Value Id	Va	lue						De	esci	ripti	on																		
Α	RW	DIR									Pir	n di	irec	tior	ı. Sa	me	ph	ıysi	al r	egi	ster	as (DIR I	regis	ter							
			Input	0							Co	nfi	gure	e pi	n as	an	in	out	pin													
			Output	1							Co	nfi	gure	e pi	n as	an	ou	tpu	t pi	n												
В	RW	INPUT									Co	nn	ect	or c	disc	onn	ect	inp	ut	buf	er											
			Connect	0							Co	nn	ect	inp	ut b	uff	er															
			Disconnect	1							Dis	sco	nne	ct i	npu	t b	uffe	er														
С	RW	PULL									Pu	III c	onfi	igur	atio	n																
			Disabled	0							No	рι	الد																			
			Pulldown	1							Pu	III d	low	n oı	n pii	n																
			Pullup	3							Pu	ıll u	ро	n pi	in																	
D	RW	DRIVE									Dr	ive	cor	nfig	urat	ion	1															
			S0S1	0							Sta	and	lard	'0' ,	, sta	nda	ard	'1'														
			H0S1	1							Hi	gh	driv	e '0)', st	and	dar	d '1	'													
			S0H1	2							Sta	and	lard	'0' ,	, hig	h d	Iriv	e '1	1													
			H0H1	3							Hi	gh	driv	e '0)', hi	igh	'dr	ve '	1"													
			DOS1	4							Dis	sco	nne	ct '	0' st	tan	dar	d '1	' (n	orm	ally	use	d fo	or w	red	-or						
											со	nn	ecti	ons)																	



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.24 PIN_CNF[14]

Address offset: 0x738

Configuration of GPIO pins

Bit nur	mbe	r		31	30	29 2	28 2	7 26	5 25	5 24	23	3 22	21 2	20 1	19 1	8 1	7 1	6 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5 4	4 3	2	1	С
Id																ı	Ξ Ε						D	D	D				C	: C	В	1
Reset (0x0	0000002		0	0	0	0 (0 0	0	0	0	0	0 (0	0 () (0) (0 0) (0	0	0	0	0	0	0	0	0	0	1	(
ld R	RW	Field	Value Id	Va	lue						De	escri	otio	n																		
A R	RW	DIR									Pir	n dir	ectio	on.	San	ne p	hys	ica	l re	gist	er a	s D	IR re	egist	ter							
			Input	0							Со	onfig	ıre į	pin	as a	ın iı	npu	t pi	in													
			Output	1							Со	onfig	ıre į	pin	as a	ın c	utp	ut	pin													
B R	RW	INPUT									Со	nne	ct or	r di:	scor	ne	ct ir	npu	t bu	ıffe	r											
			Connect	0							Со	nne	ct in	put	t bu	ffer																
			Disconnect	1							Dis	scon	nect	t in	put	buf	fer															
C R	RW	PULL									Pu	ıll co	nfig	ura	tion																	
			Disabled	0							No	o pul	l																			
			Pulldown	1							Pu	ıll do	wn (on	pin																	
			Pullup	3							Pu	ıll up	on	pin																		
D R	RW	DRIVE									Dri	ive c	onfi	igui	ratio	n																
			SOS1	0							Sta	anda	rd '()', s	stan	dar	d '1															
			H0S1	1							Hig	gh d	rive	'0',	sta	nda	rd '	1'														
			S0H1	2							Sta	anda	rd '()', ł	nigh	dri	ve '	1'														
			H0H1	3							Hig	gh d	rive	'0',	hig	h 'd	rive	· '1'	"													
			DOS1	4							Dis	scon	nect	t '0'	' sta	nda	ard	'1' ((nor	ma	lly ι	use	d fo	wii	red-	or						
											со	nne	tion	ns)																		
			D0H1	5							Dis	scon	nect	t '0'	', hig	gh c	iriv	e '1	' (n	orn	nally	/ us	ed f	or v	vired	d-or						
											со	nne	tion	ns)																		
			SOD1	6							Sta	anda	rd '()'. c	disco	onn	ect	'1'	(no	rma	ally	use	d fo	r wi	red-	-and	t					
											со	nne	tion	ns)																		
			H0D1	7							Hig	gh d	rive	'0',	disc	con	nec	t '1	' (n	orn	nally	us us	ed f	or v	vired	d-ar	nd					
											СО	nne	tion	ns)																		
E R	RW	SENSE									Pir	n ser	sing	g m	ech	anis	sm															
			Disabled	0							Dis	sable	ed																			
			High	2							Se	nse	for h	nigh	ı lev	el																
			Low	3							Se	nse	for le	ow	leve	el																

20.3.25 PIN_CNF[15]

Address offset: 0x73C Configuration of GPIO pins



Reset 0x00000002 O 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin Configure pin as an output pin Connect or disconnect input buffer Connect 0 Connect input buffer Connect 1 Disconnect input buffer C RW PULL Pull configuration Disabled 0 No pull Pulldown 1 Pull down on pin Pull up on pin Pull up on pin	1 0
A RW DIR Input O Configure pin as an input pin Output 1 Configure pin as an output pin Connect or disconnect input buffer Connect Disconnect Pull configuration No pull Pulldown 1 Pull down on pin Pull up on pin	
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 1 Disconnect input buffer C RW PULL Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
B RW INPUT Connect or disconnect input buffer Connect Disconnect D	
B RW INPUT Connect or disconnect input buffer Connect of Disconnect input buffer Disconnect of Disconnect input buffer Disconnect input buffer Pull configuration No pull Pull down on pin Pull up on pin	
Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Disconnect 1 Disconnect input buffer C RW PULL Disabled Disabled Pull down on pin Pullup 3 Pull up on pin	
C RW PULL Pull configuration Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Pulldown 1 Pull down on pin Pullup 3 Pull up on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	
H0S1 1 High drive '0', standard '1'	
SOH1 2 Standard '0', high drive '1'	
H0H1 3 High drive '0', high 'drive '1"	
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or	
connections)	
D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or	
connections)	
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and	
connections)	
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and	
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	

20.3.26 PIN_CNF[16]

Address offset: 0x740 Configuration of GPIO pins

Bit r	numb	er		31	30	29	28 :	27 :	26 2	5 2	4 23	22	2 21	20	19	18	17	16	15	14	13	L2 1	1 1	0 9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					[D	D					СС	: В	Α
Res	et OxC	00000002		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0) 1	. 0
Id	RW	Field	Value Id	Va	lue						De	esci	ripti	on																		
Α	RW	DIR									Pir	n di	irec	tior	ı. Sa	me	ph	ıysi	al r	egi	ster	as (DIR I	regis	ter							
			Input	0							Co	nfi	gure	e pi	n as	an	in	out	pin													
			Output	1							Co	nfi	gure	e pi	n as	an	ou	tpu	t pi	n												
В	RW	INPUT									Co	nn	ect	or c	disc	onn	ect	inp	ut	buf	er											
			Connect	0							Co	nn	ect	inp	ut b	uff	er															
			Disconnect	1							Dis	sco	nne	ct i	npu	t b	uffe	er														
С	RW	PULL									Pu	III c	onfi	igur	atio	n																
			Disabled	0							No	рι	الد																			
			Pulldown	1							Pu	III d	low	n oı	n pii	n																
			Pullup	3							Pu	ıll u	ро	n pi	in																	
D	RW	DRIVE									Dr	ive	cor	nfig	urat	ion	1															
			S0S1	0							Sta	and	lard	'0' ,	, sta	nda	ard	'1'														
			H0S1	1							Hi	gh	driv	e '0)', st	and	dar	d '1	'													
			S0H1	2							Sta	and	lard	'0' ,	, hig	h d	Iriv	e '1	1													
			H0H1	3							Hi	gh	driv	e '0)', hi	igh	'dr	ve '	1"													
			DOS1	4							Dis	sco	nne	ct '	0' st	tan	dar	d '1	' (n	orm	ally	use	d fo	or w	red	-or						
											со	nn	ecti	ons)																	



Bit number		31 3	0 29	28	27	26	25	24 2	23 2:	2 21	20	19	18	17	16 :	15 1	4 1	3 12	11	10	9	8	7	6 5	5 4	3	2	1	0
Id														Е	Е					D	D	D				С	С	В	Α
Reset 0x00000002		0 0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0 ()	0 (0	0	0	1	0
ld RW Field	Value Id	Valu	e					ı	Desc	ripti	on																		
	D0H1	5						ı	Disco	onne	ct '(0', h	igh	driv	ve ':	1' (n	orm	ally	use	d fo	r w	ired	-or						
								(conn	nectio	ons))																	
	SOD1	6						9	Stan	dard	'0'.	dis	con	nec	t '1'	' (nc	rma	ally u	ısed	for	niw	ed-	anc	ı					
								(conn	nectio	ons))																	
	H0D1	7						ŀ	High	driv	e '0	', di	sco	nne	ct ':	1' (n	orm	ally	use	d fo	r w	ired	-an	d					
								(conn	nectio	ons))																	
E RW SENSE								ı	Pin s	ensi	ng n	necl	nan	ism															
	Disabled	0						[Disab	bled																			
	High	2						9	Sens	e for	hig	gh le	vel																
	Low	3						9	Sens	e for	· lov	v lev	/el																

20.3.27 PIN_CNF[17]

Address offset: 0x744

Configuration of GPIO pins

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E D D D C C B A
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and connections)
E	RW	SENSE			Pin sensing mechanism
-			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level
			== ::	-	

20.3.28 PIN_CNF[18]

Address offset: 0x748



Reset 000000002	Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW DIR Input 0 Configure pin as an input pin B RW INPUT Connect Connect or disconnect input buffer C Connect Disconnect Disconnect input buffer Disconnect Disconnect input buffer Pull configuration C RW PUL Pull on Pull down on pin Pull up on pin Pull up on pin DISCONNECT SOS1 O Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' HOH1 3 High drive '0', high drive '1' (normally used for wired-or connections) DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) FW SDD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) FW FW SENSE High drive '0', disconnect '1' (normally used for wired-and connections)	Id					E E DDD CCBA
A RW DIR	Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Input	Id	RW	Field	Value Id	Value	Description
B RW INPUT Connect Connect of disconnect input buffer Connect place input buffer Disconnect input buffer Pull configuration Disabled Pulldown Pullup Pullup Pullup Pullup Pullup Pullup Pullup Pullup on pin Disabled Pullup Pullup Pullup on pin Pullup Pullup Pullup on pin Pullup Pullup on pin Pullup on	Α	RW	DIR			Pin direction. Same physical register as DIR register
B RW INPUT Connect Connect Connect Connect input buffer Disconnect Disco				Input	0	Configure pin as an input pin
Connect Disconnect 0 Connect input buffer Disconnect input buffer Disconnect input buffer Pull configuration C RW PULL Pull Pull Pull Pull Pull Pull Pull Pu				Output	1	Configure pin as an output pin
C RW PULL Pullonfiguration Disabled 0 No pull Onfiguration Pullon Pull down on pin Pullup 3 Pull Up on pin Drive configuration Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 Disconnect '0' standard '1' (normally used for wired-or connections) Disconnect '0', high drive '1' (normally used for wired-or connections) Disconnect '1' (normally used for wired-and connect '1' (normally used for wired-and connections) E RW SENSE Disabled Disabled O Disabled	В	RW	INPUT			Connect or disconnect input buffer
C RW PULL Disabled 0 No pull Pull down on pin Pullup 3 Pull up on pin D RW DRIVE SOS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' HOH1 3 High drive '0', high drive '1" DOS1 4 Disconnect '0', high drive '1' DOS1 5 Standard '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) FOR DISSONSE RW SENSE Disabled 0 Disabled Pull own on pin Pull up				Connect	0	Connect input buffer
Disabled 0 No pull Pulldown 1 Pull down on pin Pullup 3 Pull up on pin Drive configuration Drive configuration SoS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1' H0H1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) BOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				Disconnect	1	Disconnect input buffer
Pulldown 1 Pulldown on pin Pullup 3 Pull up on pin D RW DRIVE Drive configuration SOS1 0 Standard '0', standard '1' HOS1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high drive '1' DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled	С	RW	PULL			Pull configuration
Pullup 3 Pullup on pin Drive configuration Standard '0', standard '1' H0S1 1 High drive '0', standard '1' H0H1 3 High drive '0', high drive '1' DoS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Standard '0', high drive '1' (normally used for wired-and connections) Fig. 8W SENSE Disabled Disabled Pullup on pin Drive configuration Drive configuration Standard '0', standard '1' High drive '0', high drive '1' High drive '0', disconnect '1' (normally used for wired-and connections) Pin sensing mechanism Disabled Disabled				Disabled	0	No pull
D RW DRIVE SOS1 O Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high drive '1" DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled				Pulldown	1	Pull down on pin
SOS1 0 Standard '0', standard '1' H0S1 1 High drive '0', standard '1' SOH1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1" DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0', disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled O Disabled				Pullup	3	Pull up on pin
H0S1 1 High drive '0', standard '1' S0H1 2 Standard '0', high drive '1' H0H1 3 High drive '0', high 'drive '1" D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled	D	RW	DRIVE			Drive configuration
SOH1 2 Standard '0', high drive '1' HOH1 3 High drive '0', high 'drive '1" DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				SOS1	0	Standard '0', standard '1'
H0H1 3 High drive '0', high 'drive '1" D0S1 4 Disconnect '0' standard '1' (normally used for wired-or connections) D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				H0S1	1	High drive '0', standard '1'
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				S0H1	2	Standard '0', high drive '1'
connections) DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled O Disabled				H0H1	3	High drive '0', high 'drive '1"
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
connections) SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) HOD1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Disabled 0 Disabled						connections)
S0D1 6 Standard '0'. disconnect '1' (normally used for wired-and connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
connections) H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled						connections)
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled				SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
connections) E RW SENSE Pin sensing mechanism Disabled 0 Disabled						connections)
E RW SENSE Pin sensing mechanism Disabled 0 Disabled				H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
Disabled 0 Disabled						connections)
	E	RW	SENSE			Pin sensing mechanism
				Disabled	0	Disabled
High 2 Sense for high level				High	2	Sense for high level
Low 3 Sense for low level				Low	3	Sense for low level

20.3.29 PIN_CNF[19]

Address offset: 0x74C Configuration of GPIO pins

Bit r	numb	er		31	30	29	28 :	27 :	26 2	5 2	4 23	22	2 21	20	19	18	17	16	15	14	13	L2 1	1 1	0 9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					[D	D					СС	: В	Α
Res	et OxC	00000002		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0) 1	. 0
Id	RW	Field	Value Id	Va	lue						De	esci	ripti	on																		
Α	RW	DIR									Pir	n di	irec	tior	ı. Sa	me	ph	ıysi	al r	egi	ster	as (DIR I	regis	ter							
			Input	0							Co	nfi	gure	e pi	n as	an	in	out	pin													
			Output	1							Co	nfi	gure	e pi	n as	an	ou	tpu	t pi	n												
В	RW	INPUT									Co	nn	ect	or c	disc	onn	ect	inp	ut	buf	er											
			Connect	0							Co	nn	ect	inp	ut b	uff	er															
			Disconnect	1							Dis	sco	nne	ct i	npu	t b	uffe	er														
С	RW	PULL									Pu	III c	onfi	igur	atio	n																
			Disabled	0							No	рι	الد																			
			Pulldown	1							Pu	III d	low	n oı	n pii	n																
			Pullup	3							Pu	ıll u	ро	n pi	in																	
D	RW	DRIVE									Dr	ive	cor	nfig	urat	ion	1															
			S0S1	0							Sta	and	lard	'0' ,	, sta	nda	ard	'1'														
			H0S1	1							Hi	gh	driv	e '0)', st	and	dar	d '1	'													
			S0H1	2							Sta	and	lard	'0' ,	, hig	h d	Iriv	e '1	1													
			H0H1	3							Hi	gh	driv	e '0)', hi	igh	'dr	ve '	1"													
			DOS1	4							Dis	sco	nne	ct '	0' st	tan	dar	d '1	' (n	orm	ally	use	d fo	or w	red	-or						
											со	nn	ecti	ons)																	



Bit number	31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.30 PIN_CNF[20]

Address offset: 0x750

Configuration of GPIO pins

-	9	diation of all 10 p			
Bit	numb	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E D D D C C B A
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			SOS1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Ε	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.31 PIN_CNF[21]

Address offset: 0x754



Reset 0x00000002 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	C C B A 0 0 0 1 0													
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin	0 0 0 1 0													
A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin														
Input 0 Configure pin as an input pin														
	, , ,													
Output 1 Configure pin as an output pin														
B RW INPUT Connect or disconnect input buffer														
Connect 0 Connect input buffer														
Disconnect 1 Disconnect input buffer														
C RW PULL Pull configuration														
Disabled 0 No pull	No pull													
Pulldown 1 Pull down on pin	Pull down on pin													
Pullup 3 Pull up on pin														
D RW DRIVE Drive configuration														
SOS1 0 Standard '0', standard '1'														
H0S1 1 High drive '0', standard '1'														
SOH1 2 Standard '0', high drive '1'	Standard '0', high drive '1'													
H0H1 3 High drive '0', high 'drive '1"														
D0S1 4 Disconnect '0' standard '1' (normally used for wired-or														
connections)														
DOH1 5 Disconnect '0', high drive '1' (normally used for wired-or														
connections)														
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and	Standard '0'. disconnect '1' (normally used for wired-and													
connections)														
HOD1 7 High drive '0', disconnect '1' (normally used for wired-and														
connections)														
E RW SENSE Pin sensing mechanism														
Disabled 0 Disabled														
High 2 Sense for high level														
Low 3 Sense for low level														

20.3.32 PIN_CNF[22]

Address offset: 0x758
Configuration of GPIO pins

Bit r	numb	er		31	30	29	28 :	27 :	26 2	5 2	4 23	22	2 21	20	19	18	17	16	15	14	13 1	12 1	1 1	9	8	7	6	5	4	3 2	1	0												
Id																	Ε	Ε					С	D	D				(С	В	Α												
Reset 0x00000002						0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	1	0												
Id	RW	Field	Value Id	Value								escr	ripti	on																														
Α	RW	DIR								Pin direction. Same physical register as DIR register																																		
			Input	0							Configure pin as an input pin																																	
			Output	1								nfi	gure	e pi	n as	an	ou	tpu	t pi	n																								
В	RW	INPUT									Connect or disconnect input buffer																																	
			Connect	0							Co	nn	ect	inp	ut b	uff	er																											
			Disconnect	1								Disconnect input buffer																																
С	RW	PULL		0 1								Pull configuration																																
			Disabled									No pull																																
			Pulldown									Pull down on pin																																
			Pullup									Pull up on pin																																
D	RW	DRIVE										Drive configuration																																
			S0S1	0 Star									Standard '0', standard '1'																															
			H0S1	1 2							High drive '0', standard '1'																																	
			S0H1								Standard '0', high drive '1'																																	
			H0H1	3								High drive '0', high 'drive '1"																																
			DOS1	4							Dis	sco	nne	ct '	0' st	an	dar	d '1	no	orm	ally	use	d fo	r wi	red-	or																		
											со	nne	ecti	ons)																	Disconnect '0' standard '1' (normally used for wired-or connections)												



Bit number		31 3	30 29	9 28	8 27	26	25 2	24 2	23 22	21	20 :	19 1	8 1	7 16	5 15	14	13	12	11 :	10 9) ;	3 7	6	5	4	3	2	1 0
Id													E	E						DΙ))				С	С	ВА
Reset 0x00000002		0	0 0	0	0	0	0	0	0 0	0	0	0 (0 (0	0	0	0	0	0	0 () (0	0	0	0	0	0	1 0
Id RW Field V	/alue Id	Valu	ıe						Descr	iptic	n																	
D	00H1	5							Disco	nnec	t '0	', hi	gh d	rive	'1'	(no	rma	ally u	ısec	for	wi	red-	or					
								c	conne	ectio	ns)																	
S	60D1	6						5	Stand	ard '	0'.	disc	onn	ect	'1' (nor	mal	ly us	sed	for v	vir	ed-a	nd					
								c	conne	ectio	ns)																	
н	H0D1	7						H	High (drive	'0',	, dis	con	nect	'1'	(no	rma	ally u	ısec	for	wi	red-	and	ł				
								c	conne	ectio	ns)																	
E RW SENSE								F	Pin se	nsin	g m	ech	anis	m														
D	Disabled	0						[Disab	led																		
н	ligh	2						5	Sense	for	higl	n lev	/el															
L	ow	3						5	Sense	for	low	lev	el															

20.3.33 PIN_CNF[23]

Address offset: 0x75C

Configuration of GPIO pins

	E E DDD CCBA
eset 0x00000002	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
RW Field Value Id	Value Description
RW DIR	Pin direction. Same physical register as DIR register
Input	0 Configure pin as an input pin
Output	1 Configure pin as an output pin
RW INPUT	Connect or disconnect input buffer
Connect	0 Connect input buffer
Disconnect	1 Disconnect input buffer
RW PULL	Pull configuration
Disabled	0 No pull
Pulldown	1 Pull down on pin
Pullup	3 Pull up on pin
RW DRIVE	Drive configuration
S0S1	0 Standard '0', standard '1'
H0S1	1 High drive '0', standard '1'
S0H1	2 Standard '0', high drive '1'
H0H1	3 High drive '0', high 'drive '1"
D0S1	4 Disconnect '0' standard '1' (normally used for wired-or
	connections)
D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
	connections)
SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
	connections)
H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
	connections)
	Pin sensing mechanism
RW SENSE	0 0 1 1 1
Disabled	0 Disabled
	2 Sense for high level 3 Sense for low level

20.3.34 PIN_CNF[24]

Address offset: 0x760

Configuration of GPIO pins



Bit	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x00000002		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPUT			Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIVE			Drive configuration
		S0S1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENSE			Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

20.3.35 PIN_CNF[25]

Address offset: 0x764 Configuration of GPIO pins

СВА
0 1 0



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E D D D C C B A
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.36 PIN_CNF[26]

Address offset: 0x768

Configuration of GPIO pins

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.37 PIN_CNF[27]

Address offset: 0x76C

Configuration of GPIO pins



Bit	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x00000002		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPUT			Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIVE			Drive configuration
		S0S1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENSE			Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

20.3.38 PIN_CNF[28]

Address offset: 0x770 Configuration of GPIO pins

Bit r	numbe	er		31	30 :	29 2	28 2	27 2	26 25	5 24	4 23	22	21	20	19	18	17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id																	Ε	Ε					D	D	D				C	С	В	Α
Rese	et OxC	0000002		0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	1	0
Id	RW	Field	Value Id	Va	lue						De	scr	ipti	on																		
Α	RW	DIR									Pin	ı di	rect	ion	. Sa	me	ph	ysic	al r	egis	ter	as D	IR r	egis	ter							
			Input	0							Co	nfi	gure	piı	n as	an	inp	ut p	oin													
			Output	1							Co	nfi	gure	piı	n as	an	out	put	t pir	1												
В	RW	INPUT									Co	nn	ect o	or d	lisco	nn	ect	inp	ut b	uffe	er											
			Connect	0							Co	nn	ect i	npı	ut bi	uffe	er															
			Disconnect	1							Dis	co	nne	ct ii	npu	bu	ıffe	r														
С	RW	PULL									Pu	II c	onfi	gur	atio	n																
			Disabled	0							No	рι	ıll																			
			Pulldown	1							Pu	ll d	owr	or	n pir																	
			Pullup	3							Pu	ll u	p or	n pi	n																	
D	RW	DRIVE									Dri	ive	con	figu	urati	on																
			S0S1	0							Sta	and	ard	'0',	sta	nda	ırd	'1'														
			H0S1	1							Hig	gh (drive	e '0	', st	and	larc	l '1'														
			S0H1	2							Sta	and	ard	'0',	hig	h dı	rive	'1'														
			H0H1	3							Hig	gh (drive	e '0	', hi	gh '	dri	/e ':	1''													
			DOS1	4							Dis	sco	nne	ct '(O' st	and	lard	1'1'	(nc	rma	ally	use	d fo	r wi	red-	or						
											coı	nne	ectio	ns))																	



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E D D D C C B A
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.39 PIN_CNF[29]

Address offset: 0x774

Configuration of GPIO pins

Bit nu	ımbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Reset	0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.40 PIN_CNF[30]

Address offset: 0x778

Configuration of GPIO pins



Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E D D D C C B A
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Ε	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.41 PIN_CNF[31]

Address offset: 0x77C Configuration of GPIO pins

numb	er		31	. 30	29	28	27	26 2	25 :	24	23 2	22	21 :	20	19 1	18 :	17 :	16	15 :	.4 :	13 :	12 :	l1 1	.0 9	8	7	6	5	4	3	2 :	1 0
																	Е	E					1) C	D					С	C E	3 A
et 0x(00000002		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 1	1 0
RW	Field	Value Id	Va	lue							Des	cri	ptio	n																		
RW	DIR										Pin	dir	ecti	on.	Sar	ne	phy	sic	al re	gis	ter	as	DIR	regi	ster							
		Input	0								Con	fig	ure	pin	as	an i	inpı	ut p	in													
		Output	1								Con	fig	ure	pin	as	an (out	put	pin													
RW	INPUT										Con	ne	ct o	r di	sco	nne	ect i	npı	ut b	uff	er											
		Connect	0								Con	ne	ct ir	npu	t bu	ffe	r															
		Disconnect	1								Disc	on	nec	t in	put	bu	ffer															
RW	PULL										Pull	со	nfig	gura	tioi	1																
		Disabled	0								No p	pul	I																			
		Pulldown	1								Pull	do	wn	on	pin																	
		Pullup	3								Pull	up	on	pir	1																	
RW	DRIVE										Driv	e c	onf	igu	rati	on																
		S0S1	0							:	Star	nda	rd '	0',	star	ıda	rd '	1'														
		H0S1	1								High	n d	rive	'0'	, sta	nd	ard	'1'														
		S0H1	2							:	Star	nda	rd '	0',	high	dr	ive	'1'														
		H0H1	3								High	n di	rive	'0'	, hig	h 'd	driv	e '1	L''													
		DOS1	4								Disc	on	nec	t '0	' sta	nd	ard	'1'	(no	rm	ally	use	ed f	or w	ired	l-or						
											con	nor	rtio	ns)																		
	RW RW	RW Field RW INPUT RW PULL RW DRIVE	RW Field Value Id RW DIR Input Output RW INPUT Connect Disconnect RW PULL Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 HOH1	RW Field Value Id Val	RW Field Value Id Input O Output I Input Output I Input Id Input Id Input Id Input Id Input Id Input Id Id Id Id Id Id Id I	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 THE SOH1 2 HOH1 3 TO T	RW Field Value Id Input O Output I I ID	RW Field Value Id Val	RW Field Value Id Value Id Value Id Value Id RW DIR RW INPUT Connect Disconnect 1 RW PULL PULL Disabled O Pulldown 1 Pullup 3 RW DRIVE SOS1 O HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1 SOH1	RW Field Value Id Value RW DIR Input 0 Output 1 RW INPUT Connect 0 Disconnect 1 RW PULL Disabled 0 Pulldown 1 Pullup 3 RW DRIVE SOS1 0 HOS1 1 SOH1 2 HOH1 3 DOS1 4	RW Field Value Id Value RW DIR Input Output 1 Connect Disconnect Disconnect Disabled Pulldown Pullup RW DRIVE SOS1 HOS1 SOH1 SOH1 SOH1 SOH1 SOH1 SOS1 HOS1 A TO SO TO	RW Field Value Id Value	RW Field Value Id Val	RW Field Value Id Value	RW Field Value Id Val	RW Field Value Id Value Valu	RW DIR	RW Field Value Market Pin direction. Same physical	RW Field Value Id Value Pin direction. Same physical reference Pin d	RW Field Value Id Value Pin direction. Same physical register	RW Field Value Id Value Id Value Id Description Pin direction. Same physical register	RW Field Value Id Value Valu	RW Field Value Id Id Id Id Id Id Id I	RW Field	RW Field Value Id Value	RW Field Value Id Value Id Pin direction. Same physical register as DIR regist	RW Field Value Id Val	RW Field Value Id Value	RW Field Value Id Value Valu	RW Field Value Id Value I	RW Field Value Id Val



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0												
Id		E E DDD CCBA												
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0												
Id RW Field Value Id	Value	Description												
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or												
		connections)												
S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and												
		connections)												
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and												
		connections)												
E RW SENSE		Pin sensing mechanism												
Disabled	0	Disabled												
High	2	Sense for high level												
Low	3	Sense for low level												

20.4 Electrical Specification

20.4.1 GPIO Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
V _{IH}	Input high voltage	0.7 x VD	D	VDD	V
V _{IL}	Input low voltage	VSS		0.3 x VDE	V
V _{OH,SD}	Output high voltage, standard drive, 0.5 mA, VDD ≥1.7	VDD-0.4		VDD	V
V _{OH,HDH}	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD-0.4		VDD	V
V _{OH,HDL}	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD-0.4		VDD	V
V _{OL,SD}	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS		VSS+0.4	V
V _{OL,HDH}	Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS		VSS+0.4	V
V _{OL,HDL}	Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS		VSS+0.4	V
I _{OL,SD}	Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7	1	2	4	mA
I _{OL,HDH}	Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA
I _{OL,HDL}	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
I _{OH,SD}	Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7	1	2	4	mA
I _{OH,HDH}	Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
I _{OH,HDL}	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3			mA
t _{RF,15pF}	Rise/fall time, low drive mode, 10-90%, 15 pF load ¹		9		ns
t _{RF,25pF}	Rise/fall time, low drive mode, 10-90%, 25 pF load ¹		13		ns
t _{RF,50pF}	Rise/fall time, low drive mode, 10-90%, 50 pF load ¹		25		ns
t _{HRF,15pF}	Rise/Fall time, high drive mode, 10-90%, 15 pF load ¹		4		ns
t _{HRF,25pF}	Rise/Fall time, high drive mode, 10-90%, 25 pF load ¹		5		ns
t _{HRF,50pF}	Rise/Fall time, high drive mode, 10-90%, 50 pF load ¹		8		ns
R _{PU}	Pull-up resistance	11	13	16	kΩ
R _{PD}	Pull-down resistance	11	13	16	kΩ
C _{PAD}	Pad capacitance		3		pF
C _{PAD_NFC}	Pad capacitance on NFC pads		4		pF
I _{NFC_LEAK}	Leakage current between NFC pads when driven to different		2	10	μΑ
	states				

The current drawn from the battery when GPIO is active as an output is calculated as follows:

I_{GPIO}=V_{DD} C_{load} f

 C_{load} being the load capacitance and "f" is the switching frequency.

¹ Rise and fall times based on simulations



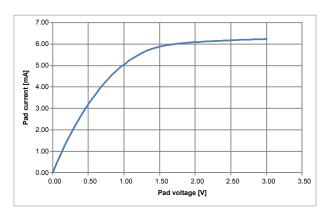


Figure 22: GPIO drive strength vs Voltage, standard drive, VDD = 3.0 V

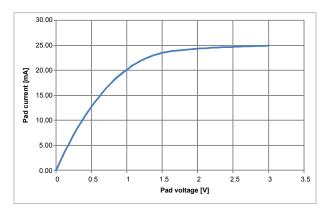


Figure 23: GPIO drive strength vs Voltage, high drive, VDD = 3.0 V

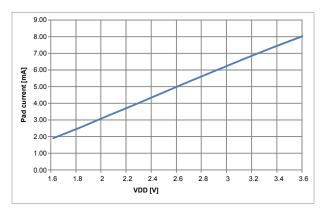


Figure 24: Max sink current vs Voltage, standard drive

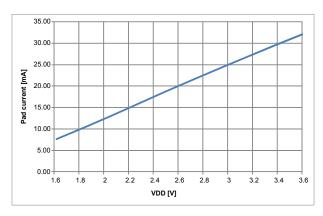


Figure 25: Max sink current vs Voltage, high drive

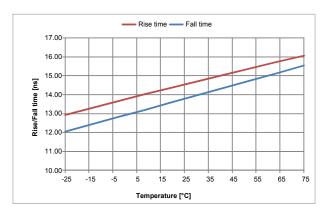


Figure 26: Rise and fall time vs Temperature, 10%-90%, 25pF load capacitance, VDD = 3.0 V



21 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Low power detection of pin state changes is possible when in System ON or System OFF.

Table 26: GPIOTE properties

Instance	Number of GPIOTE channels
mistance	Number of Griotz chamies
GPIOTE	8

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one (OUT) is configurable to perform following operations:

- Set
- Clear
- · Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- · Rising edge
- Falling edge
- · Any change

21.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The tasks (SET[n], CLR[n] and OUT[n]) can be used for writing to individual pins, and the events (IN[n]) can be generated from changes occurring at the inputs of individual pins.

The SET task will set the pin selected in CONFIG[n].PSEL to high.

The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in CONFIG[n].POLARITY, and can either set the pin high, set it low, or toggle it.

The tasks and events are configured using the CONFIG[n] registers. Every set of SET, CLR and OUT[n] tasks and IN[n] events has one CONFIG[n] register associated with it.

As long as a SET[n], CLR[n] and OUT[n] task or an IN[n] event is configured to control a pin **n**, the pin's output value will only be updated by the GPIOTE module. The pin's output value as specified in the GPIO will therefore be ignored as long as the pin is controlled by GPIOTE. Attempting to write a pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, see MODE field in CONFIG[n] register, the associated pin will get the output and configuration values specified in the GPIO module.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, the precedence of the tasks will be as described in *Table 27: Task priorities* on page 154.

Table 27: Task priorities

Priority	Task
1	OUT
2	CLR
3	SET



When setting the CONFIG[n] registers, MODE=Disabled does not have the same effect as MODE=Task and POLARITY=None. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, according to the priorities described in the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the OUTINIT field of CONFIG[n].

21.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See *GPIO* — *General purpose input/output* on page 107 for more information about the DETECT signal.

Putting the system into System ON IDLE while DETECT is high will not cause DETECT to wake the system up again. Make sure to clear all DETECT sources before entering sleep. If the LATCH register is used as a source, if any bit in LATCH is still high after clearing all or part of the register (for instance due to one of the PINx.DETECT signal still high), a new rising edge will be generated on DETECT, see *Pin configuration* on page 107.

Trying to put the system to System OFF while DETECT is high will cause a wakeup from System OFF reset.

This feature is always enabled although the peripheral itself appears to be IDLE, that is, no clocks or other power intensive infrastructure have to be requested to keep this feature enabled. This feature can therefore be used to wake up the CPU from a WFI or WFE type sleep in System ON with all peripherals and the CPU idle, that is, lowest power consumption in System ON mode.

In order to prevent spurious interrupts from the PORT event while configuring the sources, the user shall first disable interrupts on the PORT event (through INTENCLR.PORT), then configure the sources (PIN_CNF[n].SENSE), clear any potential event that could have occurred during configuration (write '1' to EVENTS_PORT), and finally enable interrupts (through INTENSET.PORT).

21.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO.

Only one GPIOTE channel can be assigned to one physical pin. Failing to do so may result in unpredictable behavior.

21.4 Registers

Table 28: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40006000	GPIOTE	GPIOTE	GPIO tasks and events		

Table 29: Register Overview

Register	Offset	Description
TASKS_OUT[0]	0x000	Task for writing to pin specified in CONFIG[0]. PSEL. Action on pin is configured in
		CONFIG[0].POLARITY.
TASKS_OUT[1]	0x004	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is configured in
		CONFIG[1].POLARITY.



Register	Offset	Description
TASKS_OUT[2]	0x008	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is configured in
.,00.[2]	choco	CONFIG[2].POLARITY.
TASKS_OUT[3]	0x00C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is configured in
17.51.5_001[5]	OXOGE	CONFIG[3].POLARITY.
TASKS_OUT[4]	0x010	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is configured in
17.585_551[4]	0.010	CONFIG[4].POLARITY.
TASKS_OUT[5]	0x014	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is configured in
17.5.65_551[5]	0.014	CONFIG[5].POLARITY.
TASKS_OUT[6]	0x018	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is configured in
173/3_001[0]	0.010	CONFIG[6].POLARITY.
TASKS_OUT[7]	0x01C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is configured in
173/3_001[7]	OXOIC	CONFIG[7].POLARITY.
TASKS_SET[0]	0x030	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it high.
TASKS_SET[1]	0x034	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it high.
TASKS_SET[2]	0x034 0x038	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it high.
TASKS_SET[2]	0x03C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it high.
TASKS_SET[4]	0x040	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it high.
TASKS_SET[4]	0x040	
TASKS_SET[6]	0x044 0x048	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it high. Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high.
TASKS_SET[7]	0x046	
TASKS_CLR[0]	0x04C 0x060	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it high. Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low.
TASKS_CLR[1]	0x064	
_	0x068	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low.
TASKS_CLR[2]		Task for writing to pin specified in CONFIG[2] PSEL. Action on pin is to set it low.
TASKS_CLR[3]	0x06C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low.
TASKS_CLR[4]	0x070	Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low.
TASKS_CLR[5]	0x074	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low.
TASKS_CLR[6]	0x078 0x07C	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low.
TASKS_CLR[7]	0x100	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low.
EVENTS_IN[0]	0x100	Event generated from pin specified in CONFIG[0].PSEL Event generated from pin specified in CONFIG[1].PSEL
EVENTS_IN[1]	0x104 0x108	
EVENTS_IN[2]	0x108 0x10C	Event generated from pin specified in CONFIG[2].PSEL Event generated from pin specified in CONFIG[3].PSEL
EVENTS_IN[3] EVENTS_IN[4]	0x10C 0x110	Event generated from pin specified in CONFIG[3].F3EL Event generated from pin specified in CONFIG[4].PSEL
EVENTS_IN[5]	0x110	Event generated from pin specified in CONFIG[4].F3EL
EVENTS_IN[6]	0x114 0x118	Event generated from pin specified in CONFIG[6].PSEL
EVENTS_IN[7]	0x116	Event generated from pin specified in CONFIG[7].PSEL
EVENTS_PORT	0x11C 0x17C	Event generated from multiple input GPIO pins with SENSE mechanism enabled
INTENSET	0x17C 0x304	Event generated from multiple input GPIO pins with SENSE mechanism enabled Enable interrupt
INTENCLR	0x304 0x308	Disable interrupt
CONFIG[0]	0x510	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[1]	0x510 0x514	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[2]	0x514 0x518	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[3]	0x516 0x51C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[4]	0x51C 0x520	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[5]	0x520 0x524	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[6]	0x524 0x528	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[7]	0x526 0x52C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event
CONFIG[7]	UXJZC	Cominguration for Outpirt, serting and Central tasks and Inting event

21.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	1	H G F E D C B A
Reset 0x00000000	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description

A RW INO Write '1' to Enable interrupt for IN[0] event



	numbe	er		31 30 2	29 28	27 26	5 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0												
Id				1				H G F E D C B A												
kes Id		0000000 Field	Value Id	Value	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0												
Iu	IVVV	rieiu	value lu	value				See EVENTS_IN[0]												
			Set	1				Enable												
			Disabled	0				Read: Disabled												
			Enabled	1				Read: Enabled												
В	RW	IN1						Write '1' to Enable interrupt for IN[1] event												
								See EVENTS_IN[1]												
			Set	1				Enable												
			Disabled	0				Read: Disabled												
			Enabled	1				Read: Enabled												
С	RW	IN2						Write '1' to Enable interrupt for IN[2] event												
								See EVENTS_IN[2]												
			Set	1				Enable												
			Disabled	0				Read: Disabled												
			Enabled	1				Read: Enabled												
D	RW	IN3						Write '1' to Enable interrupt for IN[3] event												
								See EVENTS_IN[3]												
			Set	1				Enable												
			Disabled	0				Read: Disabled												
			Enabled	1				Read: Enabled												
Ε	RW	IN4						Write '1' to Enable interrupt for IN[4] event												
								See EVENTS_IN[4]												
			Set	1				Enable												
			Disabled	0				Read: Disabled												
			Enabled	1				Read: Enabled												
F	RW	IN5						Write '1' to Enable interrupt for IN[5] event												
								See EVENTS_IN[5]												
			Set	1				Enable												
			Disabled	0				Read: Disabled												
			Enabled	1				Read: Enabled												
G	RW	IN6						Write '1' to Enable interrupt for IN[6] event												
								See EVENTS_IN[6]												
			Set	1				Enable												
			Disabled	0				Read: Disabled												
			Enabled	1				Read: Enabled												
Н	RW	IN7						Write '1' to Enable interrupt for IN[7] event												
								See EVENTS_IN[7]												
			Set	1				Enable												
			Disabled	0				Read: Disabled												
			Enabled	1				Read: Enabled												
I	RW	PORT						Write '1' to Enable interrupt for PORT event												
								See EVENTS_PORT												
			Set	1				Enable												
			Disabled	0				Read: Disabled												
			Enabled	1				Read: Enabled												

21.4.2 INTENCLR

Address offset: 0x308

Disable interrupt



Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			T.	HGFEDCBA
	set 0x00000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld ^	RW Field	Value Id	Value	Description Write 14 to Displie intervent for INIO count
Α	RW INO			Write '1' to Disable interrupt for IN[0] event
				See EVENTS_IN[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
_	5	Enabled	1	Read: Enabled
В	RW IN1			Write '1' to Disable interrupt for IN[1] event
				See EVENTS_IN[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW IN2			Write '1' to Disable interrupt for IN[2] event
				See EVENTS_IN[2]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW IN3			Write '1' to Disable interrupt for IN[3] event
				See EVENTS_IN[3]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW IN4			Write '1' to Disable interrupt for IN[4] event
				See EVENTS_IN[4]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW IN5			Write '1' to Disable interrupt for IN[5] event
				See EVENTS_IN[5]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW IN6			Write '1' to Disable interrupt for IN[6] event
				See EVENTS_IN[6]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW IN7			Write '1' to Disable interrupt for IN[7] event
				See EVENTS_IN[7]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
I	RW PORT			Write '1' to Disable interrupt for PORT event
				See EVENTS_PORT
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
			-	

21.4.3 CONFIG[0]

Address offset: 0x510



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E DD BBBB AA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW MODE	Mode
Disabled	O Disabled. Pin specified by PSEL will not be acquired by the
	GPIOTE module.
Event	1 Event mode
	The pin specified by PSEL will be configured as an input and the
	IN[n] event will be generated if operation specified in POLARITY
	occurs on the pin.
Task	3 Task mode
	The GPIO specified by PSEL will be configured as an output and
	triggering the SET[n], CLR[n] or OUT[n] task will perform the
	operation specified by POLARITY on the pin. When enabled as a
	task the GPIOTE module will acquire the pin and the pin can no
	longer be written as a regular output pin from the GPIO module.
B RW PSEL	[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
	and IN[n] event
D RW POLARITY	When In task mode: Operation to be performed on output
	when OUT[n] task is triggered. When In event mode: Operation
	on input that shall trigger IN[n] event.
None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
	IN[n] event generated on pin activity.
LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
	IN[n] event when rising edge on pin.
HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
	IN[n] event when falling edge on pin.
Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
	IN[n] when any change on pin.
E RW OUTINIT	When in task mode: Initial value of the output when the GPIOTE
	channel is configured. When in event mode: No effect.
Low	0 Task mode: Initial value of pin before task triggering is low
High	1 Task mode: Initial value of pin before task triggering is high

21.4.4 CONFIG[1]

Address offset: 0x514

Bit r	ıumbe	r		31 3	0 29	28 2	27 2	6 25	24	23 2	22 :	21 20	0 19	9 18	3 17	' 16	15	14	13	12	11 1	0 9	8	7	6 !	5 4	3	2	1 ()
Id	Id											Е			D	D				В	ВЕ	3 B	В						Α ,	4
Res	Reset 0x00000000					0	0 (0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0 (0 0	0	0	0 ()
Id	RW	Field	Value Id	Value						Des	cri	ption	ı																	
Α	RW	MODE								Mod	de																			
			Disabled	0					Disabled. Pin specified by PSEL will not be acquired by the																					
										GPIOTE module.																				
			Event	1						Event mode																				
										The	pir	ı spe	cifi	ed b	y P	SEL	will	be	cor	nfigu	ıred	as a	n in	put	and	the				
										IN[r	ո] e	vent	wil	l be	ger	nera	ited	lifo	pe	ratio	on sp	ecifi	ied i	in P	OLAI	RITY				
									occurs on the pin.																					
			Task	3						Tasl	k m	ode																		
									The GPIO specified by PSEL will be configured as an output and																					
											ger	ing th	ne S	SET[n],	CLR	[n] (or C	DUT	[n] 1	task	will	perf	orn	n the					
											operation specified by POLARITY on the pin. When enabled as a																			
										task	k th	e GP	IOT	E m	odu	ıle v	vill	acq	uire	e the	e pin	and	the	pir	n can	no				
										long	ger	be w	ritt	en a	as a	reg	ula	r ou	ıtpu	ıt pi	n fro	m th	ne G	PIC) mo	dule				



Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E DD BBBBB AA
Re	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
В	RW PSEL		[031]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
				and IN[n] event
D	RW POLARITY			When In task mode: Operation to be performed on output
				when OUT[n] task is triggered. When In event mode: Operation
				on input that shall trigger IN[n] event.
		None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no
				IN[n] event generated on pin activity.
		LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate
				IN[n] event when rising edge on pin.
		HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate
				IN[n] event when falling edge on pin.
		Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate
				IN[n] when any change on pin.
Ε	RW OUTINIT			When in task mode: Initial value of the output when the GPIOTE
				channel is configured. When in event mode: No effect.
		Low	0	Task mode: Initial value of pin before task triggering is low
		High	1	Task mode: Initial value of pin before task triggering is high

21.4.5 CONFIG[2]

Address offset: 0x518

Bit nu	umbe	er		31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				E	D D B B B B B
Reset	t 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description	
Α	RW	MODE		Mode	
			Disabled	0 Disabled. Pin	specified by PSEL will not be acquired by the
				GPIOTE modu	ıle.
			Event	1 Event mode	
				The pin speci	fied by PSEL will be configured as an input and the
				IN[n] event w	vill be generated if operation specified in POLARITY
				occurs on the	pin.
			Task	3 Task mode	
				The GPIO spe	cified by PSEL will be configured as an output and
				triggering the	SET[n], CLR[n] or OUT[n] task will perform the
				operation spe	ecified by POLARITY on the pin. When enabled as a
				task the GPIC	TE module will acquire the pin and the pin can no
				longer be wri	tten as a regular output pin from the GPIO module.
В	RW	PSEL		[031] GPIO number	associated with SET[n], CLR[n] and OUT[n] tasks
				and IN[n] eve	ent
D	RW	POLARITY		When In task	mode: Operation to be performed on output
				when OUT[n]	task is triggered. When In event mode: Operation
				on input that	shall trigger IN[n] event.
			None	0 Task mode: N	lo effect on pin from OUT[n] task. Event mode: no
				IN[n] event g	enerated on pin activity.
			LoToHi	1 Task mode: S	et pin from OUT[n] task. Event mode: Generate
				IN[n] event w	hen rising edge on pin.
			HiToLo	2 Task mode: C	lear pin from OUT[n] task. Event mode: Generate
				IN[n] event w	hen falling edge on pin.
			Toggle	3 Task mode: T	oggle pin from OUT[n]. Event mode: Generate
				IN[n] when a	ny change on pin.



Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	.0	9 1	3 7	7 6	5	4	3	2	1	0
Id													Ε			D	D				В	В	В	ВΙ	3						Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0
ld RW Field	Value Id	Va	lue							De	scri	pti	on																			
E RW OUTINIT										Wŀ	nen	in t	tasl	c mo	ode	: In	itia	l va	lue	of t	he	out	out	wh	en t	he (GPI	OTE				
										cha	ann	el i	s cc	nfig	gure	ed.	Wh	en	in e	ven	it m	ode	: N	o ef	fec	t.						
	Low	0								Tas	sk n	nod	le: I	niti	al v	alu	e of	f pir	n be	for	e ta	sk t	rigg	erii	ng i	s lov	v					
	High	1								Tas	sk n	nod	le: I	niti	al v	alu	e of	f pir	n be	for	e ta	sk t	rigg	erii	ng i	s hig	gh					

21.4.6 CONFIG[3]

Address offset: 0x51C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

			• • •																										
	numbe	er		31	. 30	29	28 27	7 26 :	25 2	4 23	22 21		19 1				14 :	L3 1	2 11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id												Ε		D	D			E	3 B	В	В	В						Α	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0 (0 0	0 0	0	0	0 0	0	0	0	0 (0	0	0	0	0	0	0 () (0	0	0
ld	RW	Field	Value Id	Va	alue					De	scripti	ion																	
Α	RW	MODE								Mo	ode																		
			Disabled	0						Dis	abled	. Pir	spe	ifie	d by	PSE	Lw	ll no	t be	acc	uire	ed b	y th	ie					
										GP	IOTE r	nod	ule.																
			Event	1						Ev	ent mo	ode																	
										Th	e pin s	рес	ified	by P	SEL	will	be (conf	igur	ed a	s ar	inp	ut a	and	the	:			
										IN	[n] eve	ent v	will b	e ge	nera	ated	if o	pera	tion	spe	cifi	ed ii	n PC	LA	RITY	1			
										OC	curs o	n th	e pin																
			Task	3						Ta	sk mod	de																	
										Th	e GPIC) sp	ecifie	d by	/ PSI	EL w	ill b	e co	nfigi	ured	as	an c	utp	ut	and				
										tri	ggerin	g th	e SET	[n],	CLR	[n] (or O	UT[r	n] ta	sk w	ill p	erfo	orm	the	e				
										ор	eratio	n sp	ecifie	ed b	y PC	DLAF	RITY	on t	he p	in. \	Vhe	n e	nab	led	as a	1			
										tas	k the	GPI	OTE r	nod	ule v	will	acqu	iire 1	he į	oin a	nd	the	pin	car	n no				
										lor	nger be	e wr	itten	as a	reg	gular	out	put	pin	fron	n th	e GI	PIO	mo	dule	э.			
В	RW	PSEL		[0	31]					GP	IO nur	nbe	r ass	ocia	ted	with	SE7	[n],	CLR	[n] a	and	OU [.]	T[n]	tas	sks				
										an	d IN[n] ev	ent																
D	RW	POLARITY								WI	nen In	tasl	k mo	de: 0	Ope	ratio	n to	be	perf	orm	ed (on c	utp	ut					
										wh	ien Ol	JT[n] tasl	c is t	rigg	erec	l. W	hen	In e	vent	mo	ode:	Ор	era	tion	1			
										on	input	tha	t sha	ll tri	gger	· IN[n] e	/ent											
			None	0						Ta	sk mod	de: I	No ef	fect	on	pin f	rom	OU	T[n]	tasl	k. Ev	vent	mc	de	: no				
											[n] eve	_				•													
			LoToHi	1							sk mod								Eve	nt n	nod	e: G	ene	rat	e				
											[n] eve				-	-													
			HiToLo	2							sk mod								k. E	vent	mc	ode:	Gei	ner	ate				
				_							[n] eve				-	_						_							
			Toggle	3							sk mod							nj. i	ver	it m	ode	: Ge	ner	ate					
_	D\A'	OUTINIT									[n] wh					-		-f +l-	۰.۰	ıtını.			+h.c	CD	NOT!	г -			
E	KW	OUTINIT									nen in													GΡ	101	E			
			Law	0							annel i		_																
			Low	0							sk mod sk mod					•						_							
			High	1						I d	0011176	ue: I	ıııııd	vdl	ue 0	n bit	ı ne	ore	tdSl	v triệ	ger	ıııg	15 []	gII					

21.4.7 CONFIG[4]

Address offset: 0x520



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E DD BBBBB AA
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW MODE			Mode
	Disabled	0	Disabled. Pin specified by PSEL will not be acquired by the
			GPIOTE module.
	Event	1	Event mode
			The pin specified by PSEL will be configured as an input and the
			IN[n] event will be generated if operation specified in POLARITY
			occurs on the pin.
	Task	3	Task mode
			The GPIO specified by PSEL will be configured as an output and
			triggering the SET[n], CLR[n] or OUT[n] task will perform the
			operation specified by POLARITY on the pin. When enabled as a
			task the GPIOTE module will acquire the pin and the pin can no
			longer be written as a regular output pin from the GPIO module.
B RW PSEL		[031]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
			and IN[n] event
D RW POLARITY			When In task mode: Operation to be performed on output
			when OUT[n] task is triggered. When In event mode: Operation
			on input that shall trigger IN[n] event.
	None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no
			IN[n] event generated on pin activity.
	LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate
			IN[n] event when rising edge on pin.
	HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate
			IN[n] event when falling edge on pin.
	Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate
			IN[n] when any change on pin.
E RW OUTINIT			When in task mode: Initial value of the output when the GPIOTE
			channel is configured. When in event mode: No effect.
	Low	0	Task mode: Initial value of pin before task triggering is low
	High	1	Task mode: Initial value of pin before task triggering is high

21.4.8 CONFIG[5]

Address offset: 0x524

Bit r	ıumbe	r		31 3	0 29	28 2	27 2	6 25	24	23 2	22 :	21 20	0 19	9 18	3 17	' 16	15	14	13	12	11 1	0 9	8	7	6 !	5 4	3	2	1 ()
Id												Е			D	D				В	ВЕ	3 B	В						Α ,	4
Res	et 0x0	0000000		0 (0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0 (0 0	0	0	0 ()
Id	RW	Field	Value Id	Valu	e					Des	cri	ption	ı																	
Α	RW	MODE								Mod	de																			
			Disabled	0						Disa	able	ed. Pi	n s	peci	fiec	d by	PSE	EL w	vill r	not l	be a	cquir	ed l	by t	he					
										GPI	OT	E mod	dul	e.																
			Event	1						Eve	nt r	node	è																	
										The	pir	ı spe	cifi	ed b	y P	SEL	will	be	cor	nfigu	ıred	as a	n in	put	and	the				
										IN[r	ո] e	vent	wil	l be	ger	nera	ited	lifo	pe	ratio	on sp	ecifi	ied i	in P	OLAI	RITY				
										occi	urs	on th	ne p	pin.																
			Task	3						Tasl	k m	ode																		
										The	GP	lO sp	eci	ified	l by	PSE	Lw	ill b	oe c	onfi	gure	d as	an	out	put a	and				
										trigg	ger	ing th	ne S	SET[n],	CLR	[n] (or C	DUT	[n] 1	task	will	perf	orn	n the					
										ope	rat	ion s	pec	ifie	d by	PO	LAF	RITY	on on	the	pin.	Wh	en e	enal	bled	as a				
										task	k th	e GP	IOT	E m	odu	ıle v	vill	acq	uire	e the	e pin	and	the	pir	n can	no				
										long	ger	be w	ritt	en a	as a	reg	ula	r ou	ıtpu	ıt pi	n fro	m th	ne G	PIC) mo	dule				



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E DD BBBB AA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
B RW PSEL	[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
	and IN[n] event
D RW POLARITY	When In task mode: Operation to be performed on output
	when OUT[n] task is triggered. When In event mode: Operation
	on input that shall trigger IN[n] event.
None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
	IN[n] event generated on pin activity.
LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
	IN[n] event when rising edge on pin.
HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
	IN[n] event when falling edge on pin.
Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
	IN[n] when any change on pin.
E RW OUTINIT	When in task mode: Initial value of the output when the GPIOTE
	channel is configured. When in event mode: No effect.
Low	0 Task mode: Initial value of pin before task triggering is low
High	1 Task mode: Initial value of pin before task triggering is high

21.4.9 CONFIG[6]

Address offset: 0x528

Bit nu	umbe	er		31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				E	D D B B B B B
Reset	t 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description	
Α	RW	MODE		Mode	
			Disabled	0 Disabled. Pin	specified by PSEL will not be acquired by the
				GPIOTE modu	ıle.
			Event	1 Event mode	
				The pin speci	fied by PSEL will be configured as an input and the
				IN[n] event w	vill be generated if operation specified in POLARITY
				occurs on the	pin.
			Task	3 Task mode	
				The GPIO spe	cified by PSEL will be configured as an output and
				triggering the	SET[n], CLR[n] or OUT[n] task will perform the
				operation spe	ecified by POLARITY on the pin. When enabled as a
				task the GPIC	TE module will acquire the pin and the pin can no
				longer be wri	tten as a regular output pin from the GPIO module.
В	RW	PSEL		[031] GPIO number	associated with SET[n], CLR[n] and OUT[n] tasks
				and IN[n] eve	ent
D	RW	POLARITY		When In task	mode: Operation to be performed on output
				when OUT[n]	task is triggered. When In event mode: Operation
				on input that	shall trigger IN[n] event.
			None	0 Task mode: N	lo effect on pin from OUT[n] task. Event mode: no
				IN[n] event g	enerated on pin activity.
			LoToHi	1 Task mode: S	et pin from OUT[n] task. Event mode: Generate
				IN[n] event w	hen rising edge on pin.
			HiToLo	2 Task mode: C	lear pin from OUT[n] task. Event mode: Generate
				IN[n] event w	hen falling edge on pin.
			Toggle	3 Task mode: T	oggle pin from OUT[n]. Event mode: Generate
				IN[n] when a	ny change on pin.



Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	.0	9 1	3 7	7 6	5	4	3	2	1	0
Id													Ε			D	D				В	В	В	В	3						Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0
ld RW Field	Value Id	Va	lue							De	scri	pti	on																			
E RW OUTINIT										Wŀ	nen	in t	tasl	c mo	ode	: In	itia	l va	lue	of t	he	out	out	wh	en t	he (GPI	OTE				
										cha	ann	el i	s cc	nfig	gure	ed.	Wh	en	in e	ven	it m	ode	: N	o ef	fec	t.						
	Low	0								Tas	sk n	nod	le: I	niti	al v	alu	e of	f pir	n be	for	e ta	sk t	rigg	erii	ng i	s lov	v					
	High	1								Tas	sk n	nod	le: I	niti	al v	alu	e of	f pir	n be	for	e ta	sk t	rigg	erii	ng i	s hig	gh					

21.4.10 CONFIG[7]

Address offset: 0x52C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			E DD BBBBB AA
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW MODE			Mode
	Disabled	0	Disabled. Pin specified by PSEL will not be acquired by the
			GPIOTE module.
	Event	1	Event mode
			The pin specified by PSEL will be configured as an input and the
			IN[n] event will be generated if operation specified in POLARITY
			occurs on the pin.
	Task	3	Task mode
			The GPIO specified by PSEL will be configured as an output and
			triggering the SET[n], CLR[n] or OUT[n] task will perform the
			operation specified by POLARITY on the pin. When enabled as a
			task the GPIOTE module will acquire the pin and the pin can no
			longer be written as a regular output pin from the GPIO module.
B RW PSEL		[031]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
			and IN[n] event
D RW POLARITY			When In task mode: Operation to be performed on output
			when OUT[n] task is triggered. When In event mode: Operation
			on input that shall trigger IN[n] event.
	None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no
			IN[n] event generated on pin activity.
	LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate
			IN[n] event when rising edge on pin.
	HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate
			IN[n] event when falling edge on pin.
	Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate
			IN[n] when any change on pin.
E RW OUTINIT			When in task mode: Initial value of the output when the GPIOTE
			channel is configured. When in event mode: No effect.
	Low	0	Task mode: Initial value of pin before task triggering is low
	High	1	Task mode: Initial value of pin before task triggering is high

21.5 Electrical Specification

21.5.1 GPIOTE Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
$I_{GPIOTE,IN}$	Run current with 1 or more GPIOTE active channels in Input		0.1	0.5	μΑ
	mode				



22 PPI — Programmable peripheral interconnect

The Programmable peripheral interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

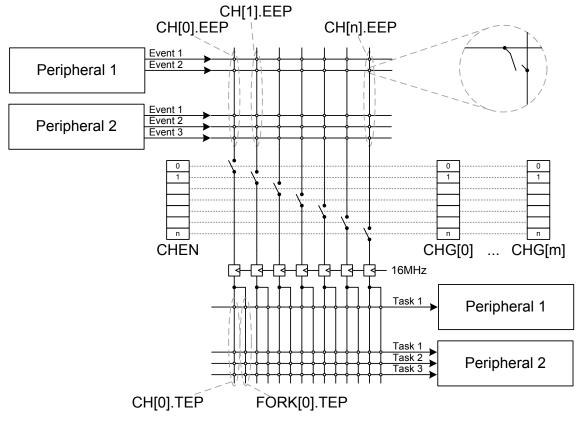


Figure 27: PPI block diagram

The PPI system has, in addition to the fully programmable peripheral interconnections, a set of channels where the event end point (EEP) and task end points (TEP) are fixed in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels.

Table 30: Configurable and fixed PPI channels

Instance	Channel	Number of channels	Number of groups
PPI	0-19	20	6
PPI (fixed)	20-31	12	

The PPI provides a mechanism to automatically trigger a task in one peripheral as a result of an event occurring in another peripheral. A task is connected to an event through a PPI channel. The PPI channel is composed of three end point registers, one EEP and two TEPs. A peripheral task is connected to a TEP using the address of the task register associated with the task. Similarly, a peripheral event is connected to an EEP using the address of the event register associated with the event.

On each PPI channel, the signals are synchronized to the 16 MHz clock, to avoid any internal violation of setup and hold timings. As a consequence, events that are synchronous to the 16 MHz clock will be delayed by one clock period, while other asynchronous events will be delayed by up to one 16 MHz clock period.

Each TEP implements a fork mechanism that enables a second task to be triggered at the same time as the task specified in the TEP is triggered. This second task is configured in the task end point register in the FORK registers groups, e.g. FORK.TEP[0] is associated with PPI channel CH[0].



There are two ways of enabling and disabling PPI channels:

- Enable or disable PPI channels individually using the CHEN, CHENSET, and CHENCLR registers.
- Enable or disable PPI channels in PPI channel groups through the groups' ENABLE and DISABLE tasks. Prior to these tasks being triggered, the PPI channel group must be configured to define which PPI channels belongs to which groups.

Note that when a channel belongs to two groups m and n, and CHG[m].EN and CHG[n].DIS occur simultaneously (m and n can be equal or different), EN on that channel has priority.

PPI tasks (for example, CHG[0].EN) can be triggered through the PPI like any other task, which means they can be hooked up to a PPI channel as a TEP. One event can trigger multiple tasks by using multiple channels and one task can be triggered by multiple events in the same way.

22.1 Pre-programmed channels

Some of the PPI channels are pre-programmed. These channels cannot be configured by the CPU, but can be added to groups and enabled and disabled like the general purpose PPI channels. The FORK TEP for these channels are still programmable and can be used by the application.

For a list of pre-programmed PPI channels, see the table below.

Table 31: Pre-programmed channels

Channel	EEP	TEP
20	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
21	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
22	TIMERO->EVENTS_COMPARE[1]	RADIO->TASKS_DISABLE
23	RADIO->EVENTS_BCMATCH	AAR->TASKS_START
24	RADIO->EVENTS_READY	CCM->TASKS_KSGEN
25	RADIO->EVENTS_ADDRESS	CCM->TASKS_CRYPT
26	RADIO->EVENTS_ADDRESS	TIMERO->TASKS_CAPTURE[1]
27	RADIO->EVENTS_END	TIMERO->TASKS_CAPTURE[2]
28	RTCO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
29	RTCO->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
30	RTCO->EVENTS_COMPARE[0]	TIMERO->TASKS_CLEAR
31	RTCO->EVENTS_COMPARE[0]	TIMERO->TASKS_START

22.2 Registers

Table 32: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x4001F000	PPI	PPI	PPI controller		

Table 33: Register Overview

Register	Offset	Description
TASKS_CHG[0].EN	0x000	Enable channel group 0
TASKS_CHG[0].DIS	0x004	Disable channel group 0
TASKS_CHG[1].EN	0x008	Enable channel group 1
TASKS_CHG[1].DIS	0x00C	Disable channel group 1
TASKS_CHG[2].EN	0x010	Enable channel group 2
TASKS_CHG[2].DIS	0x014	Disable channel group 2
TASKS_CHG[3].EN	0x018	Enable channel group 3
TASKS_CHG[3].DIS	0x01C	Disable channel group 3
TASKS_CHG[4].EN	0x020	Enable channel group 4
TASKS_CHG[4].DIS	0x024	Disable channel group 4
TASKS_CHG[5].EN	0x028	Enable channel group 5
TASKS_CHG[5].DIS	0x02C	Disable channel group 5
CHEN	0x500	Channel enable register
CHENSET	0x504	Channel enable set register
CHENCLR	0x508	Channel enable clear register



Register	Offset	Description
CH[0].EEP	0x510	Channel 0 event end-point
CH[0].TEP	0x514	Channel 0 task end-point
CH[1].EEP	0x518	Channel 1 event end-point
CH[1].TEP	0x51C	Channel 1 task end-point
CH[2].EEP	0x520	Channel 2 event end-point
CH[2].TEP	0x524	Channel 2 task end-point
CH[3].EEP	0x528	Channel 3 event end-point
CH[3].TEP	0x52C	Channel 3 task end-point
CH[4].EEP	0x530	Channel 4 event end-point
CH[4].TEP	0x534	Channel 4 task end-point
CH[5].EEP	0x538	Channel 5 event end-point
CH[5].TEP	0x53C	Channel 5 task end-point
CH[6].EEP	0x540	Channel 6 event end-point
CH[6].TEP	0x544	Channel 6 task end-point
CH[7].EEP	0x548	Channel 7 event end-point
CH[7].TEP	0x54C	Channel 7 task end-point
CH[8].EEP	0x550	Channel 8 event end-point
CH[8].TEP	0x554	Channel 8 task end-point
CH[9].EEP	0x558	Channel 9 event end-point
CH[9].TEP	0x55C	Channel 9 task end-point
CH[10].EEP	0x560	Channel 10 event end-point
CH[10].TEP	0x564	Channel 10 task end-point
CH[11].EEP	0x568	Channel 11 event end-point
CH[11].TEP	0x56C	Channel 11 task end-point
CH[12].EEP	0x570	Channel 12 event end-point
CH[12].TEP	0x574	Channel 12 task end-point
CH[13].EEP	0x578	Channel 13 event end-point
CH[13].TEP	0x57C	Channel 13 task end-point
CH[14].EEP	0x580	Channel 14 event end-point
CH[14].TEP	0x584	Channel 14 task end-point
CH[15].EEP	0x588	Channel 15 event end-point
CH[15].TEP	0x58C	Channel 15 task end-point
CH[16].EEP	0x590	Channel 16 event end-point
CH[16].TEP	0x594	Channel 16 task end-point
CH[17].EEP	0x598	Channel 17 event end-point
CH[17].TEP	0x59C	Channel 17 task end-point
CH[18].EEP	0x5A0	Channel 18 event end-point
CH[18].TEP	0x5A4	Channel 18 task end-point
CH[19].EEP	0x5A8	Channel 19 event end-point
CH[19].TEP	0x5AC	Channel 19 task end-point
CHG[0]	0x800	Channel group 0
CHG[1]	0x804	Channel group 1
CHG[2]	0x808	Channel group 2
CHG[3]	0x80C	Channel group 3
CHG[4]	0x810	Channel group 4
CHG[5]	0x814	Channel group 5
FORK[0].TEP	0x910	Channel 0 task end-point
FORK[1].TEP	0x914	Channel 1 task end-point
FORK[2].TEP	0x918	Channel 2 task end-point
FORK[3].TEP	0x91C	Channel 3 task end-point
FORK[4].TEP	0x920	Channel 4 task end-point
FORK[5].TEP	0x924	Channel 5 task end-point
FORK[6].TEP	0x928	Channel 6 task end-point
FORK[7].TEP	0x92C	Channel 7 task end-point
FORK[8].TEP	0x930	Channel 8 task end-point
FORK[9].TEP	0x934	Channel 9 task end-point
FORK[10].TEP	0x938	Channel 10 task end-point
FORK[11].TEP	0x93C	Channel 11 task end-point



Register	Offset	Description	
FORK[12].TEP	0x940	Channel 12 task end-point	
FORK[13].TEP	0x944	Channel 13 task end-point	
FORK[14].TEP	0x948	Channel 14 task end-point	
FORK[15].TEP	0x94C	Channel 15 task end-point	
FORK[16].TEP	0x950	Channel 16 task end-point	
FORK[17].TEP	0x954	Channel 17 task end-point	
FORK[18].TEP	0x958	Channel 18 task end-point	
FORK[19].TEP	0x95C	Channel 19 task end-point	
FORK[20].TEP	0x960	Channel 20 task end-point	
FORK[21].TEP	0x964	Channel 21 task end-point	
FORK[22].TEP	0x968	Channel 22 task end-point	
FORK[23].TEP	0x96C	Channel 23 task end-point	
FORK[24].TEP	0x970	Channel 24 task end-point	
FORK[25].TEP	0x974	Channel 25 task end-point	
FORK[26].TEP	0x978	Channel 26 task end-point	
FORK[27].TEP	0x97C	Channel 27 task end-point	
FORK[28].TEP	0x980	Channel 28 task end-point	
FORK[29].TEP	0x984	Channel 29 task end-point	
FORK[30].TEP	0x988	Channel 30 task end-point	
FORK[31].TEP	0x98C	Channel 31 task end-point	

22.2.1 CHEN

Address offset: 0x500 Channel enable register

Bitı	numbe	er		3	1 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 1	7 1	5 15	14	13	12	11	10 !	9 8	3 7	6	5	4	3 2	2 1	. 0
Id				f	e	d	С	b	а	Z	Υ	Χ	W	VΙ	. ر	Т :	S F	R C	Į P	0	N	М	L	K .	J	I H	G	F	Е	D (C E	A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0 (0	0
Id	RW	Field	Value Id	٧	alue	•						De	escrip	tio	n																	
Α	RW	CH0										En	able	or c	lisa	ble	cha	inne	el O													
			Disabled	0								Dis	sable	cha	ann	el																
			Enabled	1								En	able	cha	nne	el																
В	RW	CH1										En	able	or c	lisa	ble	cha	inne	1													
			Disabled	0								Dis	sable	cha	ann	el																
			Enabled	1								En	able	cha	nne	el																
С	RW	CH2										En	able	or c	lisa	ble	cha	nne	el 2													
			Disabled	0								Dis	sable	cha	ann	el																
			Enabled	1								En	able	cha	nne	el																
D	RW	CH3										En	able	or c	lisa	ble	cha	inne	13													
			Disabled	0								Dis	sable	cha	ann	el																
			Enabled	1								En	able	cha	nne	el																
E	RW	CH4										En	able	or c	lisa	ble	cha	nne	el 4													
			Disabled	0								Dis	sable	cha	ann	el																
			Enabled	1								En	able	cha	nne	el																
F	RW	CH5										En	able	or c	lisa	ble	cha	nne	15													
			Disabled	0								Dis	sable	cha	nn	el																
			Enabled	1								En	able	cha	nne	el																
G	RW	CH6										En	able	or c	lisa	ble	cha	inne	l 6													
			Disabled	0								Dis	sable	cha	nn	el																
			Enabled	1								En	able	cha	nne	el																
Н	RW	CH7										En	able	or c	lisa	ble	cha	nne	17													
			Disabled	0								Dis	sable	cha	nn	el																
			Enabled	1								En	able	cha	nne	el																
I	RW	CH8										En	able	or c	lisa	ble	cha	inne	8 le													
			Disabled	0								Dis	sable	cha	nn	el																
			Enabled	1									able																			
J	RW	CH9										En	able	or c	lisa	ble	cha	nne	19													



Bit n	umbe	er		31 30	29 2	8 27	7 26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d d	c b	а	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Rese	t 0x0	0000000		0 0	0 (0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Disabled	0					Disable channel
			Enabled	1					Enable channel
K	RW	CH10	D: 11 1						Enable or disable channel 10
			Disabled	0					Disable channel
L	D\A/	CH11	Enabled	1					Enable channel Enable or disable channel 11
-	11.00	CHII	Disabled	0					Disable channel
			Enabled	1					Enable channel
М	RW	CH12							Enable or disable channel 12
			Disabled	0					Disable channel
			Enabled	1					Enable channel
N	RW	CH13							Enable or disable channel 13
			Disabled	0					Disable channel
			Enabled	1					Enable channel
0	RW	CH14							Enable or disable channel 14
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Р	RW	CH15							Enable or disable channel 15
			Disabled	0					Disable channel
	DIA	CUAC	Enabled	1					Enable channel
Q	RW	CH16	Disabled	0					Enable or disable channel 16
			Disabled Enabled	0					Disable channel Enable channel
R	R\M/	CH17	Ellableu	1					Enable or disable channel 17
	11.00	CHIT	Disabled	0					Disable channel
			Enabled	1					Enable channel
S	RW	CH18							Enable or disable channel 18
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Т	RW	CH19							Enable or disable channel 19
			Disabled	0					Disable channel
			Enabled	1					Enable channel
U	RW	CH20							Enable or disable channel 20
			Disabled	0					Disable channel
			Enabled	1					Enable channel
V	RW	CH21							Enable or disable channel 21
			Disabled	0					Disable channel
۱۸/	D\A/	CH22	Enabled	1					Enable channel Enable or disable channel 22
W	KVV	CH22	Disabled	0					Disable channel
			Enabled	1					Enable channel
Х	RW	CH23	Liidaica	-					Enable or disable channel 23
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Υ	RW	CH24							Enable or disable channel 24
			Disabled	0					Disable channel
			Enabled	1					Enable channel
Z	RW	CH25							Enable or disable channel 25
			Disabled	0					Disable channel
			Enabled	1					Enable channel
а	RW	CH26							Enable or disable channel 26
			Disabled	0					Disable channel
			Enabled	1					Enable channel
b	RW	CH27							Enable or disable channel 27
			Disabled	0					Disable channel



Bit r	numbe	r		31	30	29	28 2	27 2	26 2	25 2	24 2	23 2	22 2	1 2	0 1	9 1	8 1	7 16	5 15	5 14	4 1	3 12	2 11	10	9	8	7	6 5	5 4	3	2	1	0
Id				f	е	d	С	b	a i	Z	Υ)	X١	w v	/ ι	J 1	Γ 5	R	(a	P	C	1 (IN	1 L	K	J	1	Н	G I	= E	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0 (0	0 0) () () (0	0	0	0) (0	0	0	0	0	0	0 (0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						C	Des	crip	tior	1																		
			Enabled	1							Е	nal	ble o	ha	nne	el																	
С	RW	CH28									Е	nal	ble o	or d	lisal	ble	cha	nne	1 28	3													
			Disabled	0								Disa	ble	cha	nne	el																	
			Enabled	1							E	nal	ble o	ha	nne	el																	
d	RW	CH29									Е	nal	ble o	or d	lisal	ble	cha	nne	1 29	Э													
			Disabled	0							C	Disa	ble	cha	nne	el																	
			Enabled	1							Е	nal	ble o	ha	nne	el																	
е	RW	CH30									Е	nal	ble o	or d	lisal	ble	cha	nne	1 30)													
			Disabled	0								Disa	ble	cha	nne	el																	
			Enabled	1							Е	nal	ble o	ha	nne	el																	
f	RW	CH31									E	nal	ble o	or d	lisal	ble	cha	nne	13:	1													
			Disabled	0							C	Disa	ble	cha	nne	el																	
			Enabled	1							E	nal	ble o	ha	nne	el																	

22.2.2 CHENSET

Address offset: 0x504

Channel enable set register

Read: reads value of CH{i} field in CHEN register.

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	3 22 2	21 2	20	19	18	17	16	15	14	1 13	3 1	2 1	111	0 9	9 8	7	' 6	5	4	3	2	1	0
Id				f	e	d	С	b	а	Z	Υ	Х	W	V	U	Т	S	R	Q	Р	C	N	Ν	1	L F	(J	ŀ	1 6	F	Ε	D	С	В	Α
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C)	0 () (0	(0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	llue	•						D	escrip	otio	n																				
Α	RW	CH0										Cl	hanne	el O	en	abl	e s	et r	egi	ste	r. \	Vrit	ing	g '0	' ha	s n	o ef	fec	t						
			Disabled	0								Re	ead: c	har	nne	el d	isal	oled	ı																
			Enabled	1								Re	ead: c	har	nne	el e	nak	led																	
			Set	1								W	/rite:	Ena	ble	e ch	an	nel																	
В	RW	CH1										Cl	hanne	el 1	en	abl	e s	et r	egi	ste	r. \	Vrit	ing	g '0	' ha	s n	o ef	fec	t						
			Disabled	0								Re	ead: c	har	nne	el d	isal	oled	ı																
			Enabled	1								Re	ead: c	har	nne	el e	nak	led																	
			Set	1								W	/rite:	Ena	ble	e ch	an	nel																	
С	RW	CH2										Cl	hanne	el 2	en	abl	e s	et r	egi	ste	r. \	Vrit	ing	g '0	' ha	s n	o ef	fec	t						
			Disabled	0								Re	ead: c	har	nne	el d	isal	oled	ı																
			Enabled	1								Re	ead: c	har	nne	el e	nak	led																	
			Set	1								W	/rite:	Ena	ble	e ch	an	nel																	
D	RW	CH3										Cl	hanne	el 3	en	abl	e s	et r	egi	ste	r. \	Vrit	ing	g '0	' ha	s n	o ef	fec	t						
			Disabled	0								Re	ead: c	har	nne	el d	isal	oled	ı																
			Enabled	1								Re	ead: c	har	nne	el e	nak	led																	
			Set	1								W	/rite:	Ena	able	e ch	an	nel																	
Е	RW	CH4										Cl	hanne	el 4	en	abl	e s	et r	egi	ste	r. \	Vrit	ing	g '0	' ha	s n	o ef	fec	t						
			Disabled	0								Re	ead: c	har	nne	el d	isal	oled	ı																
			Enabled	1								Re	ead: c	har	nne	el e	nak	led																	
			Set	1								W	/rite:	Ena	able	e ch	an	nel																	
F	RW	CH5										Cl	hanne	el 5	en	abl	e s	et r	egi	ste	r. \	Vrit	ing	g '0	' ha	s n	o ef	fec	t						
			Disabled	0								Re	ead: c	har	nne	el d	isal	oled	ı																
			Enabled	1								Re	ead: c	har	nne	el e	nak	led																	
			Set	1								W	/rite:	Ena	able	e ch	an	nel																	
G	RW	CH6										Cl	hanne	el 6	en	abl	e s	et r	egi	ste	r. \	Vrit	ing	g '0	' ha	s n	o ef	fec	t						
			Disabled	0								Re	ead: c	har	nne	el d	isal	oled	ı																
			Enabled	1								Re	ead: c	har	nne	el e	nak	led																	
			Set	1								W	/rite:	Ena	ble	e ch	an	nel																	
Н	RW	CH7										Cl	hanne	el 7	en	abl	e s	et r	egi	ste	r. \	Vrit	ing	g '0	' ha	s n	o ef	fec	t						
			Disabled	0								Re	ead: c	har	nne	el d	isal	oled	1																



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW Field	Value Id	Value Description
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
I	RW CH8		Channel 8 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
J	RW CH9		Channel 9 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
K	RW CH10		Channel 10 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
L	RW CH11		Channel 11 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
М	RW CH12	D: 11 1	Channel 12 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
	DW CH12	Set	1 Write: Enable channel
N	RW CH13	Disabled	Channel 13 enable set register. Writing '0' has no effect O Read: channel disabled
		Disabled	
		Enabled	
0	RW CH14	Set	Write: Enable channel Channel 14 enable set register. Writing '0' has no effect
U	KW CH14	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Р	RW CH15	360	Channel 15 enable set register. Writing '0' has no effect
•	6.125	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Q	RW CH16		Channel 16 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
R	RW CH17		Channel 17 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
S	RW CH18		Channel 18 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Т	RW CH19		Channel 19 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
U	RW CH20		Channel 20 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
٧	RW CH21		Channel 21 enable set register. Writing '0' has no effect



Bit r	numbe	er		31 30	29 2	28 2	7 26 :	25 24	23	3 22 2	1 2	20 1	9 1	.8 1	17 1	16 :	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1
Id				f e																										
Res	et 0x0	0000000		0 0	0	0 0	0	0 0	0	0 ()	0 (0 (0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Value	:				De	escrip	tio	n																		
			Disabled	0					Re	ead: cl	har	nnel	dis	abl	led															
			Enabled	1					Re	ead: cl	har	nnel	en	abl	ed															
			Set	1					W	rite: E	na	ble	cha	nn	el															
W	RW	CH22							Ch	nanne	1 22	2 en	abl	e s	et r	egi	ste	r. V	√riti	ng '	0' h	as n	o e	ffec	t					
			Disabled	0					Re	ead: cl	har	nnel	dis	abl	led															
			Enabled	1						ead: cl																				
			Set	1						rite: E																				
Х	RW	CH23								nanne						egi	ste	r. V	√riti	ng '	0' h	as n	o e	ffec	t					
			Disabled	0						ead: cl																				
			Enabled	1						ead: cl																				
V	DIA	CU24	Set	1						rite: E								- \^	/=:+:	na '	O' b			er o						
Υ	r VV	CH24	Disabled	0						nanne ead: cl						egi	عدد	ı. V	villi	ııg	U III	a5 IÌ	υe	iiec	ı					
			Enabled	1						ead: cl																				
			Set	1						rite: E																				
Z	RW	CH25		-						nanne						egi	iste	r. V	√riti	ng '	0' ha	as n	o e	ffec	t					
			Disabled	0						ead: cl						-0				Ü										
			Enabled	1					Re	ead: cl	har	nnel	ena	abl	ed															
			Set	1					W	rite: E	na	ble	cha	nn	el															
а	RW	CH26							Cŀ	nanne	126	6 en	abl	e s	et r	egi	ste	r. V	√riti	ng '	0' h	as n	o e	ffec	t					
			Disabled	0					Re	ead: cl	har	nnel	dis	ab	led															
			Enabled	1					Re	ead: cl	har	nnel	ena	abl	ed															
			Set	1					W	rite: E	na	ble	cha	nn	el															
b	RW	CH27							Ch	nanne	127	7 en	abl	e s	et r	egi	ste	r. V	√riti	ng '	0' h	as n	o e	ffec	t					
			Disabled	0						ead: cl																				
			Enabled	1						ead: cl																				
			Set	1						rite: E																				
С	RW	CH28	Disabled	0						nanne						egı	ste	r. V	Vriti	ng '	O. P	as n	o e	ttec	t					
			Disabled Enabled	0						ead: cl																				
			Set	1						rite: E																				
d	RW	CH29	300	_						nanne						egi	iste	r V	/riti	nø '	Ո' h։	as n	o e	ffec	t					
_		5.125	Disabled	0						ead: cl						υ _Б .			• • • • •	6					•					
			Enabled	1						ead: cl																				
			Set	1					W	rite: E	na	ble	cha	nn	el															
e	RW	CH30								nanne						egi	ste	r. V	Vriti	ng '	0' h	as n	o e	ffec	t					
			Disabled	0					Re	ead: cl	har	nnel	dis	ab	led															
			Enabled	1					Re	ead: cl	har	nnel	ena	abl	ed															
			Set	1					W	rite: E	na	ble	cha	nn	el															
f	RW	CH31							Ch	nanne	13:	1 en	abl	e s	et r	egi	ste	r. V	√riti	ng '	0' h	as n	o e	ffec	t					
			Disabled	0					Re	ead: cl	har	nnel	dis	ab	led															
			Enabled	1					Re	ead: cl	har	nnel	ena	abl	ed															
			Set	1					W	rite: E	na	ble	cha	nn	el															

22.2.3 CHENCLR

Address offset: 0x508

Channel enable clear register

Read: reads value of CH{i} field in CHEN register.



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Α	RW CH0		Channel 0 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
_	B	Clear	1 Write: disable channel
В	RW CH1	5	Channel 1 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
_	DW CH2	Clear	1 Write: disable channel
С	RW CH2	Disabled	Channel 2 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
D	DW CH3	Clear	1 Write: disable channel
D	RW CH3	Disabled	Channel 3 enable clear register. Writing '0' has no effect O Read: channel disabled
		Disabled	
		Enabled	1 Read: channel enabled
_	DW CHA	Clear	1 Write: disable channel
E	RW CH4	Disabled	Channel 4 enable clear register. Writing '0' has no effect O Read: channel disabled
		Disabled Enabled	
		Clear	1 Read: channel enabled 1 Write: disable channel
Е	RW CH5	Clear	
Г	NW CH3	Disabled	Channel 5 enable clear register. Writing '0' has no effect O Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
G	RW CH6	Clear	Channel 6 enable clear register. Writing '0' has no effect
J	NW CHO	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
Н	RW CH7	5 .ca.	Channel 7 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
ı	RW CH8		Channel 8 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
J	RW CH9		Channel 9 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
K	RW CH10		Channel 10 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
L	RW CH11		Channel 11 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
М	RW CH12		Channel 12 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
N	RW CH13		Channel 13 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled



Bit n	numbe	er		31 30	29 2	8 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	c b	a :	Z Y	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Rese	et 0x0	0000000		0 0	0 0	0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	•				Description
			Clear	1					Write: disable channel
0	RW	CH14							Channel 14 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
Р	RW	CH15							Channel 15 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
Q	RW	CH16		_					Channel 16 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
R	RW	CH17							Channel 17 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
S	RW	CH18		_					Channel 18 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
_			Clear	1					Write: disable channel
Т	RW	CH19	5	_					Channel 19 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
	DIA	CU20	Clear	1					Write: disable channel
U	KW	CH20	D' III I	•					Channel 20 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
.,	D) 4 /	CUDA	Clear	1					Write: disable channel
V	KW	CH21	District.	•					Channel 21 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
١	DVA	CU22	Clear	1					Write: disable channel
vv	RW	CH22	Disabled	0					Channel 22 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
v	DVA	CH22	Clear	1					Write: disable channel
Х	KVV	CH23	Disabled	0					Channel 23 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
٧,	DVA	CU24	Clear	1					Write: disable channel
Υ	KW	CH24	D' III I	•					Channel 24 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
-	DVA	CHOE	Clear	1					Write: disable channel
Z	KW	CH25	Disabled	0					Channel 25 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
	D. C.	CU2C	Clear	1					Write: disable channel
а	КW	CH26	D: 11 1	•					Channel 26 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
b	RW	CH27							Channel 27 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled



Rit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id	number		
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
С	RW CH28		Channel 28 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
d	RW CH29		Channel 29 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
e	RW CH30		Channel 30 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel
f	RW CH31		Channel 31 enable clear register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Clear	1 Write: disable channel

22.2.4 CH[0].EEP

Address offset: 0x510

Channel 0 event end-point

Bit r	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 :	L8 1	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id															Α	Α	A A	4 Α	Δ Α	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۱	А А
Rese	et OxC	0000000		0	0	0	0	0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 () (0 0				
Id	RW	Field	Value Id	0 0 0 0 0 0 0 d																													
Α	RW	EEP										Poi	inte	r to	eve	ent	regi	stei	r. A	cce	ots (only	ad	dres	sses	to	reg	iste	rs				
												fro	m t	he l	ver	nt g	rou	٥.															

22.2.5 CH[0].TEP

Address offset: 0x514 Channel 0 task end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (,
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ĺ
Res	et 0x0	0000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (,	
Id	RW	Field							De	scri	ptic	on																				ı			
Α	RW	TEP		Value											ta	sk r	egis	ter	. A	cce	ots	onl	y a	ddr	ess	es t	o re	egis	ter	s					7

from the Task group.

22.2.6 CH[1].EEP

Address offset: 0x518

Channel 1 event end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	L7 1	16 1	15 1	14 1	13 1	2 :	11 1) 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	Α.	Α.	Α	Α.	Α	A A	. Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																		
Α	RW	EEP										Poi	nte	r to	eve	ent	regi	iste	r. A	cce	pts	on	ly a	ddr	esse	s to	re	giste	ers				

Pointer to event register. Accepts only addresses to registers

from the Event group.



22.2.7 CH[1].TEP

Address offset: 0x51C Channel 1 task end-point

Bit r	umb	er		33	1 30	29	28	27	7 26	25	24	23	22	21 2	0 19	9 18	3 17	16	15	14	13	12	11 1	.0	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Д Д	A	Α	Α	Α	Α	Α	Α	Α.	Δ.	Α	Α	Α	Α	Α	Α	Α ,	A A	4 A
Res	et Ox(0000000		0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0				
Id	RW	Field	Value Id			De	scrip	otio	n																								
Λ	D\A/	TEP					Poi	intei	r to	task	reg	iste	r. A	ccei	nts	only	v ad	ldre	sse	s to	re	gist	ters	5									
_	L AA	161														0			,			,					0						

22.2.8 CH[2].EEP

Address offset: 0x520 Channel 2 event end-point

Bit r	iumbe	er		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue	•						De	scri	ptic	on																			
Α	RW	EEP										Ро	inte	r to	ev	ent	reg	giste	er. A	Acc	ept	s or	nly a	add	res	ses	to	reg	iste	rs				
												fro	m t	he	Eve	nt g	rou	ıp.																

22.2.9 CH[2].TEP

Address offset: 0x524 Channel 2 task end-point

Bitı	numbe	r		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12 :	l1 1	.0	9	8	7	6	5 4	4 3	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α.	A A	A A	A	Α	Α	Α	Α	Α	Α.	Δ.	A	Α.	Α.	A	A A	4 Α	A A	Α	Α				
Res	et 0x0(000000		0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0				
Id	RW	Field													n																		
Α	RW	TEP										Poi	nter	to	task	re	giste	r. A	cce	pts	only	/ ad	dre	sse	s to	re	gist	ers					
												froi	m th	ne T	ask	gro	up.																

22.2.10 CH[3].EEP

Address offset: 0x528

Channel 3 event end-point

Bit r	iumbe	r		31	30	29	28	27	26	25	24	23	22	21 :	20	19	18	17 :	16	15 :	14	13 :	12 :	11 :	10 !	9	8	7	6	5 4	1 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Д	A	Д	A	Δ Α	Α Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																			
Α	RW	EEP										Poi	nte	r to	eve	ent	reg	iste	er. A	Acce	ept	on	ly a	ıddı	ress	es	to r	egi	ster	s				

from the Event group.

22.2.11 CH[3].TEP

Address offset: 0x52C Channel 3 task end-point

Bit r	umb	er		31	30	29 :	28 :	27 :	26	25 :	24	23 :	22 :	21 2	20 1	19 1	18 3	17 1	16 :	15 1	.4 1	13 1	2 1	.1 1	0 9	9 8	3 7	' E	5 5	5 4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	Α	Α.	Α	A .	Δ,	Α.	4 /	Δ,	Δ Α	\ <i>A</i>	Δ Δ		A A	A A	A	Α	A A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () () (0	(0	0	0	0	0 0
Id	RW	Field	Value Id	Va	ue							Des	crip	otio	n																		
Α	RW	TEP										Poir	ntei	r to	tas	k re	gis	ter.	Ac	сер	ts o	nly	ado	dre	sses	to	reg	iste	ers				

Pointer to task register. Accepts only addresses to registers

from the Task group.



22.2.12 CH[4].EEP

Address offset: 0x530

Channel 4 event end-point

Bit r	numb	oer			31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	7 16	5 15	14	13	12	11 1	LO	9	8 7	7	6 5	5 4	4 3	2	1	0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A	A	Α	Α	Α	Α	Α.	Α.	A	A A	Δ,	Α Α	Δ ,	А А	Α	Α	Α
Res	et 0x	(000	000000		A A A A A A O O O O O O O O O O O O O O									0	0	0 (0	0	0	0	0	0	0	0	0	0	0 ()	0 (0 (0 0	0	0	0
Id	RW	V F	ield	Value Id	0 0 0 0 0 0											n																		
Α	RW	/ E	EP										Poi	ntei	r to	eve	nt r	egis	ster	. Ac	сер	ts o	nly a	addı	ess	es	to re	egis	ster	s				

22.2.13 CH[4].TEP

Address offset: 0x534 Channel 4 task end-point

Bit r	umbe	er		31	. 30	29	28	3 27	7 26	5 25	5 24	23	22	21	20	19	18	17 :	16	15 :	L4 1	.3 1	.2 1	1 1) 9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	. A	. A	А	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ.	Δ ,	Α Α	. Δ	. A	Α	Α	Α	Α	Α	Α	A A	ĺ
Res	t Ox0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	llue	2						De	scri	ptic	on																			l
Α	RW	TEP										Ро	inte	r to	ta:	sk re	egis	ter.	. Ac	сер	ts o	nly	ado	dres	ses	to r	egi	ster	S					
												fro	m t	he	Tas	k gr	oup).																

22.2.14 CH[5].EEP

Address offset: 0x538

Channel 5 event end-point

Bit	numb	er		3:	1 30	29	28	3 27	7 26	25	24	23	22	21	20 1	L9 1	L8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	. A	A	Α	Α	Α	Α	Α	Α	Α.	A A	4 <i>A</i>	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	۱ ۸	A A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	V	alue							De	scri	ptic	n																		
Α	RW	EEP										Ро	inte	r to	eve	nt i	regi	ster	. Ac	cept	ts o	nly a	add	res	ses	to i	regi	iste	rs				
												fro	m t	he E	ver	nt gi	rou	٥.															

22.2.15 CH[5].TEP

Address offset: 0x53C Channel 5 task end-point

Bit number 31 30	30 29 28 27 26 25 24	23 22 21 20 19 18 17	7 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id A A	A A A A A A	A	. A A A A A A .	A A A A A A A A A
Reset 0x00000000 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id Value	lue	Description		
A RW TEP		Pointer to task registe	er. Accepts only addresse	es to registers

from the Task group.

22.2.16 CH[6].EEP

Address offset: 0x540 Channel 6 event end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW EEP		Pointer to event register. Accepts only addresses to registers

Pointer to event register. Accepts only addresses to registers

from the Event group.



22.2.17 CH[6].TEP

Address offset: 0x544 Channel 6 task end-point

Bitı	numbe	er		31	30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																			
Α	RW	TEP										Ро	inte	er to	ta	sk r	egi	ster	. A	cce	pts	onl	y ac	ldre	esse	s t	o re	gis	ters					

from the Task group.

22.2.18 CH[7].EEP

Address offset: 0x548 Channel 7 event end-point

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 1	.7 1	16 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	A A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	EEP										Poi	inte	r to	eve	ent	regi	ste	r. A	cce	pts	only	ad	dres	ses	to	reg	iste	ers				
												fro	m tl	he f	ver	nt g	rou	n.															

22.2.19 CH[7].TEP

Address offset: 0x54C Channel 7 task end-point

Bit r	iumbe	er		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20	19 :	18 1	.7 1	.6 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	Α	Α	Α ,	4 /	4 Α	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue	:						De	scri	ptic	on																		
Α	RW	TEP										Ро	inte	r to	tas	k re	gist	er.	Acc	ept	10 2:	nly a	ddr	esse	es t	o re	gis	ters	5				
												fro	m t	he 1	Task	gr	oup.																

22.2.20 CH[8].EEP

Address offset: 0x550

Channel 8 event end-point

Bitı	numbe	er		31	30	29	28	27	26	25 2	24 :	23 :	22 2	21 2	20 1	.9 1	l8 1	.7 1	6 1	5 1	4 1	3 1	2 1	1 10) 9	8	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Δ.	A A	Α,	4 <i>A</i>	A A	Α Α	۸ 4	A A	Α Α	A	. A	Α	Α	Α	Α	Α	A	١.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0) () () () (0	0	0	0	0	0	0	0	0 ()	0 0
Id	RW	Field	Value Id	Va	lue						- 1	Des	crip	tio	n																			
Α	RW	EEP										Poir	nter	to	eve	ntı	regi	ste	r. A	cce	pts	onl	y a	ddre	sse	s to	to	regi	iste	rs				
												-		_																				

from the Event group.

22.2.21 CH[8].TEP

Address offset: 0x554 Channel 8 task end-point

A RW TEP

Bit number		31	30	29	9 2	8 2	7 2	26	25	24	23	22 2	21 :	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	1	0
Id		Α	Α	Α		۱ ۸	Δ.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Reset 0x00000000		0	0	0	C) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
ld RW Field	Value Id	Va	lue	2							Des	crip	otio	n																			

Pointer to task register. Accepts only addresses to registers

from the Task group.



22.2.22 CH[9].EEP

Address offset: 0x558

Channel 9 event end-point

Bit r	numb	oer			31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	7 16	5 15	14	13	12	11 1	LO	9	8 7	7	6 5	5 4	4 3	2	1	0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A	A	Α	Α	Α	Α	Α.	Α.	A	A A	Δ,	Α Α	Δ ,	А А	Α	Α	Α
Res	et 0x	(000	000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 ()	0 (0 (0 0	0	0	0
Id	RW	V F	ield	Value Id	Va	lue							De	scrip	ptio	n																		
Α	RW	/ E	EP										Poi	ntei	r to	eve	nt r	egis	ster	. Ac	сер	ts o	nly a	addı	ess	es	to re	egis	ster	s				

22.2.23 CH[9].TEP

Address offset: 0x55C Channel 9 task end-point

Bit r	iumbe	er		31	. 30	29	28	3 27	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue	:						De	scr	ipti	on																			
Α	RW	TEP										Pc	inte	er to	ta	sk r	egis	ster	. A	cce	pts	onl	y ac	ddre	esse	es t	o re	gis	ters	5				
												fro	om t	he	Tas	k gr	out	D.																

22.2.24 CH[10].EEP

Address offset: 0x560

Channel 10 event end-point

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	7 16	15	14	13	12 :	l1 1	0 !	9 8	3 7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A	Α	Α	Α	Α	Α	A ,	Δ,	Α /	A A	A	. A	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0)) (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																		
Α	RW	EEP										Poi	nte	r to	eve	nt r	egis	ter.	Acc	ept	s or	ıly a	ddr	ess	es t	o re	gist	ers					7
												fro	m th	ne E	ven	t gr	auo.																

22.2.25 CH[10].TEP

Address offset: 0x564

Channel 10 task end-point

Bit number 31 30	30 29 28 27 26 25 24	23 22 21 20 19 18 17	7 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id A A	A A A A A A	A	. A A A A A A .	A A A A A A A A A
Reset 0x00000000 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id Value	lue	Description		
A RW TEP		Pointer to task registe	er. Accepts only addresse	es to registers

from the Task group.

22.2.26 CH[11].EEP

Address offset: 0x568

Channel 11 event end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0										
Id		A A A A A A A A A A A A A A A A A A A										
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										
Id RW Field	Value Id	Value Description										
A RW EEP		Pointer to event register. Accepts only addresses to registers										

Pointer to event register. Accepts only addresses to registers

from the Event group.



22.2.27 CH[11].TEP

Address offset: 0x56C

Channel 11 task end-point

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0										
d	A A A A A A A A A A A A A A A A A A A										
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$										
d RW Field Value Id	Value Description										
A RW TEP Pointer to task register. Accepts only addresses to registers											

from the Task group.

22.2.28 CH[12].EEP

Address offset: 0x570

Channel 12 event end-point

Bit r	numb	er		31	. 30	29	28	3 2	7 26	25	5 24	23	22	21	20	19	18 :	17 :	16 :	15 1	L4 1	.3 1	.2 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Δ ,	Δ ,	۱ ۸	A A	Α	Α	Α	Α	Α	Α	Α	А А
Res	Reset 0x00000000			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue	:						De	scri	ptic	on																		
Α	A RW EEP Pointer to event register. Accepts only addresses to registers																																
			from the Event group.																														

22.2.29 CH[12].TEP

Address offset: 0x574

Channel 12 task end-point

Bit r	numb	er		31	. 30	29	28	27	26	25	24	23	22	21 2	20 1	9 1	8 17	16	15	14	13	12	11 1	.0	9	8	7	6	5	4	3 2	1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A	Α	Α	Α	Α	Α	Α.	Δ.	Α	Α	Α	Α	Α	Α	A A	. 4	A A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	C	0
Id	RW	Field	Value Id	Va	lue							De	scri	otio	n																		
Α	A RW TEP Pointer to task register. Accepts only addresses to registers																																
												fro	m tl	ne T	ask	gro	un.																

22.2.30 CH[13].EEP

Address offset: 0x578

Channel 13 event end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	L6 1	15 1	L4 1	13 :	L2 :	11 :	10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	Α.	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ĺ
Reset 0x00000000				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				ı
Α	A RW EEP Pointer to event register. Accepts only addresses to registers										7																								
															_																				

from the Event group.

22.2.31 CH[13].TEP

Address offset: 0x57C

Channel 13 task end-point

Bit number	31 30 2	9 28 27 26 25 24 23 2	22 21 20 19 18 17 16	5 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id	A A A	4 A A A A A A A	A A A A A A	A A A A A A	A A A A A A A A
Reset 0x00000000	0 0 0	0000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field Value	ld Value	Desc	cription		

RW TEP Pointer to task register. Accepts only addresses to registers

from the Task group.



22.2.32 CH[14].EEP

Address offset: 0x580

Channel 14 event end-point

Bit r	iumb	er		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18 :	17 1	16 :	15 1	L4 :	L3 1	12 1	1 1	0 9) 8	7	6	5	4	3	2	1	5
Id				Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	A A	A A	\ A		A	Α	Α	Α	Α	Α	A .	Δ
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () () (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	A A A 0 0 0								De	scri	ptic	on																			ı
Α	RW	EEP		0 0 0								Ро	inte	r to	ev	ent	reg	iste	r. A	Acce	pts	on	ly a	ddr	esse	es t	o re	gist	ers					7
												fro	m t	he I	Eve	nt g	rou	p.																

22.2.33 CH[14].TEP

Address offset: 0x584

Channel 14 task end-point

Bit r	numb	er		31	. 30	29	28	3 2	7 26	5 25	5 24	23	3 22	21	20	19	18	17	16	15	14 :	13 1	L2 1	11:	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Δ	A	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	Д	Α.	Α	Α.	Α	Α	Α	Α	A A	A 4	A A
Res	et Ox	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	alue	:						De	escr	pti	on																			
Α	RW	TEP										Po	inte	er to	ta:	sk r	egis	ter	. Ac	cep	ts c	nly	ad	dre	sse	s to	re	gist	ers					
												fro	om t	he	Tas	k gr	oup).																

22.2.34 CH[15].EEP

Address offset: 0x588

Channel 15 event end-point

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	7 16	15	14	13	12 :	l1 1	0 !	9 8	3 7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A	Α	Α	Α	Α	Α	A ,	Δ,	Α /	A A	A	. A	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0)) (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																		
Α	RW	EEP										Poi	nte	r to	eve	nt r	egis	ter.	Acc	ept	s or	ıly a	ddr	ess	es t	o re	gist	ers					7
												fro	m th	ne E	ven	t gr	auo.																

22.2.35 CH[15].TEP

Address offset: 0x58C

Channel 15 task end-point

Bit r	iumbe	r		31	30	29	28	27	26	25	24	23	22	21 :	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۸ ۸	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																			
Α	RW	TEP										Poi	nte	r to	tas	k re	egis	ter.	. Ac	cep	ots	only	/ ac	ldre	esse	s to	o re	gis	ters	5				

from the Task group.

22.2.36 CH[16].EEP

Address offset: 0x590

Channel 16 event end-point

Bit number		31	30	29	9 2	8 2	7 2	26	25	24	23	22 2	21 :	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	1	0
Id		Α	Α	Α		۱ ۸	Δ.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Reset 0x00000000		0	0	0	C) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
ld RW Field	Value Id	Va	lue	2							Des	crip	otio	n																			

A RW EEP Pointer to event register. Accepts only addresses to registers

from the Event group. $% \label{eq:from_prop_state}% % \label{eq:from_prop_state}%$



22.2.37 CH[16].TEP

Address offset: 0x594

Channel 16 task end-point

Bitı	numbe	er		3:	1 30	29	9 2	8 2	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α		Δ,	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et OxC	0000000		0	0	0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	A A A 0 0 0 Value									De	scri	ptic	on																				
Α	RW	TEP		A A 0 0									Poi	inte	r to	ta	sk r	egis	ster	. A	cce	pts	onl	y a	ddr	esse	es to	o re	gis	ters	5					
														m t																						

22.2.38 CH[17].EEP

Address offset: 0x598

Channel 17 event end-point

Bit r	iumbe	er		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue	•						De	scri	ptic	on																			
Α	RW	EEP										Ро	inte	r to	ev	ent	reg	giste	er. A	Acc	ept	s or	nly a	add	res	ses	to	reg	iste	rs				
												fro	m t	he	Eve	nt g	rou	ıp.																

22.2.39 CH[17].TEP

Address offset: 0x59C

Channel 17 task end-point

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 A	Α	Α	Α	Α	Α	A	4 Α	Δ Δ	Α	Α	Α	Α	Α	Α	A A	. 4	А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	TEP										Poi	nter	to	task	regi	ste	r. A	ccep	ots (only	ado	dres	ses 1	to re	egis	ters	5				
												froi	m th	e T	ask g	rou	p.															

22.2.40 CH[18].EEP

Address offset: 0x5A0

Channel 18 event end-point

Bit r	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 18	3 17	16	15	14	13 1	2 1:	10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	ΑА	A	Α	Α	Α	Α	A A	A	Α	Α	Α	Α	Α	Α	Α	А А	. 4	A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	RW	EEP										Poi	nter	to	ever	nt re	egist	er.	Acc	ept:	s onl	y ac	ldre	sses	to	reg	iste	rs				
												froi	m th	ne E	vent	gro	oup.															

22.2.41 CH[18].TEP

Address offset: 0x5A4 Channel 18 task end-point

В	Sit number		31	. 30	29	2	8 2	7 2	6 2	25 2	24 2	23 2	22 2	21 2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 1	1 1	.0 9	9 8	7	6	5	4	3	2 1	1 0
lo	d		Α	Α	Α	Δ		Δ Α	Δ.	Α.	Α	Α	Α.	Α,	Δ ,	Δ ,	Δ Δ	A A	A A	A A	Δ Α	۸ ۸	Δ ,	Δ ,	4 4	A A	A	Α	Α	Α	Α ,	4 Α	A A
R	Reset 0x00000000		0	0	0	0) () (0	0	0	0	0	0	0 (0 (0) () (0	0) (0 (0 (0 () (0	0	0	0	0	0 (0 0
le	d RW Field	Value Id	Va	lue							ı	Des	crip	tio	n																		

A RW TEP Pointer to task register. Accepts only addresses to registers

from the Task group.



22.2.42 CH[19].EEP

Address offset: 0x5A8

Channel 19 event end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	16	15	14	13	12 :	1 1	0 9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Α Α	A	Α	Α	Α	Α	Α	Α ,	Α Δ	. Α	A	Α	Α	Α	Α	Α	A	Δ
Re	set 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (o
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	EEP										Poi	nter	to	eve	nt r	egis	ter.	Acc	ept	s or	ıly a	ddr	esse	es to	o re	gist	ers					7

from the Event group.

22.2.43 CH[19].TEP

Address offset: 0x5AC Channel 19 task end-point

Bit r	numbe	er		31	1 30	29	2	8 2	7 2	6 2	25 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	. 4	\ A	۸ 4	Δ.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et OxC	0000000	0 0 0 Value Id Value							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	A A A O O O Value Id Value										Des	cri	otic	on																				
Α	RW	TEP						Poi	nte	r to	ta	sk r	egi	stei	r. A	cce	pts	on	ly a	ddr	esse	es to	o re	gis	ter	s					_					

22.2.44 CHG[0]

Address offset: 0x800 Channel group 0

		o. g. cap c																															
Bit	numb	er		31	1 30	29	28	27	26	25 :	24	23	22 2	21 :	20 1	19 1	18 :	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	V	U .	Т	S	R	Q	Р	О	N N	ΛL	. K	J	1	Н	G	F	E I) (В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue						ı	De	scrip	otio	n																		
Α	RW	CH0									- 1	Inc	clude	or	exc	lud	e c	har	ne	Ι0													
			Excluded	0							ı	Exc	clude	9																			
			Included	1							-	Inc	clude	•																			
В	RW	CH1									- 1	Inc	clude	or	exc	lud	e c	har	ne	l 1													
			Excluded	0							ı	Exc	clude	9																			
			Included	1							-	Inc	clude	:																			
С	RW	CH2									-	Inc	clude	or	exc	lud	e c	har	ne	12													
			Excluded	0							ı	Exc	clude	9																			
			Included	1							ı	Inc	clude	•																			
D	RW	CH3										Inc	clude	or	exc	lud	e c	har	ne	13													
			Excluded	0							- 1	Exc	clude	9																			
			Included	1							ı	Inc	clude	•																			
E	RW	CH4									ı	Inc	clude	or	exc	lud	e c	har	ne	l 4													
			Excluded	0							ı	Exc	clude	9																			
			Included	1							ı	Inc	clude	•																			
F	RW	CH5									- 1	Inc	clude	or	exc	lud	e c	har	ne	15													
			Excluded	0							١	Exc	clude	9																			
			Included	1							ı	Inc	clude	•																			
G	RW	CH6									-	Inc	clude	or	exc	lud	e c	har	ne	l 6													
			Excluded	0							١	Exc	clude	9																			
			Included	1							ı	Inc	clude	•																			
Н	RW	CH7									- 1	Inc	clude	or	exc	lud	e c	har	ne	۱7													
			Excluded	0							- 1	Exc	clude	9																			
			Included	1							ı	Inc	clude	•																			
I	RW	CH8									١	Inc	clude	or	exc	lud	e c	har	ne	l 8													
			Excluded	0							-	Exc	clude	9																			



Bit r	numb	er		31 30	29 28	27 26	25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	ΖY	/ X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et OxC	00000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Included	1				Include
J	RW	CH9						Include or exclude channel 9
			Excluded	0				Exclude
.,			Included	1				Include
K	RW	CH10	Football d	0				Include or exclude channel 10
			Excluded Included	0				Exclude Include
L	RW	CH11	included	1				Include or exclude channel 11
_		011	Excluded	0				Exclude
			Included	1				Include
М	RW	CH12						Include or exclude channel 12
			Excluded	0				Exclude
			Included	1				Include
N	RW	CH13						Include or exclude channel 13
			Excluded	0				Exclude
			Included	1				Include
0	RW	CH14						Include or exclude channel 14
			Excluded	0				Exclude
	DIA	CHAF	Included	1				Include
Р	KW	CH15	Evaludad	0				Include or exclude channel 15
			Excluded Included	1				Exclude Include
Q	RW	CH16	included	1				Include or exclude channel 16
~		0.110	Excluded	0				Exclude
			Included	1				Include
R	RW	CH17						Include or exclude channel 17
			Excluded	0				Exclude
			Included	1				Include
S	RW	CH18						Include or exclude channel 18
			Excluded	0				Exclude
			Included	1				Include
Т	RW	CH19						Include or exclude channel 19
			Excluded	0				Exclude
	D\A/	CU20	Included	1				Include Include or exclude channel 20
U	KVV	CH20	Excluded	0				Exclude
			Included	1				Include
V	RW	CH21		-				Include or exclude channel 21
			Excluded	0				Exclude
			Included	1				Include
W	RW	CH22						Include or exclude channel 22
			Excluded	0				Exclude
			Included	1				Include
Χ	RW	CH23						Include or exclude channel 23
			Excluded	0				Exclude
			Included	1				Include
Υ	RW	CH24						Include or exclude channel 24
			Excluded	0				Exclude
7	D\A/	CH25	Included	1				Include
Z	KVV	CH25	Excluded	0				Include or exclude channel 25 Exclude
			Included	1				Include
а	RW	CH26		_				Include or exclude channel 26
			Excluded	0				Exclude
			Included	1				Include



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZ'	Y X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
b RW CH27			Include or exclude channel 27
	Excluded	0	Exclude
	Included	1	Include
c RW CH28			Include or exclude channel 28
	Excluded	0	Exclude
	Included	1	Include
d RW CH29			Include or exclude channel 29
	Excluded	0	Exclude
	Included	1	Include
e RW CH30			Include or exclude channel 30
	Excluded	0	Exclude
	Included	1	Include
f RW CH31			Include or exclude channel 31
	Excluded	0	Exclude
	Included	1	Include

22.2.45 CHG[1]

Address offset: 0x804 Channel group 1

Bit r	numbe	er		31	30	29 28	8 27	26	25 2	4 :	23 22 21 2	20 19	18	17	16 1	5 14	13	12 1	.1 10	9	8	7	6 !	5 4	1 3	2	1 0
Id				f	e	d c	b	а	ΖY	Y	x w v	U T	S	R	Q I	9 0	N	М	L K	J	ī	Н	G I	= E	D	С	ВА
Res	et 0x0	0000000		0	0	0 0	0	0	0 ()	0 0 0	0 0	0	0	0 (0 0	0	0 (0 0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Va	lue					ı	Descriptio	n															
Α	RW	CH0								-	nclude or	exclu	de (char	nnel	0											
			Excluded	0						ı	Exclude																
			Included	1						ı	nclude																
В	RW	CH1								ı	nclude or	exclu	de (char	nnel	1											
			Excluded	0						ı	Exclude																
			Included	1						ı	nclude																
С	RW	CH2								-	nclude or	exclu	de (char	nnel	2											
			Excluded	0						ı	Exclude																
			Included	1						ı	nclude																
D	RW	CH3								-	nclude or	exclu	de (char	nel	3											
			Excluded	0						ı	Exclude																
			Included	1						ı	nclude																
Ε	RW	CH4								-	nclude or	exclu	de (char	nnel	4											
			Excluded	0						١	Exclude																
			Included	1						ı	nclude																
F	RW	CH5								-	nclude or	exclu	de (char	nnel	5											
			Excluded	0						١	Exclude																
			Included	1						١	nclude																
G	RW	CH6								-	nclude or	exclu	de (char	nnel	6											
			Excluded	0						١	Exclude																
			Included	1						ı	nclude																
Н	RW	CH7								ı	nclude or	exclu	de (char	nnel	7											
			Excluded	0						١	Exclude																
			Included	1						ı	nclude																
1	RW	CH8								ı	nclude or	exclu	de (char	nnel	8											
			Excluded	0						١	Exclude																
			Included	1						١	nclude																
J	RW	CH9								-	nclude or	exclu	de (char	nnel	9											
			Excluded	0						١	Exclude																
			Included	1						- 1	nclude																



Bit r	number		31 30 29 28 27 2	
Id				a ZYXWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
K	RW CH10			Include or exclude channel 10
		Excluded	0	Exclude
		Included	1	Include
L	RW CH11			Include or exclude channel 11
		Excluded	0	Exclude
		Included	1	Include
М	RW CH12			Include or exclude channel 12
		Excluded	0	Exclude
		Included	1	Include
N	RW CH13			Include or exclude channel 13
		Excluded	0	Exclude
		Included	1	Include
0	RW CH14			Include or exclude channel 14
		Excluded	0	Exclude
		Included	1	Include
Р	RW CH15			Include or exclude channel 15
		Excluded	0	Exclude
		Included	1	Include
Q	RW CH16			Include or exclude channel 16
-		Excluded	0	Exclude
		Included	1	Include
R	RW CH17			Include or exclude channel 17
-		Excluded	0	Exclude
		Included	1	Include
S	RW CH18	meladea	-	Include or exclude channel 18
5	NW CITIO	Excluded	0	Exclude
		Included	1	Include
Т	RW CH19	meladea	1	Include or exclude channel 19
•	NW CITES	Excluded	0	Exclude
		Included	1	Include
U	RW CH20	meladea	<u>.</u>	Include or exclude channel 20
U	NW CH20	Excluded	0	Exclude Exclude
		Included	1	Include
V	RW CH21	ilicidaed	1	Include or exclude channel 21
٧	NW CHZI	Excluded	0	Exclude Channel 21
		Included	1	Include
۱۸/	RW CH22	included	1	Include Include or exclude channel 22
W	RVV CH22	Evaludad	0	
		Excluded	0	Exclude
v	DW CH33	Included	1	Include
X	RW CH23	Evoluded	0	Include or exclude channel 23
		Excluded	0	Exclude
V	DW CH24	Included	1	Include
Υ	RW CH24		0	Include or exclude channel 24
		Excluded	0	Exclude
-	DIA 6::25	Included	1	Include
Z	RW CH25			Include or exclude channel 25
		Excluded	0	Exclude
		Included	1	Include
а	RW CH26			Include or exclude channel 26
		Excluded	0	Exclude
		Included	1	Include
b	RW CH27			Include or exclude channel 27
		Excluded	0	Exclude
		Included	1	Include
С	RW CH28			Include or exclude channel 28



Bitı	numbe	r		31	30	29	28 2	27 2	26 2	25 2	24 2	3 22	21	20	19	18 :	17 1	16 1	L5 1	l4 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id				f	e	d	С	b	а	Z	Υ)	(W	٧	U	Т	S	R (Q	Р	1 0	I M	L	K	J	1	Н	G	F E	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Val	lue						C	escr	iptio	on																		
			Excluded	0							Е	xclu	de																			
			Included	1 Include Include or exclude channel 29																												
d	RW	CH29		Include or exclude channel 29																												
			Excluded	0							E	xclu	de																			
			Included	1							b	nclud	le																			
е	RW	CH30									li	nclud	le o	ex	clud	le c	han	nel	30													
			Excluded	0							Е	xclu	de																			
			Included	1							li	nclud	le																			
f	RW	CH31									b	nclud	le o	ex	clud	le c	han	nel	31													
			Excluded	0							E	xclu	de																			
			Included	1							b	nclud	le																			

22.2.46 CHG[2]

Address offset: 0x808 Channel group 2

011	am	iei group z																														
Bit	numb	er		3	1 30	0 29	9 28	27	26 2	25 2	4 2	23 22	21	20	19	18	17	16	15	14	13	12 :	11 1	0 9	9 8	3 7	6	5	4	3	2	1
Id				f	е	e d	l c	b	а	ZΥ	/ :	X W	٧	U	Т	S	R	Q	Р	0	N	M	L	〈 J		Н	G	F	Ε	D	С	В.
Res	et 0x0	0000000		0	0	0	0	0	0	0 ()	0 0	0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alu	e						Descri	ptic	on																		
Α	RW	CH0									ı	nclud	e or	ex	cluc	le c	har	ne	10													
			Excluded	0							E	xclud	e																			
			Included	1							ı	nclud	9																			
В	RW	CH1									- 1	nclud	e or	ex	cluc	le c	har	ne	l 1													
			Excluded	0							E	xclud	e																			
			Included	1							- 1	nclud	9																			
С	RW	CH2									- 1	nclud	e or	ex	cluc	le c	har	ne	12													
			Excluded	0							E	xclud	e																			
			Included	1							I	nclud	9																			
D	RW	CH3									-1	nclud	e or	ex	cluc	le c	har	ne	13													
			Excluded	0							E	xclud	e																			
			Included	1							-1	nclud	9																			
Е	RW	CH4									ı	nclud	e or	ex	cluc	le c	har	ne	۱4													
			Excluded	0							E	Exclud	e																			
			Included	1							ı	nclud	9																			
F	RW	CH5									ı	nclud	e or	ex	cluc	le c	har	ne	15													
			Excluded	0							E	xclud	е																			
			Included	1							-1	nclud	9																			
G	RW	CH6									I	nclud	e or	ex	clud	le c	har	ne	۱6													
			Excluded	0							E	Exclud	e																			
			Included	1							I	nclud	9																			
Н	RW	CH7									-1	nclud	e or	ex	clud	le c	har	ne	17													
			Excluded	0							E	Exclud	e																			
			Included	1							- 1	nclud	9																			
1	RW	CH8									I	nclud	e or	ex	cluc	le c	har	ne	18													
			Excluded	0							E	xclud	e																			
			Included	1							I	nclud	e																			
J	RW	CH9									- 1	nclud	e or	ex	cluc	le c	har	ne	19													
			Excluded	0							E	xclud	e																			
			Included	1							- 1	nclud	е																			
K	RW	CH10									I	nclud	e or	ex	cluc	le c	har	ne	110)												
			Excluded	0							E	xclud	e																			
			Included	1							ı	nclud	е																			
L	RW	CH11									- 1	nclud	e or	ex	cluc	le c	har	ne	l 11													



Bit r	numbe	er		31 30	29 28	27 26	5 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	ΖY	Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Excluded	0				Exclude
			Included	1				Include
М	RW	CH12	Freshode d	0				Include or exclude channel 12
			Excluded Included	0				Exclude Include
N	R\M	CH13	included	1				Include or exclude channel 13
	11.00	CHIS	Excluded	0				Exclude
			Included	1				Include
0	RW	CH14						Include or exclude channel 14
			Excluded	0				Exclude
			Included	1				Include
Р	RW	CH15						Include or exclude channel 15
			Excluded	0				Exclude
			Included	1				Include
Q	RW	CH16						Include or exclude channel 16
			Excluded	0				Exclude
			Included	1				Include
R	RW	CH17						Include or exclude channel 17
			Excluded	0				Exclude
	DIA	CUAO	Included	1				Include
S	RW	CH18	Foodbade d	0				Include or exclude channel 18
			Excluded Included	0				Exclude Include
Т	RW	CH19	included	1				Include or exclude channel 19
	11.00	CHIS	Excluded	0				Exclude
			Included	1				Include
U	RW	CH20						Include or exclude channel 20
			Excluded	0				Exclude
			Included	1				Include
V	RW	CH21						Include or exclude channel 21
			Excluded	0				Exclude
			Included	1				Include
W	RW	CH22						Include or exclude channel 22
			Excluded	0				Exclude
			Included	1				Include
X	RW	CH23						Include or exclude channel 23
			Excluded	0				Exclude
V	D\A/	CH34	Included	1				Include Include or exclude channel 24
Υ	κvv	CH24	Excluded	0				Exclude Exclude
			Included	1				Include
Z	RW	CH25		-				Include or exclude channel 25
			Excluded	0				Exclude
			Included	1				Include
a	RW	CH26						Include or exclude channel 26
			Excluded	0				Exclude
			Included	1				Include
b	RW	CH27						Include or exclude channel 27
			Excluded	0				Exclude
			Included	1				Include
С	RW	CH28						Include or exclude channel 28
			Excluded	0				Exclude
			Included	1				Include
d	RW	CH29	5 1 1 1	•				Include or exclude channel 29
			Excluded	0				Exclude



Bit	numbe	er		31	30 2	9 2	28 27	7 26	25	24	23	22 2	21 2	20 1	.9 18	3 17	16	15	14 1	3 12	11	10	9	8 7	' E	5	4	3	2	1 0
Id				f	e d	ł	c b	а	Z	Υ	Χ	W	Vι	U T	T S	R	Q	Р	0 1	N M	L	K	J	I F	I	F	Ε	D	С	ВА
Res	et 0x0	0000000		0	0 ()	0 0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	scrip	otio	n																
			Included	1							Inc	lude	:																	
е	RW	CH30									Inc	lude	or	exc	lude	cha	nne	1 30												
			Excluded	0							Exc	clude	9																	
			Included	1							Inc	lude																		
f	RW	CH31									Inc	lude	or	exc	lude	cha	nne	l 31												
			Excluded	0							Exc	clude	9																	
			Included	1							Inc	lude	:																	

22.2.47 CHG[3]

Address offset: 0x80C Channel group 3

Cn	ann	iel group 3																										
Bit	numb	er		31 30	29 2	8 27	7 26	25 24	1 23	3 22 2	1 20	19	18	17 :	16	15 :	14 1	3 12	2 11	10	9	8	7 6	5	4	3	2 :	L 0
Id				f e	d	c b	а	Z Y	X	w v	/ U	Т	S	R	Q	Р	1 0	۱ N	1 L	K	J	L	1 6	F	Ε	D	C E	3 A
Res	et 0x0	00000000		0 0	0 (0 0	0	0 0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0 (0
Id	RW	Field	Value Id	Value	,				D	escript	tion																	
Α	RW	CH0							In	ıclude	or e	xclu	de d	han	nne	I 0												
			Excluded	0					E>	kclude																		
			Included	1					In	clude																		
В	RW	CH1							In	clude	or e	xclu	de d	han	nne	l 1												
			Excluded	0					E>	kclude																		
			Included	1					In	clude																		
С	RW	CH2							In	clude	or e	xclu	de d	han	ne	12												
			Excluded	0					E>	kclude																		
			Included	1					In	clude																		
D	RW	CH3							In	clude	or e	xclu	de d	han	ne	13												
			Excluded	0					E>	kclude																		
			Included	1					In	clude																		
Е	RW	CH4							In	clude	or e	xclu	de d	han	ne	l 4												
			Excluded	0					E>	kclude																		
			Included	1					In	clude																		
F	RW	CH5							In	clude	or e	xclu	de d	han	ne	15												
			Excluded	0					E>	kclude																		
			Included	1					In	clude																		
G	RW	CH6							In	clude	or e	xclu	de d	han	ne	l 6												
			Excluded	0					E>	kclude																		
			Included	1					In	clude																		
Н	RW	CH7								ıclude	or e	xclu	de d	han	nne	17												
			Excluded	0						kclude																		
			Included	1						iclude																		
I	RW	CH8								ıclude	or e	xclu	de d	han	nne	18												
			Excluded	0						kclude																		
			Included	1						clude																		
J	RW	CH9		_						iclude	or e	xclu	de d	han	nne	19												
			Excluded	0						kclude 																		
			Included	1						clude																		
K	RW	CH10	5 1 1 1	•						ıclude	or e	xclu	de d	han	ine	ı 10												
			Excluded	0						kclude																		
	Dia	CU111	Included	1						clude			al a			111												
L	KW	CH11	Eveluded	0						ıclude	or e	xclu	de d	han	ine	ı 11												
			Excluded	0						kclude																		
	D. A.	CU12	Included	1						clude																		
М	КW	CH12	Evelvedeed	0						ıclude	or e	xclu	ae c	nan	ine	112												
			Excluded	0					E	kclude																		



Bit n	umbe	er		31 30	29 2	8 27	26 2	25 24	23 22 21 20 19	9 18	17 3	16 15	5 14	13 1	2 11	10	9 8	7	6	5 4	3	2 1	0
Id				f e	d d	c b	a Z	Z Y	X W V U T	S	R	Q P	0	N N	ΛL	K	JI	Н	G	F E	D	C E	3 A
Rese	t 0x0	0000000		0 0	0 (0 0	0 (0 0	0 0 0 0 0	0	0	0 0	0	0 (0	0	0 0	0	0	0 0	0	0 () 0
ld	RW	Field	Value Id	Value					Description														
			Included	1					Include														
N	RW	CH13							Include or exclu	ude	chan	inel :	L3										
			Excluded	0					Exclude														
			Included	1					Include														
0	RW	CH14							Include or exclu	ude	chan	inel :	L4										
			Excluded	0					Exclude														
			Included	1					Include														
Р	RW	CH15							Include or exclu	ude	chan	inel :	L5										
			Excluded	0					Exclude														
			Included	1					Include														
Q	RW	CH16							Include or exclu	ude	chan	inel :	16										
			Excluded	0					Exclude														
			Included	1					Include														
R	RW	CH17							Include or exclu	ude	chan	inel :	L7										
			Excluded	0					Exclude														
			Included	1					Include														
S	RW	CH18							Include or exclu	ude	chan	inel :	L8										
			Excluded	0					Exclude														
			Included	1					Include														
T	RW	CH19							Include or exclu	ude	chan	inel :	L9										
			Excluded	0					Exclude														
			Included	1					Include														
U	RW	CH20							Include or exclu	ude	chan	inel 2	20										
			Excluded	0					Exclude														
			Included	1					Include														
V	RW	CH21							Include or exclu	ude	chan	inel 2	21										
			Excluded	0					Exclude														
			Included	1					Include														
W	RW	CH22		_					Include or exclu	ude	chan	inel 2	22										
			Excluded	0					Exclude														
.,	5111		Included	1					Include														
Х	RW	CH23							Include or exclu	ude	chan	inel 2	23										
			Excluded	0					Exclude														
.,	5111		Included	1					Include														
Υ	RW	CH24	5 1 1 1						Include or exclu	ude	chan	inel 2	24										
			Excluded	0					Exclude														
7	DIA	CURE	Included	1					Include				٠-										
Z	KVV	CH25	Final radia d	0					Include or exclu	uae	cnan	inei 2	25										
			Excluded	0					Exclude														
_	DIA	CHac	Included	1					Include														
а	ĸw	CH26	Evaludad	0					Include or exclu	uue	unan	mel 2	20										
			Excluded	0					Exclude														
	DIM	CURT	Included	1					Include														
b	RW	CH27	5 1 1 1	•					Include or exclu	ude	chan	inel 2	2/										
			Excluded	0					Exclude														
_	DVA	CH30	Included	1					Include	ء اي	che	no! 1	0										
С	ĸw	CH28	Evaludad	0					Include or exclu	uue	unan	mel 2	ō										
			Excluded	0					Exclude														
d	DV	CU20	Included	1					Include	ر اس	ak.	m - 1 -	10										
d	ĸW	CH29	Evaluded	0					Include or exclu	ude	cnan	inel 2	29										
			Excluded	0					Exclude														
	Divi	CU20	Included	1					Include														
е	кW	CH30	Freshode d	0					Include or exclu	uae	cnan	inel 3	sU										
			Excluded	0					Exclude														
			Included	1					Include														



Bit r	numbe	r		31	1 30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	L8 1	l7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S	R (Q F	· (N	М	L	K	J	L	Н	G	F	Ε	D (Э В	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	alue							De	scri	ptio	n																		
f	RW	CH31										Inc	lude	e or	exc	lud	e cl	hanı	nel	31													
			Excluded	0								Exc	lud	e																			
			Included	1								Inc	lude	9																			

22.2.48 CHG[4]

Address offset: 0x810 Channel group 4

OII	aiiii	iei group 4																													
Bit r	numbe	er		31 30	29	28 2	27 20	5 2	5 24	1 2	23 22 21	L 20	19	18	17	16	15	14	13	12	11 1	10 9	9 8	3 7	6	5	4	3	2	1	C
Id				f e	d	С	b a	2	Z Y)	x w v	U	Т	S	R	Q	Р	0	Ν	М	L	K J		Н	(F	Е	D	С	В	1
Res	et OxC	0000000		0 0	0	0	0 0	(0 0	(0 0 0	0	0	0	0	0	0	0	0	0	0	0 0) (0	C	0	0	0	0	0	(
Id	RW	Field	Value Id	Value	!					C	Descript	ion																			
Α	RW	CH0								li	nclude d	or ex	kclu	de c	har	ne	Ι0														
			Excluded	0						E	xclude																				
			Included	1						li	nclude																				
В	RW	CH1								h	nclude d	or ex	kclu	de c	har	ne	l 1														
			Excluded	0						Е	xclude																				
			Included	1						li	nclude																				
С	RW	CH2								li	nclude d	or ex	kclu	de c	har	ne	12														
			Excluded	0						E	xclude																				
			Included	1						li	nclude																				
D	RW	CH3								li	nclude d	or ex	kclu	de c	har	ne	13														
			Excluded	0						E	xclude																				
			Included	1						li	nclude																				
Е	RW	CH4								li	nclude d	or ex	kclu	de c	har	ne	l 4														
			Excluded	0						E	xclude																				
			Included	1						li	nclude																				
F	RW	CH5								h	nclude o	or ex	kclu	de c	har	ne	l 5														
			Excluded	0						E	xclude																				
			Included	1						li	nclude																				
G	RW	CH6								li	nclude o	or ex	kclu	de c	har	ne	l 6														
			Excluded	0						E	xclude																				
			Included	1						li	nclude																				
Н	RW	CH7								li	nclude o	or ex	kclu	de c	har	ne	۱7														
			Excluded	0						Е	xclude																				
			Included	1						li	nclude																				
I	RW	CH8								li	nclude o	or ex	kclu	de c	har	ne	l 8														
			Excluded	0						E	xclude																				
			Included	1							nclude																				
J	RW	CH9								li	nclude o	or ex	kclu	de c	har	ne	19														
			Excluded	0							xclude																				
			Included	1						li	nclude																				
K	RW	CH10								li	nclude o	or ex	kclu	de c	har	ne	110)													
			Excluded	0							xclude																				
			Included	1						li	nclude																				
L	RW	CH11									nclude o	or ex	kclu	de c	har	ne	l 11														
			Excluded	0							xclude																				
			Included	1							nclude																				
M	RW	CH12									nclude o	or ex	kclu	de c	har	ne	l 12	!													
			Excluded	0							xclude																				
			Included	1							nclude																				
N	RW	CH13									nclude o	or ex	kclu	de c	har	ne	l 13	3													
			Excluded	0							xclude																				
			Included	1						li	nclude																				



Bit r	numbe	er		31 30	29 28	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	idilibe	-1						X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000						0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
0	RW	CH14						Include or exclude channel 14
			Excluded	0				Exclude
			Included	1				Include
Р	RW	CH15						Include or exclude channel 15
			Excluded	0				Exclude
			Included	1				Include
Q	RW	CH16						Include or exclude channel 16
			Excluded	0				Exclude
			Included	1				Include
R	RW	CH17						Include or exclude channel 17
			Excluded	0				Exclude
_	DIA	CUAO	Included	1				Include
S	RW	CH18	Excluded	0				Include or exclude channel 18 Exclude
			Included	1				Include
Т	R\M/	CH19	included	1				Include or exclude channel 19
	IVVV	C1113	Excluded	0				Exclude
			Included	1				Include
U	RW	CH20	moladea	-				Include or exclude channel 20
			Excluded	0				Exclude
			Included	1				Include
٧	RW	CH21						Include or exclude channel 21
			Excluded	0				Exclude
			Included	1				Include
W	RW	CH22						Include or exclude channel 22
			Excluded	0				Exclude
			Included	1				Include
Х	RW	CH23						Include or exclude channel 23
			Excluded	0				Exclude
			Included	1				Include
Υ	RW	CH24						Include or exclude channel 24
			Excluded	0				Exclude
			Included	1				Include
Z	RW	CH25						Include or exclude channel 25
			Excluded	0				Exclude
			Included	1				Include
а	RW	CH26	5 1 1 1					Include or exclude channel 26
			Excluded	0				Exclude
b	D\A/	CH27	Included	1				Include Include or exclude channel 27
D	IV V V	CH27	Excluded	0				Exclude Exclude
			Included	1				Include
С	RW/	CH28	included	-				Include or exclude channel 28
		C1120	Excluded	0				Exclude
			Included	1				Include
d	RW	CH29						Include or exclude channel 29
			Excluded	0				Exclude
			Included	1				Include
e	RW	CH30						Include or exclude channel 30
			Excluded	0				Exclude
			Included	1				Include
f	RW	CH31						Include or exclude channel 31
			Excluded	0				Exclude
			Included	1				Include



22.2.49 CHG[5]

Address offset: 0x814 Channel group 5

		iloup 5			
	number				5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					ZYXWVUTSRQPONMLKJIHGFEDCBA
	et 0x00000				000000000000000000000000000000000000000
Id	RW Fiel		Value Id	Value	Description
Α	RW CHO				Include or exclude channel 0
			Excluded	0	Exclude
			Included	1	Include
В	RW CH1				Include or exclude channel 1
			Excluded	0	Exclude
			Included	1	Include
С	RW CH2				Include or exclude channel 2
			Excluded	0	Exclude
			Included	1	Include
D	RW CH3				Include or exclude channel 3
			Excluded	0	Exclude
			Included	1	Include
Ε	RW CH4				Include or exclude channel 4
			Excluded	0	Exclude
			Included	1	Include
F	RW CH5				Include or exclude channel 5
			Excluded	0	Exclude
			Included	1	Include
G	RW CH				Include or exclude channel 6
			Excluded	0	Exclude
			Included	1	Include
Н	RW CH7				Include or exclude channel 7
			Excluded	0	Exclude
			Included	1	Include
I	RW CH				Include or exclude channel 8
			Excluded	0	Exclude
			Included	1	Include
J	RW CHS				Include or exclude channel 9
			Excluded	0	Exclude
			Included	1	Include
K	RW CH1	0			Include or exclude channel 10
			Excluded	0	Exclude
			Included	1	Include
L	RW CH1	1			Include or exclude channel 11
			Excluded	0	Exclude
			Included	1	Include
М	RW CH1	2			Include or exclude channel 12
			Excluded	0	Exclude
			Included	1	Include
N	RW CH1	.3			Include or exclude channel 13
			Excluded	0	Exclude
			Included	1	Include
0	RW CH1	4			Include or exclude channel 14
			Excluded	0	Exclude
			Included	1	Include
Р	RW CH1	5			Include or exclude channel 15
			Excluded	0	Exclude
			Included	1	Include
Q	RW CH1	6			Include or exclude channel 16
			Excluded	0	Exclude



Bit n	umbe	r		31 30 2	9 28 27	7 26 25	24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	t 0x0	0000000		0 0 0	0 0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Included	1				Include
R	RW	CH17						Include or exclude channel 17
			Excluded	0				Exclude
			Included	1				Include
S	RW	CH18						Include or exclude channel 18
			Excluded	0				Exclude
			Included	1				Include
Т	RW	CH19						Include or exclude channel 19
			Excluded	0				Exclude
			Included	1				Include
U	RW	CH20						Include or exclude channel 20
			Excluded	0				Exclude
			Included	1				Include
V	RW	CH21						Include or exclude channel 21
			Excluded	0				Exclude
			Included	1				Include
W	RW	CH22						Include or exclude channel 22
			Excluded	0				Exclude
			Included	1				Include
X	RW	CH23						Include or exclude channel 23
			Excluded	0				Exclude
.,			Included	1				Include
Υ	RW	CH24	5 1 1 1	•				Include or exclude channel 24
			Excluded	0				Exclude
7	D\A/	CHAE	Included	1				Include
Z	KVV	CH25	Excluded	0				Include or exclude channel 25 Exclude
			Included	1				Include
a	D\A/	CH26	included	1				Include or exclude channel 26
a	IVV	CHZO	Excluded	0				Exclude
			Included	1				Include
b	RW	CH27	meladed	•				Include or exclude channel 27
		01127	Excluded	0				Exclude
			Included	1				Include
С	RW	CH28		=				Include or exclude channel 28
-		-	Excluded	0				Exclude
			Included	1				Include
d	RW	CH29						Include or exclude channel 29
			Excluded	0				Exclude
			Included	1				Include
e	RW	CH30						Include or exclude channel 30
			Excluded	0				Exclude
			Included	1				Include
f	RW	CH31						Include or exclude channel 31
			Excluded	0				Exclude
			Included	1				Include

22.2.50 FORK[0].TEP

Address offset: 0x910 Channel 0 task end-point



Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	А А
Res	et 0x0	0000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (
Id	Reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0												scri	ptic	on																			
Α	RW	TEP		I Value Description Pointer to task register																														

22.2.51 FORK[1].TEP

Address offset: 0x914 Channel 1 task end-point

Bit	numl	ber					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	ı
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	l				
Re	et 0x	(00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	l		
Id	RW	V I	Field		Va	lue							De	scri	ptic	on																				l		
Α	Id RW Field Value Id Value A RW TEP													Poi	nte	r to	tas	sk re	egis	ter																	١	

22.2.52 FORK[2].TEP

Address offset: 0x918 Channel 2 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21	20 :	19	18	17	16	15 :	14	13	12 :	11 :	.0	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ.	Α	Α	Α	Α	Α	Α	Α .	Δ,	A A	1
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 ()
Id	Reset 0x00000000											De	crip	otic	n																				
Α	Id RW Field Value Id Value A RW TEP													r to	tas	k re	egis	ter																	7

22.2.53 FORK[3].TEP

Address offset: 0x91C Channel 3 task end-point

Bit nun	mber		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	.0	9	8	7	6	5	4	3	2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ.	Α	Α	Α	Α	Α	Α	Α .	Δ,	Α	Α
Reset (0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
ld R	RW Field	Value Id	Va	lue							De	scri	ptic	on																				
A R	RW TEP								Ро	nte	r to	tas	sk re	egis	ter																			

22.2.54 FORK[4].TEP

Address offset: 0x920 Channel 4 task end-point

Bit nu	mbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	0 9	9 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	A A	. A	Α	Α	Α	Α	Α	АА
Reset	0x0	0000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0	
ld i	RW	Field	Va	alue							De	scri	ptic	on																			
A F	Id RW Field Value Id Value A RW TEP												nte	r to	tas	sk r	egis	ter															

22.2.55 FORK[5].TEP

Address offset: 0x924 Channel 5 task end-point

Bit number		31	30	29	28	27	26	25	24	23	22	21 :	20	19 :	18 :	17 1	16 1	15 1	L4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A .	A A	Δ ,	A A	A A	Α	Α	Α	Α	Α	Α	A A	A A	A A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0 (0	0 0
ld RW Field	Value Id	Va	lue							Des	cri	ptio	n																		

A RW TEP Pointer to task register



22.2.56 FORK[6].TEP

Address offset: 0x928 Channel 6 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 1	l6 1	5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A A	Δ ,	Δ <i>A</i>	. Δ	. A	Α	Α	Α	Α	Α	Α	Α	Α .	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id												De	scri	otic	n																		
Α	RW												nte	r to	tas	k re	gist	ter															

22.2.57 FORK[7].TEP

Address offset: 0x92C Channel 7 task end-point

E	Bit n	umb	er					31	30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
1	d							Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А	Ĺ
F	Reset 0x00000000									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
ı	Id RW Field Value Id															De	cri	ptic	n																				ı
1	١	RW	RW TEP Pointer to task register																					7															

22.2.58 FORK[8].TEP

Address offset: 0x930 Channel 8 task end-point

Bit	nu	mbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	АА
Re	set	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	-	RW	Field	Value Id	Va	lue							De	scr	iptio	on																			
Α		RW	TEP										Ρο	inte	er to	ta	sk r	egis	ter																

22.2.59 FORK[9].TEP

Address offset: 0x934 Channel 9 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.60 FORK[10].TEP

Address offset: 0x938 Channel 10 task end-point

Bit number		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	A	A A	A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 ()
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																				
Δ RW TEP										Pο	inte	r to	ta	sk n	egiq	ter																	

22.2.61 FORK[11].TEP

Address offset: 0x93C Channel 11 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$
Id RW Field Value Id	Value Description
A RW TEP	Pointer to task register

22.2.62 FORK[12].TEP

Address offset: 0x940

Channel 12 task end-point

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 1	6 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id		AAAAAA	A A A A A A A A	A A A A A A A	A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0000000	0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW TEP			Pointer to task register		

22.2.63 FORK[13].TEP

Address offset: 0x944

Channel 13 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.64 FORK[14].TEP

Address offset: 0x948

Channel 14 task end-point

Bit numl	ber		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ A	Α Α	. A	Α	Α	Α	Α	Α	А А
Reset 0x	k00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id RV	V Field	Value Id	Va	lue							De	scri	ptic	on																		
A RW	V TEP										Poi	nte	r to	tas	sk re	egis	ter															

22.2.65 FORK[15].TEP

Address offset: 0x94C

Channel 15 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.66 FORK[16].TEP

Address offset: 0x950

Channel 16 task end-point

Bit number	31 30 29 28	27 26 25 24 23 22 21 2	0 19 18 17 16 15 14 13	12 11 10 9 8 7 6	5 4 3 2 1 0
Id	A A A A	A A A A A A A	A A A A A A A	A A A A A A	A A A A A A
Reset 0x00000000	0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0
Id RW Field Value Id	Value	Description	n		

A RW TEP Pointer to task register



22.2.67 FORK[17].TEP

Address offset: 0x954

Channel 17 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16 1	5 1	4 1	3 12	2 1:	1 10	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	A A	A /	Α Α	. Α	Α	Α	Α	Α	Α	Α	Α	A A	۸ ۸	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	TEP										Poi	nte	r to	ta	sk r	egis	ter															

22.2.68 FORK[18].TEP

Address offset: 0x958

Channel 18 task end-point

E	Bit n	umb	er			31	30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
1	d					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А	Ĺ
F	Rese	t Ox	00000	000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
ı	d	RW	Fiel	i	Value Id	Va	lue							De	cri	ptic	n																				ı
1	١	RW	TEP											Poi	nte	r to	tas	k re	gis	ter																	7

22.2.69 FORK[19].TEP

Address offset: 0x95C

Channel 19 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 3	17 :	16 :	15 1	L4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α Α	A A	A A	Α	Α	Α	Α	Α	Α	A	Δ Α	4 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																		
Α	RW	TEP										Poi	nte	r to	tas	sk re	gis	ter															

22.2.70 FORK[20].TEP

Address offset: 0x960

Channel 20 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.71 FORK[21].TEP

Address offset: 0x964

Channel 21 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.72 FORK[22].TEP

Address offset: 0x968

Channel 22 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$
Id RW Field Value Id	Value Description
A RW TEP	Pointer to task register

22.2.73 FORK[23].TEP

Address offset: 0x96C

Channel 23 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																			
Α	RW	TEP										Ро	inte	er to	ta	sk r	egis	ter																

22.2.74 FORK[24].TEP

Address offset: 0x970

Channel 24 task end-point

Е	Bit n	umb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 1	16 :	15 :	14 1	13 :	12	11 1	0 9	9 ;	3 7	7	6 !	5	4 3	3 2	. 1	. 0
10	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	A	Α ,	Δ,	4 4	۱ ۱	Δ ,	Α.	A A	Α Α	ι A	A A
F	Rese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0 (0 () (0 (0	0 (0	0	0
b	d	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
A	١	RW	TEP										Poi	nte	r to	tas	sk re	gis	ter																

22.2.75 FORK[25].TEP

Address offset: 0x974

Channel 25 task end-point

Bit numl	ber		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ A	Α Α	. A	Α	Α	Α	Α	Α	А А
Reset 0x	k00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id RV	V Field	Value Id	Va	lue							De	scri	ptic	on																		
A RW	V TEP										Poi	nte	r to	tas	sk re	egis	ter															

22.2.76 FORK[26].TEP

Address offset: 0x978

Channel 26 task end-point

Bit nu	mbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	0 9	9 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	A A	. A	Α	Α	Α	Α	Α	АА
Reset	0x0	0000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0	
ld i	RW	Field	Va	alue							De	scri	ptic	on																			
A F	RW	TEP										Ро	nte	r to	tas	sk r	egis	ter															

22.2.77 FORK[27].TEP

Address offset: 0x97C

Channel 27 task end-point

Bit number		31	30	29	28	27	26	25	24	23	22	21 2	20 1	19 1	.8 1	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A	Δ ,	4 4	A 4	λ Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id RW Field	Value Id	Val	lue							Des	cri	otio	n																		

A RW TEP Pointer to task register



22.2.78 FORK[28].TEP

Address offset: 0x980

Channel 28 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 :	16 1	5 1	4 1	3 12	2 1:	1 10	9	8	7	6	5	4	3 2	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	A A	A /	Α Α	. Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	TEP										Poi	nte	r to	ta	sk r	egis	ter															

22.2.79 FORK[29].TEP

Address offset: 0x984

Channel 29 task end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 3	17 :	16 1	15 1	.4 1	13 1	.2 1	.1 1	0 9) 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	Α.	Α,	Δ.	Δ ,	A A		A	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 () () C	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	gis	ter															

22.2.80 FORK[30].TEP

Address offset: 0x988

Channel 30 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	18 1	17 1	16 1	.5 1	4 1	3 12	2 13	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	A	Δ,	Δ <i>A</i>	. Δ	. A	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	nter	to	tas	k re	gist	ter															

22.2.81 FORK[31].TEP

Address offset: 0x98C

Channel 31 task end-point

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18	8 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description	

A RW TEP Pointer to task register



23 RADIO — 2.4 GHz Radio

The RADIO contains a 2.4 GHz radio receiver and a 2.4 GHz radio transmitter that is compatible with Nordic's proprietary 1 Mbps and 2 Mbps radio modes in addition to 1 Mbps *Bluetooth*[®] low energy mode.

EasyDMA in combination with an automated packet assembler and packet disassembler, and an automated CRC generator and CRC checker, makes it very easy to configure and use the RADIO. See *Figure 28: RADIO block diagram* on page 201 for details.

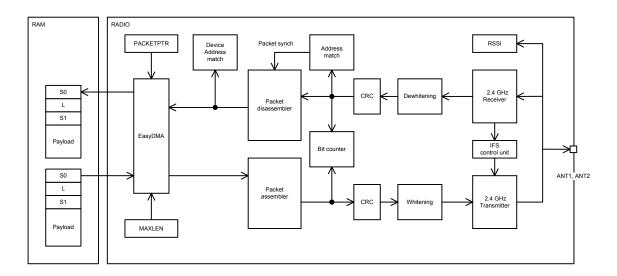


Figure 28: RADIO block diagram

The RADIO includes a Device Address Match unit and an interframe spacing control unit that can be utilized to simplify address white listing and interframe spacing respectively, in *Bluetooth* Smart and similar applications.

The RADIO also includes a Received Signal Strength Indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits have been sent or received by the RADIO.

23.1 EasyDMA

The RADIO use EasyDMA for reading and writing of data packets from and to the RAM without CPU involvement.

As illustrated in *Figure 1*, the RADIO's EasyDMA utilizes the same PACKETPTR for receiving and transmitting packets. The CPU should reconfigure this pointer every time before the RADIO is started via the START task.

The structure of a radio packet is described in detail in *Packet configuration* on page 202. The data that is stored in Data RAM and transported by EasyDMA consists of S0, LENGTH, S1, the payload itself, and a static add-on sent immediately after the payload.

The size of each of the above elements in the frame is configurable (see *Packet configuration* on page 202), and the space occupied in RAM depends on these settings. A size of zero is possible for any of the fields, it is up to the user to make sure that the resulting frame complies with the RF protocol chosen.

For the field sizes defined in bits, the occupation in RAM will always be rounded up to the next full byte size (for instance 3 bit length will allocate 1 byte in RAM, 9 bit length will allocate 2 bytes, etc.).

In addition, the S0INCL field in PCNF0 determines if S0 is present in RAM at all if its length is zero. If present, one byte is allocated in RAM.



The size of S0 is configured through the S0LEN field in PCNF0. The size of LENGTH is configured through the LFLEN field in PCNF0. The size of S1 is configured through the S1LEN field in PCNF0. The size of the payload is configured through the value in RAM corresponding to the LENGTH field. The size of the static add-on to the payload is configured through the STATLEN field in PCNF1.

The MAXLEN field in the PCNF1 register configures the maximum packet payload plus add-on size in number of bytes that can be transmitted or received by the RADIO. This feature can be used to ensure that the RADIO does not overwrite, or read beyond, the RAM assigned to the packet payload. This means that if the packet payload length defined by PCNF1.STATLEN and the LENGTH field in the packet specifies a packet larger than MAXLEN, the payload will be truncated at MAXLEN.

Note that MAXLEN includes the payload and the add-on, but excludes the size occupied by the S0, LENGTH and S1 fields. This has to be taken into account when allocating RAM.

If the payload plus add-on length is specified larger than MAXLEN, the RADIO will still transmit or receive in the same way as before except the payload is now truncated to MAXLEN. The packet's LENGTH field will not be altered when the payload is truncated. The RADIO will calculate CRC as if the packet length is equal to MAXLEN.

If the PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The DISABLED event indicates that the EasyDMA has finished accessing the RAM.

23.2 Packet configuration

A Radio packet contains the following fields: PREAMBLE, ADDRESS, S0, LENGTH, S1, PAYLOAD and CRC.

See *Figure 29: On-air packet layout* on page 202. Not shown in the figure is the static payload add-on (the length of which is defined in STATLEN, and which is 0 bytes long in a standard BLE packet), and would be sent between PAYLOAD and CRC. The Radio sends the different fields in the packet in the order they are illustrated below, from left to right. The preamble will be sent least significant bit first on-air.

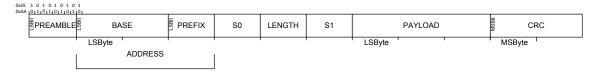


Figure 29: On-air packet layout

For all modes that can be specified in the MODE register, the PREAMBLE is one byte long. If the first bit of the ADDRESS is 0 the preamble will be set to 0xAA otherwise the PREAMBLE will be set to 0x55.

Radio packets are stored in memory inside instances of a radio packet data structure as illustrated in *Figure 30: In-RAM representation of radio packet, S0, LENGTH and S1 are optional* on page 202. The PREAMBLE, ADDRESS and CRC fields are omitted in this data structure.



Figure 30: In-RAM representation of radio packet, S0, LENGTH and S1 are optional

The byte ordering on air is always Least Significant Byte First for the ADDRESS and PAYLOAD fields and Most Significant Byte First for the CRC field. The ADDRESS fields are always transmitted and received least significant bit first on-air. The CRC field is always transmitted and received Most Significant Bit first. The bit-



endian, i.e. which order the bits are sent and received in, of the S0, LENGTH, S1 and PAYLOAD fields can be configured via the ENDIAN in PCNF1.

The S0INCL field in PCNF0 determines if S0 is present in RAM at all if its length is zero. If present, one byte is allocated in RAM.

The sizes of the S0, LENGTH and S1 fields can be individually configured via S0LEN, LFLEN and S1LEN in PCNF0 respectively. If any of these fields are configured to be less than 8 bit long the, the least significant bits of the fields, as seen from the RAM representation, are used.

If S0, LENGTH or S1 are specified with zero length their fields will be omitted in memory, otherwise each field will be represented as a separate byte, regardless of the number of bits in their on-air counterpart.

23.3 Maximum packet length

Independent of the configuration of MAXLEN, the combined length of S0, LENGTH, S1 and PAYLOAD cannot exceed 258 bytes.

23.4 Address configuration

The on-air radio ADDRESS field is composed of two parts, the base address field and the address prefix field.

The size of the base address field is configurable via BALEN in PCNF1. The base address is truncated from LSByte if the BALEN is less than 4. See *Table 34: Definition of logical addresses* on page 203.

The on-air addresses are defined in the BASEn and PREFIXn registers, and it is only when writing these registers the user will have to relate to actual on-air addresses. For other radio address registers such as the TXADDRESS, RXADDRESSES and RXMATCH registers, logical radio addresses ranging from 0 to 7 are being used. The relationship between the on-air radio addresses and the logical addresses is described in *Table 34: Definition of logical addresses* on page 203.

Table 34: Definition of logical addresses

Logical address	Base address	Prefix byte
0	BASE0	PREFIXO.APO
1	BASE1	PREFIXO.AP1
2	BASE1	PREFIXO.AP2
3	BASE1	PREFIXO.AP3
4	BASE1	PREFIX1.AP4
5	BASE1	PREFIX1.AP5
6	BASE1	PREFIX1.AP6
7	BASE1	PREFIX1.AP7

23.5 Data whitening

The RADIO is able to do packet whitening and de-whitening.

See WHITEEN in PCNF1 register for how to enable whitening. When enabled, whitening and de-whitening will be handled by the RADIO automatically as packets are sent and received.

The whitening word is generated using polynomial $g(D) = D^7 + D^4 + 1$, which then is XORed with the data packet that is to be whitened, or de-whitened. See the figure below.



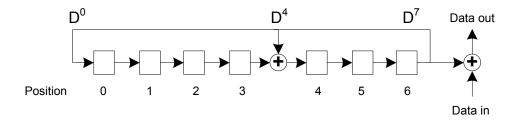


Figure 31: Data whitening and de-whitening

Whitening and de-whitening will be performed over the whole packet (except for the preamble and the address field).

The linear feedback shift register, illustrated in *Figure 31: Data whitening and de-whitening* on page 204 can be initialised via the DATAWHITEIV register.

23.6 CRC

The CRC generator in the RADIO calculates the CRC over the whole packet excluding the preamble. If desirable, the address field can be excluded from the CRC calculation as well

See CRCCNF register for more information.

The CRC polynomial is configurable as illustrated in *Figure 32: CRC generation of an n bit CRC* on page 204 where bit 0 in the CRCPOLY register corresponds to X^0 and bit 1 corresponds to X^1 etc. See CRCPOLY for more information.

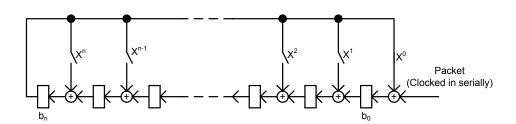


Figure 32: CRC generation of an n bit CRC

As illustrated in *Figure 32: CRC generation of an n bit CRC* on page 204, the CRC is calculated by feeding the packet serially through the CRC generator. Before the packet is clocked through the CRC generator, the CRC generator's latches b_0 through b_n will be initialized with a predefined value specified in the CRCINIT register. When the whole packet is clocked through the CRC generator, latches b_0 through b_n will hold the resulting CRC. This value will be used by the RADIO during both transmission and reception but it is not available to be read by the CPU at any time. A received CRC can however be read by the CPU via the RXCRC register independent of whether or not it has passed the CRC check.

The length (n) of the CRC is configurable, see CRCCNF for more information.

After the whole packet including the CRC has been received, the RADIO will generate a CRCOK event if no CRC errors were detected, or alternatively generate a CRCERROR event if CRC errors were detected.



The status of the CRC check can be read from the CRCSTATUS register after a packet has been received.

23.7 Radio states

The RADIO can enter a number of states.

The RADIO can enter the states described the table below. An overview state diagram for the RADIO is illustrated in *Figure 33: Radio states* on page 205. This figure shows how the tasks and events relate to the RADIO's operation. The RADIO does not prevent a task from being triggered from the wrong state. If a task is triggered from the wrong state, for example if the RXEN task is triggered from the RXDISABLE state, this may lead to incorrect behaviour. As illustrated in *Figure 33: Radio states* on page 205, the PAYLOAD event is always generated even if the payload is zero.

Table 35: RADIO state diagram

State	Description
DISABLED	No operations are going on inside the radio and the power consumption is at a minimum
RXRU	The radio is ramping up and preparing for reception
RXIDLE	The radio is ready for reception to start
RX	Reception has been started and the addresses enabled in the RXADDRESSES register are being monitored
TXRU	The radio is ramping up and preparing for transmission
TXIDLE	The radio is ready for transmission to start
TX	The radio is transmitting a packet
RXDISABLE	The radio is disabling the receiver
TXDISABLE	The radio is disabling the transmitter

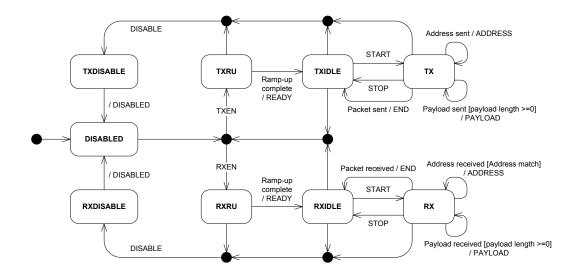


Figure 33: Radio states

23.8 Transmit sequence

Before the RADIO is able to transmit a packet, it must first ramp-up in TX mode.

See TXRU in *Figure 33: Radio states* on page 205 and *Figure 34: Transmit sequence* on page 206. A TXRU ramp-up sequence is initiated when the TXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet transmission can be initiate. A packet transmission is initiated by triggering the START task. As illustrated in *Figure 33: Radio states* on page 205 the START task can first be triggered after the RADIO has entered into the TXIDLE state.

Figure 34: Transmit sequence on page 206 illustrates a single packet transmission where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between READY and START, and between END and DISABLE. As illustrated in Figure 34: Transmit sequence on page 206



the RADIO will by default transmit '1's between READY and START, and between END and DISABLED. What is transmitted can be programmed through the DTX field in the MODECNF0 register.

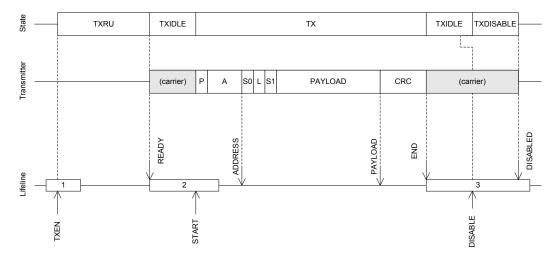


Figure 34: Transmit sequence

A slightly modified version of the transmit sequence from *Figure 34: Transmit sequence* on page 206 is illustrated in *Figure 35: Transmit sequence using shortcuts to avoid delays* on page 206 where the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

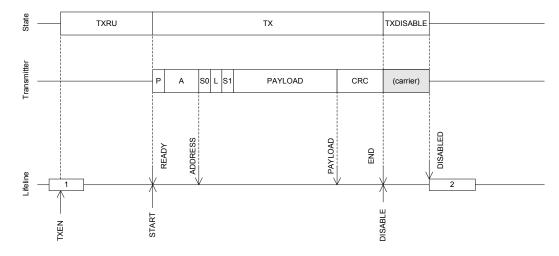


Figure 35: Transmit sequence using shortcuts to avoid delays

The RADIO is able to send multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated in *Figure 36: Transmission of multiple packets* on page 207.



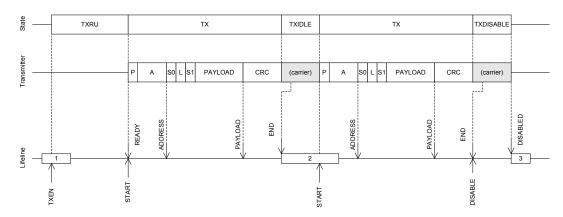


Figure 36: Transmission of multiple packets

23.9 Receive sequence

Before the RADIO is able to receive a packet, it must first ramp up in RX mode

See RXRU in *Figure 33: Radio states* on page 205 and *Figure 37: Receive sequence* on page 207. An RXRU ramp-up sequence is initiated when the RXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet reception can be initiated. A packet reception is initiated by triggering the START task. As illustrated in *Figure 33: Radio states* on page 205 the START task can, first be triggered after the RADIO has entered into the RXIDLE state.

Figure 37: Receive sequence on page 207 illustrates a single packet reception where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay, caused by CPU execution, is expected between READY and START, and between END and DISABLE. As illustrated Figure 37: Receive sequence on page 207 the RADIO will be listening and possibly receiving undefined data, illustrated with an 'X', from START and until a packet with valid preamble (P) is received.

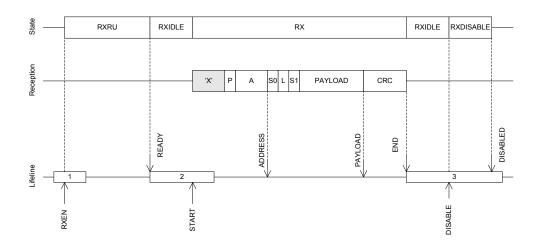


Figure 37: Receive sequence

A slightly modified version of the receive sequence from *Figure 37: Receive sequence* on page 207 is illustrated in *Figure 38: Receive sequence using shortcuts to avoid delays* on page 208 where the the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.



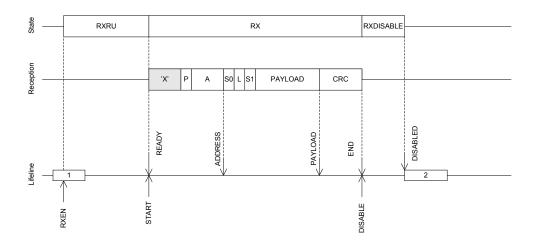


Figure 38: Receive sequence using shortcuts to avoid delays

The RADIO is able to receive multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated *Figure 39: Reception of multiple packets* on page 208.

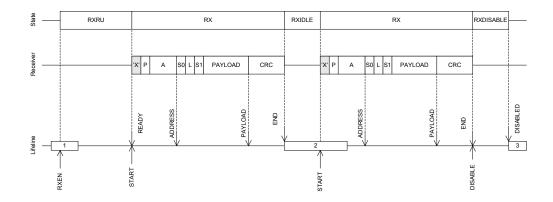


Figure 39: Reception of multiple packets

23.10 Received Signal Strength Indicator (RSSI)

The radio implements a mechanism for measuring the power in the received radio signal. This feature is called Received Signal Strength Indicator (RSSI).

Sampling of the received signal strength is started by using the RSSISTART task. The sample can be read from the RSSISAMPLE register.

The sample period of the RSSI is defined by RSSI_{PERIOD}, see the device product specification for details. The RSSI sample will hold the average received signal strength during this sample period.

For the RSSI sample to be valid the radio has to be enabled in receive mode (RXEN task) and the reception has to be started (READY event followed by START task).

23.11 Interframe spacing

Interframe spacing is the time interval between two consecutive packets.

It is defined as the time, in micro seconds, from the end of the last bit of the previous packet received and to the start of the first bit of the subsequent packet that is transmitted. The RADIO is able to enforce this



interval as specified in the TIFS register as long as TIFS is not specified to be shorter than the RADIO's turn-around time, i.e. the time needed to switch off the receiver, and switch back on the transmitter.

TIFS is only enforced if END_DISABLE and DISABLED_TXEN shortcuts are enabled. TIFS is only qualified for use in BLE_1MBIT mode, and default ramp-up mode.

23.12 Device address match

The device address match feature is tailored for address white listing in a Bluetooth Smart and similar implementations.

This feature enables on-the-fly device address matching while receiving a packet on air. This feature only works in receive mode and as long as RADIO is configured for little endian, see PCNF1.ENDIAN.

The Device Address match unit assumes that the 48 first bits of the payload is the device address and that bit number 6 in S0 is the TxAdd bit. See the Bluetooth Core Specification for more information about device addresses, TxAdd and whitelisting.

The RADIO is able to listen for eight different device addresses at the same time. These addresses are specified in a DAB/DAP register pair, one pair per address, in addition to a TxAdd bit configured in the DACNF register. The DAB register specifies the 32 least significant bits of the device address, while the DAP register specifies the 16 most significant bits of the device address.

Each of the device addresses can be individually included or excluded from the matching mechanism. This is configured in the DACNF register.

23.13 Bit counter

The RADIO implements a simple counter that can be configured to generate an event after a specific number of bits have been transmitted or received.

By using shortcuts, this counter can be started from different events generated by the RADIO and hence count relative to these.

The bit counter is started by triggering the BCSTART task, and stopped by triggering the BCSTOP task. A BCMATCH event will be generated when the bit counter has counted the number of bits specified in the BCC register. The bit counter will continue to count bits until the DISABLED event is generated or until the BCSTOP task is triggered. The CPU can therefore, after a BCMATCH event, reconfigure the BCC value for new BCMATCH events within the same packet.

The bit counter can only be started after the RADIO has received the ADDRESS event.

The bit counter will stop and reset on BCSTOP, STOP, END and DISABLE tasks.

The figure below illustrates how the bit counter can be used to generate a BCMATCH event in the beginning of the packet payload, and again generate a second BCMATCH event after sending 2 bytes (16 bits) of the payload.



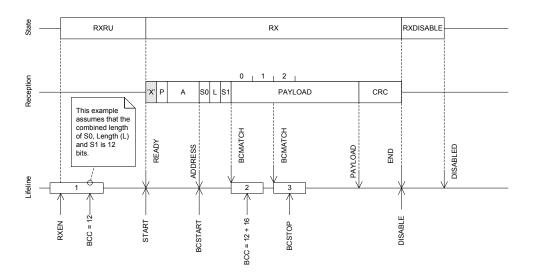


Figure 40: Bit counter example

23.14 Registers

Table 36: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40001000	RADIO	RADIO	2.4 GHz radio	

Table 37: Register Overview

Register	Offset	Description
TASKS_TXEN	0x000	Enable RADIO in TX mode
TASKS RXEN	0x004	Enable RADIO in RX mode
TASKS_START	0x008	Start RADIO
TASKS_STOP	0x00C	Stop RADIO
TASKS_DISABLE	0x010	Disable RADIO
TASKS_RSSISTART	0x014	Start the RSSI and take one single sample of the receive signal strength.
TASKS_RSSISTOP	0x018	Stop the RSSI measurement
TASKS_BCSTART	0x01C	Start the bit counter
TASKS_BCSTOP	0x020	Stop the bit counter
EVENTS_READY	0x100	RADIO has ramped up and is ready to be started
EVENTS_ADDRESS	0x104	Address sent or received
EVENTS_PAYLOAD	0x108	Packet payload sent or received
EVENTS_END	0x10C	Packet sent or received
EVENTS_DISABLED	0x110	RADIO has been disabled
EVENTS_DEVMATCH	0x114	A device address match occurred on the last received packet
EVENTS_DEVMISS	0x118	No device address match occurred on the last received packet
EVENTS_RSSIEND	0x11C	Sampling of receive signal strength complete.
EVENTS_BCMATCH	0x128	Bit counter reached bit count value.
EVENTS_CRCOK	0x130	Packet received with CRC ok
EVENTS_CRCERROR	0x134	Packet received with CRC error
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CRCSTATUS	0x400	CRC status
RXMATCH	0x408	Received address
RXCRC	0x40C	CRC field of previously received packet



Register	Offset	Description	
DAI	0x410	Device address match index	
PACKETPTR	0x504	Packet pointer	
FREQUENCY	0x508	Frequency	
TXPOWER	0x50C	Output power	
MODE	0x510	Data rate and modulation	
PCNF0	0x514	Packet configuration register 0	
PCNF1	0x518	Packet configuration register 1	
BASE0	0x51C	Base address 0	
BASE1	0x520	Base address 1	
PREFIXO	0x524	Prefixes bytes for logical addresses 0-3	
PREFIX1	0x528	Prefixes bytes for logical addresses 4-7	
TXADDRESS	0x52C	Transmit address select	
RXADDRESSES	0x530	Receive address select	
CRCCNF	0x534	CRC configuration	
CRCPOLY	0x538	CRC polynomial	
CRCINIT	0x53C	CRC initial value	
	0x540	Re	eserved
TIFS	0x544	Inter Frame Spacing in us	
RSSISAMPLE	0x548	RSSI sample	
STATE	0x550	Current radio state	
DATAWHITEIV	0x554	Data whitening initial value	
BCC	0x560	Bit counter compare	
DAB[0]	0x600	Device address base segment 0	
DAB[1]	0x604	Device address base segment 1	
DAB[2]	0x608	Device address base segment 2	
DAB[3]	0x60C	Device address base segment 3	
DAB[4]	0x610	Device address base segment 4	
DAB[5]	0x614	Device address base segment 5	
DAB[6]	0x618	Device address base segment 6	
DAB[7]	0x61C	Device address base segment 7	
DAP[0]	0x620	Device address prefix 0	
DAP[1]	0x624	Device address prefix 1	
DAP[2]	0x628	Device address prefix 2	
DAP[3]	0x62C	Device address prefix 3	
DAP[4]	0x630	Device address prefix 4	
DAP[5]	0x634	Device address prefix 5	
DAP[6]	0x638	Device address prefix 6	
DAP[7]	0x63C	Device address prefix 7	
DACNF	0x640	Device address match configuration	
MODECNF0	0x650	Radio mode configuration register 0	
POWER	0xFFC	Peripheral power control	

23.14.1 SHORTS

Address offset: 0x200

Shortcut register

Bitı	numbe	er		31	. 30	29	28	27	26 2	25 2	24 2	3 2	2 2:	1 20	19	18	17	16 1	5 1	4 1	3 12	11	10	9	8 7	6	5	4	3	2	1 0
Id																									Н	G	F	Ε	D	C I	В А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						0	esc	ript	ion																	
Α	RW	READY_START									S	hor	tcut	be	twe	en F	REAL)Y e	ven	t an	id ST	ART	tas	k							
											S	ee L	EVE	NTS	_RE	ΑD۱	a n	d <i>TA</i>	SKS	_57	ART										
			Disabled	0								Disal	ble s	shor	rtcut	t															
			Enabled	1							Е	nab	ole s	hor	tcut																
В	RW	END_DISABLE									S	hor	tcut	be	twe	en E	ND	eve	nt a	ınd	DISA	BLE	tasl	<							
											S	ee L	EVE	NTS	_EN	D a	nd 7	ASK	(S_E	OISA	BLE										



Bitı	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				H GFEDCBA
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
С	RW DISABLED_TXEN			Shortcut between DISABLED event and TXEN task
				See EVENTS_DISABLED and TASKS_TXEN
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
D	RW DISABLED_RXEN			Shortcut between DISABLED event and RXEN task
				See EVENTS_DISABLED and TASKS_RXEN
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
E	RW ADDRESS_RSSISTART			Shortcut between ADDRESS event and RSSISTART task
				See EVENTS_ADDRESS and TASKS_RSSISTART
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
F	RW END_START			Shortcut between END event and START task
				See EVENTS_END and TASKS_START
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
G	RW ADDRESS_BCSTART			Shortcut between ADDRESS event and BCSTART task
	_			Son EVENTS ADDRESS and TASKS DOSTART
		Disabled	0	See EVENTS_ADDRESS and TASKS_BCSTART Disable shortcut
		Enabled	1	Enable shortcut
Н	RW DISABLED RSSISTOP	Litablea	•	Shortcut between DISABLED event and RSSISTOP task
		5. 11.1		See EVENTS_DISABLED and TASKS_RSSISTOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut

23.14.2 INTENSET

Address offset: 0x304

Enable interrupt

	31 30 29 28 27 26 25 24	‡ 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
		LK I HGFEDCBA
	0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Value Id	Value	Description
		Write '1' to Enable interrupt for READY event
		See EVENTS_READY
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
		Write '1' to Enable interrupt for ADDRESS event
		See EVENTS_ADDRESS
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
		Write '1' to Enable interrupt for PAYLOAD event
		See EVENTS_PAYLOAD
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
	Set Disabled Enabled Set Disabled Enabled Set Disabled	Set 1 Disabled 0 Enabled 1 Set 1 Disabled 0 Enabled 1 Set 1 Disabled 0 Enabled 0 Enabl



Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				LK I HGFEDCBA
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Ε	RW DISABLED			Write '1' to Enable interrupt for DISABLED event
				See EVENTS_DISABLED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW DEVMATCH			Write '1' to Enable interrupt for DEVMATCH event
				See EVENTS_DEVMATCH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW DEVMISS			Write '1' to Enable interrupt for DEVMISS event
				See EVENTS_DEVMISS
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW RSSIEND			Write '1' to Enable interrupt for RSSIEND event
				See EVENTS_RSSIEND
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
1	RW BCMATCH			Write '1' to Enable interrupt for BCMATCH event
				See EVENTS_BCMATCH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
K	RW CRCOK			Write '1' to Enable interrupt for CRCOK event
				See EVENTS_CRCOK
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW CRCERROR			Write '1' to Enable interrupt for CRCERROR event
				See EVENTS_CRCERROR
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

23.14.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22 2	1 2	0 1	9 1	8 1	7 16	5 15	14	13	12	11 10	9	8	7	6	5	4	3	2	1 (C
Id																					L	K	- 1			Н	G	F	Ε	D	С	В	Δ
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (D
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	READY										Wri	te '1	' to	Dis	sab	le ir	iteri	rupt	for	· RE/	٩DY	even	t									_
												See	EVE	NT	S_R	EAL	DΥ																
			Clear	1								Disa	ble																				



Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					LK I HGFEDCBA
Res	et OxC	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ADDRESS			Write '1' to Disable interrupt for ADDRESS event
					See EVENTS_ADDRESS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	PAYLOAD			Write '1' to Disable interrupt for PAYLOAD event
					See EVENTS_PAYLOAD
			Clear	1	Disable
			Disabled	0	Read: Disabled
_		5110	Enabled	1	Read: Enabled
D	RW	END			Write '1' to Disable interrupt for END event
					See EVENTS_END
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	DISABLED			Write '1' to Disable interrupt for DISABLED event
					See EVENTS_DISABLED
			Clear	1	Disable
			Disabled	0	Read: Disabled
-	DIM	DEMAATCH	Enabled	1	Read: Enabled
F	KW	DEVMATCH			Write '1' to Disable interrupt for DEVMATCH event
					See EVENTS_DEVMATCH
			Clear	1	Disable
			Disabled	0	Read: Disabled
G	D\A/	DEVMISS	Enabled	1	Read: Enabled Write '1' to Disable interrupt for DEVMISS event
U	IVV	DEVIVIISS			
					See EVENTS_DEVMISS
			Clear	1	Disable
			Disabled Enabled	0	Read: Disabled Read: Enabled
Н	RW	RSSIEND	Eliableu	1	Write '1' to Disable interrupt for RSSIEND event
	11.00	NOSIEND			
					See EVENTS_RSSIEND
			Clear Disabled	0	Disable Read: Disabled
			Enabled	1	Read: Enabled
1	RW	BCMATCH	2abica	-	Write '1' to Disable interrupt for BCMATCH event
			Clear	1	See EVENTS_BCMATCH Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	CRCOK			Write '1' to Disable interrupt for CRCOK event
			Clear	1	See EVENTS_CRCOK Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
L	RW	CRCERROR			Write '1' to Disable interrupt for CRCERROR event
			Clear	1	See EVENTS_CRCERROR Disable
			Disabled	0	Read: Disabled



iu i	NW Fielu	Enabled	value	Read: Enabled
14 1	RW Field	Value Id	Value	Description
Reset	0x000000	0	0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id				LK I HGFEDCBA
Bit nu	mber		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

23.14.4 CRCSTATUS

Address offset: 0x400

CRC status

Bit	numbe	er		31 30	29	28	27	26	25 2	24 2	23 2	2 2	1 20	19	18	17	16	15	14 1	3 12	2 11	10	9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value	•						Des	crip	tion																		
Α	R	CRCSTATUS								(CRC	sta	tus	of p	acke	et re	cei	ved													
			CRCError	0						F	Pack	ket r	rece	ived	l wit	th C	RC 6	erro	r												
			CRCOk	1						F	Pack	et r	rece	ived	l wit	th C	RC (ok													

23.14.5 RXMATCH

Address offset: 0x408 Received address

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 :	L2 1	11 1	0 9	8	7	6	5	4	3	2	1 0	l
Id																																Α	A A	ı
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			l
Α	R	RXMATCH										Red	ceiv	ed	add	lres	s																	١

Logical address of which previous packet was received

23.14.6 RXCRC

Address offset: 0x40C

CRC field of previously received packet

Bit r	iumbe	er		31	1 30	29	28	3 27	7 26	5 2	5 2	4 2	3 2	22 2	21 :	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id												ļ	۱ ۸	Α ,	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	ΑА
Res	et OxC	0000000		0	0	0	0	0	0	C	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							D	es	crip	tio	n																			
												_	DC	f: al	1-1-	. e			ماء			- 1													
Α	R	RXCRC										C	ĸĊ	ne	ıa c	υгр	rev	lou	Siy	rec	eiv	ea	oac	ket											

23.14.7 DAI

Address offset: 0x410

Device address match index

Bit number 3	31 30 29 28 27 26 25 24 23 22 21	20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A
Reset 0x00000000 0	0 0 0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value Id V	Value Description	on
A R DAI	Device ad	dress match index

Index (n) of device address, see $\mathsf{DAB}[n]$ and $\mathsf{DAP}[n]$, that got an address match.

23.14.8 PACKETPTR

Address offset: 0x504



Packet pointer

В	it nu	mbe	er		31	30	29	28	3 27	26	25	24	23	22 :	21 2	20 :	19 1	L8 1	17 1	6 1	l5 1	4 13	3 12	11	10	9	8	7	6 !	5 4	4 3	2	1	0
lo	ł				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A A	Δ,	A A	A A	Α	Α	Α	Α	Α ,	Δ.	A A	4 4	4 A	Α	Α	Α
R	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0 (0	0 (0 (0 0	0	0	0
Ic	i	RW	Field	Value Id	Va	lue							Des	crip	ptio	n																		
Α		RW	PACKETPTR										Pac	ket	poi	nte	er																	
													rec	epti	ion.	Wł	hen	tra	nsm	nitti	ing,	the	pac	ket	poir	ited	on c	by 1						
													ado	lres	s w	ill b	e tr	ans	mit	ted	lan	lw b	ien	rece	eivin	g, t	he r	ece	eive	d				
													pac	ket	wil	be	wr	itte	n to	th	is a	ddre	ss.	Γhis	ado	lres	s is	a b	yte					
													alig	nec	d rai	n a	ddr	ess																

23.14.9 FREQUENCY

Address offset: 0x508

Frequency

Bit r	numbe	er		33	1 30	29	28 2	27 2	26 2	5 2	24 2	3 22	21	20	19 1	8 1	7 16	5 15	14	13 1	12 13	l 10	9	8	7	5 5	5 4	3	2	1 0
Id																								В		4 4	A A	Α	Α	A A
Res	et 0x0	0000002		0	0	0	0	0	0 () (0 (0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0 (0	0	0	1 0
Id	RW	Field	Value Id	V	alue						D	escr	iptic	on																
Α	RW	FREQUENCY		[0)10	0]					R	adio	cha	nne	el fre	que	ncy													
											F	requ	ienc	y = 1	2400) + F	REC	UEI	NCY	(MI	Ηz).									
В	RW	MAP									С	han	nel n	nap	sele	ctic	n.													
			Default	0							С	hanı	nel n	nap	bet	wee	n 24	100	MH.	Z 2	2500	МН	Z							
											F	requ	ienc	y = 1	2400) + F	REC	UEI	NCY	(MI	łz)									
			Low	1							С	han	nel n	nap	bet	wee	n 2	360	MH.	Z 2	2460	МН	Z							
											F	requ	ienc	y = :	2360) + F	REC	UEI	NCY	(MI	łz)									

23.14.10 TXPOWER

Address offset: 0x50C

Output power

		•			
Bit r	numbe	er		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A A A A A A A A A A A A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	TXPOWER			RADIO output power.
					Output power in number of dBm, i.e. if the value -20 is specified
					the output power will be set to -20dBm.
			Pos4dBm	0x04	+4 dBm
			Pos3dBm	0x03	+3 dBm
			0dBm	0x00	0 dBm
			Neg4dBm	0xFC	-4 dBm
			Neg8dBm	0xF8	-8 dBm
			Neg12dBm	0xF4	-12 dBm
			Neg16dBm	0xF0	-16 dBm
			Neg20dBm	0xEC	-20 dBm
			Neg30dBm	0xD8	-40 dBm Deprecated
			Neg40dBm	0xD8	-40 dBm
			Neg40dBm	0xD8	-40 dBm

23.14.11 MODE

Address offset: 0x510

Data rate and modulation



Bit	numbe	er		31	1 30	29	28	8 27	7 26	5 25	5 24	1 23	22	21	20	19	18	17	16	15	14	13	12	11 :	10 9	9 .	8 7	6	5	4	3	2	1 0
Id																															Α	Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	escr	iptio	on																		
Α	RW	MODE		value									dio	dat	a ra	ate	and	d mo	odu	lati	on	set	ing	Th	e ra	dio	sup	por	ts				
							Fr	equ	enc	y-sł	nift	Ke	ying	(F	SK)	mo	dul	atio	n.														
			Nrf_1Mbit	0								1	Mbi	t/s I	Nor	dic	pro	pri	eta	ry r	adi	o m	ode										
			Nrf_2Mbit										Mbi	t/s I	Nor	dic	pro	pri	eta	ry r	adi	o m	ode										
			Nrf_250Kbit	1 2								25	0 kl	bit/s	s No	ordi	ic p	rop	riet	ary	rac	lio	mod	le							Dep	rec	ated
			Ble_1Mbit	1								1	Mbi	t/s l	Blue	eto	oth	Lov	v E	ner	gy												

23.14.12 PCNF0

Address offset: 0x514

Packet configuration register 0

Bit number		31	30 29	9 28	8 27	26	25	24 2	23 22	21	20	19 1	.8 1	7 16	15	14 1	3 12	11	10 9	9 8	7	6	5	4 3	3 2	1 0
Id								Н			F	Ε	E E	Ε						C				ļ	A A	А А
Reset 0x00000000		0	0 0	0	0	0	0	0	0 0	0	0	0	0 0	0	0	0 (0	0	0 (0	0	0	0	0 (0	0 0
Id RW Field V	alue Id	Val	ue						Desci	iptio	on															
A RW LFLEN								l	.engt	h or	air	of L	ENG	ТН	field	in n	umb	er of	f bits	i.						
C RW SOLEN								l	.engt	h or	air	of S	0 fie	ld i	n nu	mbe	r of l	yte	5.							
E RW S1LEN								l	.engt	h or	air	of S	1 fie	ld i	n nu	mbe	r of l	oits.								
F RW S1INCL								I	nclu	de oi	exc	lud	e S1	fiel	d in	RAM										
A	utomatic	0						I	nclu	de S1	l fie	ld ir	RAI	M o	nly i	f S1L	EN >	0								
Ir	nclude	1						A	Alwa	/s in	clud	e S	l fiel	d in	RAN	∕l inc	lepe	nder	nt of	S1L	EN					
H RW PLEN								l	.engt	h of	pre	aml	ole o	n ai	r. De	ecisio	n pc	int:	TASI	<s_:< th=""><th>STAF</th><th>RT ta</th><th>isk</th><th></th><td></td><td></td></s_:<>	STAF	RT ta	isk			
8	bit	0						8	3-bit	prea	mbl	e														
1	6bit	1						1	L6-bi	t pre	aml	ole														

23.14.13 PCNF1

Address offset: 0x518

Packet configuration register 1

Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E	D
Reset 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
ld RW Field	Value Id	Value	Description
A RW MAXLEN		[0255]	Maximum length of packet payload. If the packet payload is
			larger than MAXLEN, the radio will truncate the payload to
			MAXLEN.
B RW STATLEN		[0255]	Static length in number of bytes
			The static length parameter is added to the total length of the
			payload when sending and receiving packets, e.g. if the static
			length is set to N the radio will receive or send N bytes more
			than what is defined in the LENGTH field of the packet.
C RW BALEN		[24]	Base address length in number of bytes
0 1111 5/12211		[=]	,
			The address field is composed of the base address and the one
			byte long address prefix, e.g. set BALEN=2 to get a total address
			of 3 bytes.
D RW ENDIAN			On air endianness of packet, this applies to the SO, LENGTH, S1
			and the PAYLOAD fields.
	Little	0	Least Significant bit on air first
	Big	1	Most significant bit on air first
E RW WHITEEN			Enable or disable packet whitening
	Disabled	0	Disable
	Enabled	1	Enable



23.14.14 BASE0

Address offset: 0x51C

Base address 0

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW BASEO		Base address 0

Radio base address 0.

23.14.15 BASE1

Address offset: 0x520

Base address 1

Bit n	umbe	r		31	30	29 2	28 2	7 2	6 2	5 2	4 23	22	21	20	19	18 1	l7 1	6 15	5 14	13	12	11	10	9	8	7	6	5 -	4 3	2	1	0
Id				0 0 0 0 0 0 0								Α	Α	Α	Α	A	A A	4 A	A	Α	Α	Α	Α	Α	Α	Α	Α	A .	4 А	A	Α	Α
Rese	t 0x0	0000000										0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Val																												
Α	RW	BASE1													1																	

Radio base address 1.

23.14.16 PREFIX0

Address offset: 0x524

Prefixes bytes for logical addresses 0-3

Bit	numbe	er		31	. 30	29	28	3 27	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12 1	11 1	LO	9	8	7	6	5	4	3	2 1	0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	В	В	В	В	В	В	Α,	Α	Α	Α	A	4 Α	A A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id																															
Α	RW	AP0		Value Description																														
В	RW	AP1										Ad	dres	s p	refi	x 1.																		
С	RW	AP2										Ad	dres	s p	refi	x 2.																		
D	RW	AP3										Ad	dres	s p	refi	x 3.																		

23.14.17 PREFIX1

Address offset: 0x528

Prefixes bytes for logical addresses 4-7

Bit	numbe	er		31	. 30	29	28	3 27	7 26	25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 (
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	В	В	В	В	В	В	Α	Α	Α	Α	A	Δ ,	4 Δ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																														
Α	RW	AP4																																
В	RW	AP5										Ad	dre	ss p	ref	ix 5																		
С	RW	AP6										Ad	dre	ss p	ref	ix 6																		
D	R\M	AP7										hΑ	dre	ss n	ref	iv 7																		

23.14.18 TXADDRESS

Address offset: 0x52C

Transmit address select



Bit	num	nbei			31 30	29	28 2	7 26	25	24	23 2	22 2	21 2	0 19	9 18	17	16	15	14	13 :	12 1	11 10	9	8	7	6	5	4	3	2 1	L 0
Id																													,	4 Α	A A
Re	set 0)x00	000000		0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 Value Description									0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0) 0	
Id	R۱	w	Field	Value Id	Value Descript								tior	1																	
Α	R۱	W	TXADDRESS								Trar	ารm	it ac	ddre	ess s	ele	ct														

Logical address to be used when transmitting a packet.

23.14.19 RXADDRESSES

Address offset: 0x530 Receive address select

D.1.					
	numbe	er		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					H G F E D C B A
Res		0000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	ADDR0			Enable or disable reception on logical address 0.
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	ADDR1			Enable or disable reception on logical address 1.
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	ADDR2			Enable or disable reception on logical address 2.
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	ADDR3			Enable or disable reception on logical address 3.
			Disabled	0	Disable
			Enabled	1	Enable
Ε	RW	ADDR4			Enable or disable reception on logical address 4.
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	ADDR5			Enable or disable reception on logical address 5.
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	ADDR6			Enable or disable reception on logical address 6.
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	ADDR7			Enable or disable reception on logical address 7.
			Disabled	0	Disable
			Enabled	1	Enable

23.14.20 CRCCNF

Address offset: 0x534 CRC configuration

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW LEN		[13]	CRC length in number of bytes.
	Disabled	0	CRC length is zero and CRC calculation is disabled
	One	1	CRC length is one byte and CRC calculation is enabled
	Two	2	CRC length is two bytes and CRC calculation is enabled
	Three	3	CRC length is three bytes and CRC calculation is enabled
B RW SKIPADDR			Include or exclude packet address field out of CRC calculation.
	Include	0	CRC calculation includes address field
	Skip	1	CRC calculation does not include address field. The CRC
			calculation will start at the first byte after the address.



23.14.21 CRCPOLY

Address offset: 0x538

CRC polynomial

Bitı	numb	er		31	. 30	29	28 2	27 2	6 2	5 24	23	22 2	1 20	0 19	18	17	16	15 1	.4 13	12	11 1	.0 9	8	7	6	5	4	3	2	1 0
Id											Α	A	ДД	A	Α	Α	Α	Α ,	А А	Α	Α.	4 4	Α Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x(0000000		0	0	0	0	0 (0	0	0	0 (0 0	0	0	0	0	0 (0 0	0	0	0 (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Des	crip	tion	ı																
Α	RW	CRCPOLY								1 / 11																				
									CRC polynomial Each term in the CRC polynomial is mapped to a bit in this register which index corresponds to the term's exponent. The																					
											leas	st sig	gnifi	cant	ter	m/b	it is	har	d-wi	red	inte	nal	ly to	1, 8	and	bit				
									least significant term/bit is hard-wired internally to 1, and bit number 0 of the register content is ignored by the hardware.																					
											The	foll	owi	ng ex	kam	ple	is f	or a	n 8 b	it CR	C po	lyn	omi	al: >	(8 +	x7	+			
											х3 н	+ x2	+ 1 :	= 1 1	.000	110)1.													

23.14.22 CRCINIT

Address offset: 0x53C

CRC initial value

Bit	numbe	er		33	1 30	29	28	27	26	5 25	24	1 23	2:	2 21	. 20) 19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (,
Id												Α	Δ	A	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Ĺ
Res	et 0x0	0000000		0 0 0 0 Value Id Value								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (,
Id	RW	Field	Value Id	0 0 0 0 Value Id Value								De	esc	ripti	on																				l
Α	RW	CRCINIT		Value Id Value								CF	RC i	niti	al v	alue	5																		

Initial value for CRC calculation.

23.14.23 TIFS

Address offset: 0x544

Inter Frame Spacing in us

Bit r	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8 7	7	6	5 4	4 3	3 2	1	1 0	
Id																											A	۱ ۱	A ,	Δ ,	Δ ,	Δ Δ		A A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0 (0 (0	C	0 0	
Id	RW	Field	Value Id	Va	lue							De	scri	iptio	on																				
Α	RW	TIFS										Int	er F	Fran	ne:	Spa	cin	g in	us																
																											o co				!				
												end	d of	f the	e la	st k	oit o	of tl	he p	ore	viou	ıs p	ack	et t	o th	e st	art o	of t	he	first	t				
												bit	of	the	sul	bse	que	ent	pac	ket															

23.14.24 RSSISAMPLE

Address offset: 0x548

RSSI sample

Bit r	numbe	er		31 3	0 29	28	27	26 2	25 24	4 2	3 22	2 21	1 20	19	18	17	16	15 3	14 1	.3 12	2 11	10	9	8	7	6	5 4	1 3	2	1	0
Id																										Α.	A A	A A	Α	Α	Α
Res	et OxO	0000000		0	0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Valu	ie					D	esc	ript	ion																		
Α	R	RSSISAMPLE		[01	27]					R	SSI	sam	ple																		
																				nis re	Ŭ							е			
										Vä	alue	e. Ac	ctua	ıl re	ceiv	ed:	sign	al s	trer	igth	is th	ere	ore	as	foll	ows	5:				
										re	ecei	ved	sig	nal s	stre	ngt	h =	-A d	Bm												



23.14.25 STATE

Address offset: 0x550 Current radio state

Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A R STATE			Current radio state
	Disabled	0	RADIO is in the Disabled state
	RxRu	1	RADIO is in the RXRU state
	RxIdle	2	RADIO is in the RXIDLE state
	Rx	3	RADIO is in the RX state
	RxDisable	4	RADIO is in the RXDISABLED state
	TxRu	9	RADIO is in the TXRU state
	TxIdle	10	RADIO is in the TXIDLE state
	Tx	11	RADIO is in the TX state
	TxDisable	12	RADIO is in the TXDISABLED state

23.14.26 DATAWHITEIV

Address offset: 0x554

Data whitening initial value

Bit r	numbe	r		31	1 30	29	28	3 27	26	25	24	23	22	2 2:	1 20	0 1	9 1	8 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000040		0	0	0	0	0	0	0	0	0	0	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							De	SCI	ript	tion	ı																				
Α	RW	DATAWHITEIV										Da	ita	wh	iter	ning	g in	itia	al va	alu	e. E	Bit (5 is	haı	rd-v	vire	d t	o '1	', w	riti	ng	'0'				
												to	it ł	nas	no	eff	ect	, a	nd i	t w	/ill	alw	ays	be	re	ad I	oacl	c ar	ıd ı	isec	d b	У				
												the	e d	evi	ce a	as ':	1'.																			
												Bit	0	cor	res	por	nds	to	Ро	siti	on	6 c	f th	ne L	.SFF	Я, В	it 1	to I	os	itio	n 5	,				
												et	c.																							

23.14.27 BCC

Address offset: 0x560 Bit counter compare

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 :	19 :	18 1	.7 1	6 1	5 14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	4 Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	ВСС										Bit	cou	nte	r cc	omp	are																

Bit counter compare register

23.14.28 DAB[0]

Address offset: 0x600

Device address base segment 0

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW DAB	Device address base segment 0

Device address base segment 0



23.14.29 DAB[1]

Address offset: 0x604

Device address base segment 1

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α ,	A A	A A	A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	DAB										Dev	ice	ado	dres	s ba	ase	seg	mer	nt 1													

23.14.30 DAB[2]

Address offset: 0x608

Device address base segment 2

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	.9 1	8 1	7 1	6 1	.5 1	4 1	3 1:	2 13	. 10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α,	Δ ,	Δ .	Δ ,	A A	Δ /	A /	. Δ	A	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0 (0	0	0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	DAB										Dev	ice	ado	lres	s ba	se	seg	me	nt 2	2												

23.14.31 DAB[3]

Address offset: 0x60C

Device address base segment 3

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 :	19 1	L8 1	.7 1	.6 1	.5 1	4 1	.3 1	2 1	1 1) 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	Δ ,	Δ ,	Δ ,	Δ ,	Δ,	Δ.	4 Α	. Δ	. A	Α	Α	Α	Α	Α	A	А А
Re	et 0x(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	DAB										Dev	/ice	ado	dre	ss b	ase	seg	gme	nt 3	3												

23.14.32 DAB[4]

Address offset: 0x610

Device address base segment 4

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21 2	20 :	19 1	18 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																				ı
Α	RW	DAB										Dev	ice	ado	dre	ss b	ase	se	gm	ent	4														7

23.14.33 DAB[5]

Address offset: 0x614

Device address base segment 5

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description	

A RW DAB Device address base segment 5

23.14.34 DAB[6]

Address offset: 0x618

Device address base segment 6



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW DAB	Device address base segment 6

23.14.35 DAB[7]

Address offset: 0x61C

Device address base segment 7

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 :	16 1	L5 1	14 :	L3 1	.2 1	.1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α	Α.	Δ.	ДД	Α	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	DAB										Dev	vice	ad	dre	ss b	ase	se	gme	ent	7												

23.14.36 DAP[0]

Address offset: 0x620 Device address prefix 0

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12 :	11 :	LO	9	8	7	6	5	4	3	2 :	1 0	j
Id																				Α	Α	Α	Α	Α	A.	Α	Α	Α	Α	Α	Α	A	Δ,	ΑД	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	,
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																				ı
Α	RW	DAP										Dev	vice	ad	dre	ss p	ref	ix 0)																7

23.14.37 DAP[1]

Address offset: 0x624 Device address prefix 1

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12	2 11 10 9 8	7 6 5 4 3 2 1 0
Id				АААА		A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0	00000	0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW DAP			Device address prefix	x 1		

23.14.38 DAP[2]

Address offset: 0x628

Device address prefix 2

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12	11 10 9 8	7 6 5	4 3 2	1 0
Id				AAAA	A A A A	ААА	A A A	A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0	0 0 0	0 0
Id RW Field	Value Id	Value	Description					
A RW DAP			Device address prefix 2					

23.14.39 DAP[3]

Address offset: 0x62C

Device address prefix 3

Bit n	umbe	er		31	30 2	9	28 2	27 26	5 25	24	23	22 2	21 2	20 1	.9 1	8 1	7 16	15	14	13	12 :	l1 1	0 9	8	7	6	5	4	3	2	1 0	ı
Id																		Α	Α	Α	Α	A A	Α Δ	A	Α	Α	Α	Α	Α	A ,	А А	l
Rese	t 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	l
Id	RW	Field	Value Id	Va	lue						De	scrip	tio	n																		l
Α	RW	DAP										vice	ado	dres	s pi	efix	3															



23.14.40 DAP[4]

Address offset: 0x630

Device address prefix 4

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 :	16 15 14 13 12	2 11 10 9 8	7 6 5 4 3 2 1 0
Id				A A A A	. A A A A	A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW DAP			Device address prefix 4			

23.14.41 DAP[5]

Address offset: 0x634

Device address prefix 5

8	Bit nu	mbe	er				31	30 2	9 2	28 27	7 26	25	24	23 :	22 2	21 2	0 1	9 1	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
1	d																				Α	Α	Α	Α	Α	Α.	Δ.	Α.	Α	Α.	Α.	A	4 Δ	A	Α
ı	Reset	0x0	0000000				0	0	0	0 0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
ı	Reset 0x00000000 Id RW Field Value Id							lue						Des	crip	tio	n																		
7	A	RW	DAP											Dev	ice	add	res	s pr	efix	5															

23.14.42 DAP[6]

Address offset: 0x638

Device address prefix 6

Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9	9 8 7 6 5 4 3 2 1 0
Id				A A A A A A	A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW DAP			Device address prefix 6		

23.14.43 DAP[7]

Address offset: 0x63C Device address prefix 7

Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 1	10 9 8 7 6 5	5 4 3 2 1 0
Id				AAAAA	AAAAAA	A A A A A
Reset 0x0000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0	00000
Id RW Field	Value Id	Value	Description			
A RW DAP			Device address prefix 7	,		

23.14.44 DACNF

Address offset: 0x640

Device address match configuration

Bit	numbe	er		31	30 2	9 2	28 27	7 20	6 25	24	1 23	22	21 2	0 1	L9 1	8 17	16	15	14	13 :	L2 1	1 1	9	8	7	6	5	4	3	2 :	1 0
Id																		Р	О	N	M I	L K	J	-1	Н	G	F	Ε	D	C I	ВА
Res	et 0x0	0000000		0	0 (0	0 0	0	0	0	0	0	0 (0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Val	ıe						De	scri	ption	n																	
Α	RW	ENA0									En	able	ord	lisa	ble	devi	ce a	ddr	ess	ma	tchi	ng u	sing	dev	/ice	ad	dre	SS			
											0																				
			Disabled	0							Dis	sable	ed																		
			Enabled	1							En	able	ed																		
В	RW	ENA1									En	able	ord	lisa	ble	devi	ce a	ddr	ess	ma	tchi	ng u	sing	dev	vice	ad	dre	SS			
											1																				
			Disabled	0							Dis	sable	ed																		



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	PONMLKJIHGFEDCBA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
Enabled	1 Enabled
C RW ENA2	Enable or disable device address matching using device address
	2
Disabled	0 Disabled
Enabled	1 Enabled
D RW ENA3	Enable or disable device address matching using device address
	3
Disabled	0 Disabled
Enabled	1 Enabled
E RW ENA4	Enable or disable device address matching using device address
	4
Disabled	0 Disabled
Enabled	1 Enabled
F RW ENA5	Enable or disable device address matching using device address
	5
Disabled	0 Disabled
Enabled	1 Enabled
G RW ENA6	Enable or disable device address matching using device address
	6
Disabled	0 Disabled
Enabled	1 Enabled
H RW ENA7	Enable or disable device address matching using device address
	7
Disabled	0 Disabled
Enabled	1 Enabled
I RW TXADD0	TxAdd for device address 0
J RW TXADD1	TxAdd for device address 1
K RW TXADD2	TxAdd for device address 2
L RW TXADD3	TxAdd for device address 3
M RW TXADD4	TxAdd for device address 4
N RW TXADDS	TxAdd for device address 5
O RW TXADD6	TxAdd for device address 6
P RW TXADD7	TxAdd for device address 7

23.14.45 MODECNF0

Address offset: 0x650

Radio mode configuration register 0

Bit r	numbe	er		31	30 :	29 2	28 2	27 2	26 2	5 2	4 23	3 22	21	20	19 1	18 1	17 1	16 1	15 1	L4 1	3 12	2 11			8	7 (6 !	5 4	3	2	1	C
Id																								С	С							Д
Res	et 0x0	0000200		0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	1	0	0 (0 (0 0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	n																		
Α	RW	RU									Ra	adio	ram	p-u	ıp ti	me																
			Default	0							D	efau	ılt ra	mp	-up	tim	ie (t	RX	EN)	, cor	npa	tible	wit	h fi	rmv	vare	9					
											w	ritte	en fo	r nf	RF5:	1																
			Fast	1							Fa	ast ra	amp	-up	(tR	XEN	N,FA	(ST	, se	e el	ectr	ical	spe	ific	atio	n fo	or n	nore				
											in	forn	natio	on																		
С	RW	DTX									D	efau	ılt TX	(va	lue																	
												pecif etwe	fies v een:	vha	at th	e R	ADI	0 v	vill 1	tran	smit	t wh	en i	t is	not	staı	rtec	d, i.e	١.			
														ENT	ΓS_F	REA	DY	and	RA	DIO	.TAS	SKS_	STA	RT								
											RA	ADIC	D.EVI	ENT	ΓS_E	ND	an	d R	ADI	0.T	ASKS	S_ST	ART									



Bit number		31	30 2	29 2	28 2	7 2	6 25	5 24	4 23	3 22	21	20	19	18	17 :	16 1	15 1	4 13	3 12	11	10 9	9 8	7	6	5	4	3 2	2 :	1 0
Id																					(0							Α
Reset 0x00000200		0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0 :	L C	0	0	0	0	0 (0 (0 0
ld RW Field	Value Id	Va	lue						D	escr	ipti	on																	
									R/	ADIC	D.E\	/EN	TS_	END) an	d R	ADI	0.E\	/ENT	S_D	ISAE	BLED)						
	B1	0							Tr	ans	mit	'1'																	
	В0	1							Tr	ans	mit	'0'																	
	Center	2							Tr	ans	mit	cen	iter	fred	que	ncy													
									W	'hen	tur	ning	g the	cry	ysta	l fo	r ce	ntre	frec	uen	cy, t	he	RAD	IO n	nust	t			
									be	e set	t in	DTX	(= C	ent	er r	nod	le to	be	able	to a	chie	eve	the	ехр	ecte	d			
									ac	cur	асу.																		

23.14.46 POWER

Address offset: 0xFFC
Peripheral power control

Bit r	numbe	r		31	. 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	1 13	3 12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 1
Id	RW	Field	Value Id	Va	lue							De	scri	ipti	on																			
Α	RW	POWER										Pe	riph	nera	ıl po	owe	er c	ont	rol	. Th	ie p	eri	phe	ral	and	its	regi	ste	rs v	vill	be			
												res	et 1	to it	s ir	itia	l st	ate	by	sw	itc	hin	g th	е ре	ripl	hera	al o	ff a	nd t	the	n			
												ba	ck c	n a	gai	n.																		
			Disabled	0								Pe	riph	nera	ıl is	pov	wei	red	off															
			Enabled	1								Pe	riph	nera	ıl is	po	wei	red	on															

23.15 Electrical Specification

23.15.1 General Radio Characteristics

Symbol	Description	Min.	Тур.	Max.	Units
f_{OP}	Operating frequencies	2360		2500	MHz
f _{PLL,PROG,RES}	PLL programming resolution		2		kHz
f _{PLL,CH,SP}	PLL channel spacing		1		MHz
f _{DELTA,1M}	Frequency deviation @ 1 Msps		±170		kHz
f _{DELTA,BLE,1M}	Frequency deviation @ BLE 1Msps		±250		kHz
f _{DELTA,2M}	Frequency deviation @ 2 Msps		±320		kHz
fsk _{SPS}	On-the-air data rate	1		2	Msps

23.15.2 Radio current consumption (Transmitter)

Symbol	Description	Min.	Тур.	Max.	Units
I _{TX,PLUS4dBM,DCDC}	TX only run current (DCDC, 3V) P _{RF} =+4 dBm		7.5		mA
I _{TX,PLUS4dBM}	TX only run current P _{RF} = +4 dBm		16.6		mA
I _{TX,0dBM,DCDC}	TX only run current (DCDC, 3V)P _{RF} = 0dBm		5.3		mA
I _{TX,0dBM}	TX only run current P _{RF} = 0dBm		11.6		mA
I _{TX,MINUS4dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -4dBm		4.2		mA
I _{TX,MINUS4dBM}	TX only run current P _{RF} = -4 dBm		9.3		mA
I _{TX,MINUS8dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -8 dBm		3.8		mA
I _{TX,MINUS8dBM}	TX only run current P _{RF} = -8 dBm		8.4		mA
I _{TX,MINUS12dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -12 dBm		3.5		mA
I _{TX,MINUS12dBM}	TX only run current P _{RF} = -12 dBm		7.7		mA
I _{TX,MINUS16dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -16 dBm		3.3		mA
I _{TX,MINUS16dBM}	TX only run current P _{RF} = -16 dBm		7.3		mA
I _{TX,MINUS20dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -20 dBm		3.2		mA
I _{TX,MINUS20dBM}	TX only run current P _{RF} = -20 dBm		7.0		mA
I _{TX,MINUS40dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -40 dBm		2.7		mA



Symbol	Description	Min.	Тур.	Max.	Units
I _{TX,MINUS40dBM}	TX only run current P _{RF} = -40 dBm		5.9		mA
I _{START,TX,DCDC}	TX start-up current DCDC, 3V, P _{RF} = 4 dBm		4.0		mA
I _{START,TX}	TX start-up current, P _{RF} = 4 dBm		8.8		mA

23.15.3 Radio current consumption (Receiver)

Symbol	Description	Min.	Тур.	Max.	Units
I _{RX,1M,DCDC}	RX only run current (DCDC, 3V) 1Msps / 1Msps BLE		5.4		mA
I _{RX,1M}	RX only run current 1Msps / 1Msps BLE		11.7		mA
I _{RX,2M,DCDC}	RX only run current (DCDC, 3V) 2Msps		5.8		mA
I _{RX,2M}	RX only run current 2Msps		12.9		mA
I _{START,RX,1M,DCDC}	RX start-up current (DCDC 3V) 1Msps / 1Msps BLE		3.5		mA
I _{START,RX,1M}	RX start-up current 1Msps / 1Msps BLE		7.5		mA

23.15.4 Transmitter specification

Symbol	Description	Min.	Тур.	Max.	Units
P _{RF}	Maximum output power		4	6	dBm
P _{RFC}	RF power control range		24		dB
P _{RFCR}	RF power accuracy			±4	dB
P _{RF1,1}	1st Adjacent Channel Transmit Power 1 MHz (1 Msps)		-25		dBc
P _{RF2,1}	2nd Adjacent Channel Transmit Power 2 MHz (1 Msps)		-50		dBc
P _{RF1,2}	1st Adjacent Channel Transmit Power 2 MHz (2 Msps)		-25		dBc
P _{RF2,2}	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps)		-50		dBc

23.15.5 Receiver operation

Symbol	Description	Min.	Тур.	Max.	Units
P _{RX,MAX}	Maximum received signal strength at < 0.1% PER		0		dBm
P _{SENS,IT,1M}	Sensitivity, 1Msps nRF mode ¹⁵		-93		dBm
P _{SENS,IT,SP,1M,BLE}	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER=1E-3 ¹⁶		-96		dBm
P _{SENS,IT,LP,1M,BLE}	Sensitivity, 1Msps BLE ideal transmitter >=128 bytes BER=1E-4 17		-95		dBm
P _{SENS,IT,2M}	Sensitivity, 2Msps nRF mode ¹⁸		-89		dBm

23.15.6 RX selectivity

RX selectivity with equal modulation on interfering signal 19

Symbol	Description	Min.	Тур.	Max.	Units
C/I _{1M,co-channel}	1Msps mode, Co-Channel interference		9		dB
C/I _{1M,-1MHz}	1 Msps mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1M,+1MHz}	1 Msps mode, Adjacent (+1 MHz) interference		-10		dB
C/I _{1M,-2MHz}	1 Msps mode, Adjacent (-2 MHz) interference		-19		dB
C/I _{1M,+2MHz}	1 Msps mode, Adjacent (+2 MHz) interference		-42		dB
C/I _{1M,-3MHz}	1 Msps mode, Adjacent (-3 MHz) interference		-38		dB
C/I _{1M,+3MHz}	1 Msps mode, Adjacent (+3 MHz) interference		-48		dB
C/I _{1M,±6MHz}	1 Msps mode, Adjacent (≥6 MHz) interference		-50		dB
C/I _{1MBLE,co-channel}	1 Msps BLE mode, Co-Channel interference		6		dB

¹⁵ Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

¹⁷ Equivalent BER limit < 10E-04

¹⁸ Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

Wanted signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented



Symbol	Description	Min.	Тур.	Max.	Units
C/I _{1MBLE,-1MHz}	1 Msps BLE mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1MBLE,+1MHz}	1 Msps BLE mode, Adjacent (+1 MHz) interference		-9		dB
C/I _{1MBLE,-2MHz}	1 Msps BLE mode, Adjacent (-2 MHz) interference		-22		dB
C/I _{1MBLE,+2MHz}	1 Msps BLE mode, Adjacent (+2 MHz) interference		-46		dB
C/I _{1MBLE,>3MHz}	1 Msps BLE mode, Adjacent (≥3 MHz) interference		-50		dB
C/I _{1MBLE,image}	Image frequency Interference		-22		dB
C/I _{1MBLE,image,1MHz}	Adjacent (1 MHz) interference to in-band image frequency		-35		dB
C/I _{2M,co-channel}	2Msps mode, Co-Channel interference		10		dB
C/I _{2M,-2MHz}	2 Msps mode, Adjacent (-2 MHz) interference		6		dB
C/I _{2M,+2MHz}	2 Msps mode, Adjacent (+2 MHz) interference		-14		dB
C/I _{2M,-4MHz}	2 Msps mode, Adjacent (-4 MHz) interference		-20		dB
C/I _{2M,+4MHz}	2 Msps mode, Adjacent (+4 MHz) interference		-44		dB
C/I _{2M,-6MHz}	2 Msps mode, Adjacent (-6 MHz) interference		-42		dB
C/I _{2M,+6MHz}	2 Msps mode, Adjacent (+6 MHz) interference		-47		dB
C/I _{2M,≥12MHz}	2 Msps mode, Adjacent (≥12 MHz) interference		-52		dB

23.15.7 RX intermodulation

RX intermodulation²⁰

Symbol	Description	Min.	Тур.	Max.	Units
P _{IMD,1M}	IMD performance, 1 Msps, 3rd, 4th, and 5th offset channel		-33		dBm
P _{IMD,1M,BLE}	IMD performance, BLE 1 Msps, 3rd, 4th, and 5th offset channel		-30		dBm
P _{IMD,2M}	IMD performance, 2 Msps, 3rd, 4th, and 5th offset channel		-33		dBm

23.15.8 Radio timing

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXEN}	Time between TXEN task and READY event after channel		140		us
	FREQUENCY configured				
t _{TXEN,FAST}	Time between TXEN task and READY event after channel		40		us
	FREQUENCY configured (Fast Mode)				
t _{TXDISABLE}	Time between DISABLE task and DISABLED event when the		6		us
	radio was in TX and mode is set to 1Msps				
t _{TXDISABLE,2M}	Time between DISABLE task and DISABLED event when the		4		us
	radio was in TX and mode is set to 2Msps				
t _{RXEN}	Time between the RXEN task and READY event after channel		140		us
	FREQUENCY configured in default mode				
t _{RXEN,FAST}	Time between the RXEN task and READY event after channel		40		us
	FREQUENCY configured in fast mode				
t _{SWITCH}	The minimum time taken to switch from RX to TX or TX to RX		20		us
	(channel FREQUENCY unchanged)				
t _{RXDISABLE}	Time between DISABLE task and DISABLED event when the		0		us
	radio was in RX				
t _{TXCHAIN}	TX chain delay		0.6		us
t _{RXCHAIN}	RX chain delay		9.4		us
t _{RXCHAIN,2M}	RX chain delay in 2Msps mode		5		us

23.15.9 Received Signal Strength Indicator (RSSI) specifications

Symbol	Description	Min.	Тур.	Max.	Units
RSSI _{ACC}	RSSI Accuracy Valid range -90 to -20 dBm		±2		dB
RSSI _{RESOLUTION}	RSSI resolution		1		dB
RSSI _{PERIOD}	Sample period		8		us

Wanted signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.



23.15.10 Jitter

Symbol	Description	Min.	Тур.	Max.	Units	
t _{DISABLEDJITTER}	Jitter on DISABLED event relative to END event when shortcut		0.25		us	
	between END and DISABLE is enabled.					
t _{READYJITTER}	Jitter on READY event relative to TXEN and RXEN task.		0.25		us	

23.15.11 Delay when disabling the RADIO

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXDISABLE,1M}	Disable delay from TX.		6		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit				
t _{RXDISABLE,1M}	Disable delay from RX.		0		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit				



24 TIMER — Timer/counter

The TIMER can operate in two modes: timer and counter.

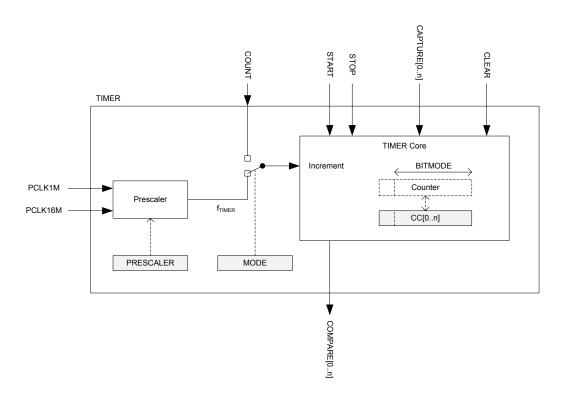


Figure 41: Block schematic for timer/counter

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timer input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The TIMER can operate in two modes, Timer mode and Counter mode. In both modes, the TIMER is started by triggering the START task, and stopped by triggering the STOP task. After the timer is stopped the timer can resume timing/counting by triggering the START task again. When timing/counting is resumed, the timer will continue from the value it had prior to being stopped.

In Timer mode, the TIMER's internal Counter register is incremented by one for every tick of the timer frequency f_{TIMER} as illustrated in *Figure 41: Block schematic for timer/counter* on page 230. The timer frequency is derived from PCLK16M as described in *Equation 1* using the values specified in the PRESCALER register:

```
f_{\text{TIMER}} = 16 \text{ MHz} / (2^{\text{PRESCALER}})
```

When f_{TIMER} <= 1 MHz the TIMER will use PCLK1M instead of PCLK16M for reduced power consumption.



In counter mode, the TIMER's internal Counter register is incremented by one each time the COUNT task is triggered, that is, the timer frequency and the prescaler are not utilized in counter mode. Similarly, the COUNT task has no effect in Timer mode.

The TIMER's maximum value is configured by changing the bit-width of the timer in the *BITMODE* on page 235 register.

PRESCALER on page 235 and the **BITMODE** on page 235 must only be updated when the timer is stopped. If these registers are updated while the TIMER is started then this may result in unpredictable behavior.

When the timer is incremented beyond its maximum value the Counter register will overflow and the TIMER will automatically start over from zero.

The Counter register can be cleared, that is, its internal value set to zero explicitly, by triggering the CLEAR task.

The TIMER implements multiple capture/compare registers.

Independent of prescaler setting the accuracy of the TIMER is equivalent to one tick of the timer frequency f_{TIMER} as illustrated in *Figure 41: Block schematic for timer/counter* on page 230.

24.1 Capture

The TIMER implements one capture task for every available capture/compare register.

Every time the CAPTURE[n] task is triggered, the Counter value is copied to the CC[n] register.

24.2 Compare

The TIMER implements one COMPARE event for every available capture/compare register.

A COMPARE event is generated when the Counter is incremented and then becomes equal to the value specified in one of the capture compare registers. When the Counter value becomes equal to the value specified in a capture compare register CC[n], the corresponding compare event COMPARE[n] is generated.

BITMODE on page 235 specifies how many bits of the Counter register and the capture/compare register that are used when the comparison is performed. Other bits will be ignored.

24.3 Task delays

After the TIMER is started, the CLEAR task, COUNT task and the STOP task will guarantee to take effect within one clock cycle of the PCLK16M.

24.4 Task priority

If the START task and the STOP task are triggered at the same time, that is, within the same period of PCLK16M, the STOP task will be prioritized.

24.5 Registers

Table 38: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40008000	TIMER	TIMERO	Timer 0	This timer instance has 4 CC registers
				(CC[03])
0x40009000	TIMER	TIMER1	Timer 1	This timer instance has 4 CC registers
				(CC[03])



Base address	Peripheral	Instance	Description	Configuration
0x4000A000	TIMER	TIMER2	Timer 2	This timer instance has 4 CC registers
				(CC[03])
0x4001A000	TIMER	TIMER3	Timer 3	This timer instance has 6 CC registers
				(CC[05])
0x4001B000	TIMER	TIMER4	Timer 4	This timer instance has 6 CC registers
				(CC[05])

Table 39: Register Overview

Register	Offset	Description	
TASKS_START	0x000	Start Timer	
TASKS_STOP	0x004	Stop Timer	
TASKS_COUNT	0x008	Increment Timer (Counter mode only)	
TASKS_CLEAR	0x00C	Clear time	
TASKS_SHUTDOWN	0x010	Shut down timer	Deprecated
TASKS_CAPTURE[0]	0x040	Capture Timer value to CC[0] register	
TASKS_CAPTURE[1]	0x044	Capture Timer value to CC[1] register	
TASKS_CAPTURE[2]	0x048	Capture Timer value to CC[2] register	
TASKS_CAPTURE[3]	0x04C	Capture Timer value to CC[3] register	
TASKS_CAPTURE[4]	0x050	Capture Timer value to CC[4] register	
TASKS_CAPTURE[5]	0x054	Capture Timer value to CC[5] register	
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match	
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match	
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match	
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match	
EVENTS_COMPARE[4]	0x150	Compare event on CC[4] match	
EVENTS_COMPARE[5]	0x154	Compare event on CC[5] match	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
MODE	0x504	Timer mode selection	
BITMODE	0x508	Configure the number of bits used by the TIMER	
PRESCALER	0x510	Timer prescaler register	
CC[0]	0x540	Capture/Compare register 0	
CC[1]	0x544	Capture/Compare register 1	
CC[2]	0x548	Capture/Compare register 2	
CC[3]	0x54C	Capture/Compare register 3	
CC[4]	0x550	Capture/Compare register 4	
CC[5]	0x554	Capture/Compare register 5	

24.5.1 SHORTS

Address offset: 0x200 Shortcut register

Bitı	numbe	er		31	1 30	29	28	27	26	25 2	24 2	23 22	2 21	20	19	18	17	16	15	14 1	3 1	2 11	10	9	8	7	6 5	4	3	2	1	0
Id																				١	ИΙ	_ K	J	1	Н		F	Е	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0 0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							Desc	ripti	on																		
Α	RW	COMPAREO_CLEAR									S	Short	tcut	bet	wee	n C	ON	ΙPΑ	RE[0] e	ven	t and	d CLI	EAR	tas	k						
											S	See E	EVEN	ITS_	co	MP	4RE	[0]	and	I TA	SKS	_CLE	AR									
			Disabled	0								Disab	ole s	hort	cut																	
			Enabled	1							E	nab	le sh	ort	cut																	
В	RW	COMPARE1_CLEAR									S	Short	tcut	bet	wee	n C	ON	ΙPΑ	RE[1] e	ven	t and	d CLI	EAR	tas	k						
											5	See E	EVEN	ITS	coi	MP	4RE	[1]	and	l <i>TA</i>	SKS	CLE	AR									
			Disabled	0									ole s																			
			Enabled	1							Е	nab	le sh	ort	cut																	



Bit	numbe	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					M L K J I H F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
С	RW	COMPARE2_CLEAR			Shortcut between COMPARE[2] event and CLEAR task
					See EVENTS_COMPARE[2] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW	COMPARE3_CLEAR			Shortcut between COMPARE[3] event and CLEAR task
					See EVENTS_COMPARE[3] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
E	RW	COMPARE4_CLEAR			Shortcut between COMPARE[4] event and CLEAR task
					See EVENTS_COMPARE[4] and TASKS_CLEAR
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
F	RW	COMPARE5 CLEAR		_	Shortcut between COMPARE[5] event and CLEAR task
		_			
			Disabled	0	See EVENTS_COMPARE[5] and TASKS_CLEAR Disable shortcut
			Enabled	1	Enable shortcut
Н	RW	COMPAREO STOP	Litablea	1	Shortcut between COMPARE[0] event and STOP task
••		00720_0.0.			
			D: 11 1	0	See EVENTS_COMPARE[0] and TASKS_STOP
			Disabled	0	Disable shortcut
	D\A/	COMPARE1_STOP	Enabled	1	Enable shortcut Shortcut between COMPARE[1] event and STOP task
'	11.00	COMPAREI_STOP			
					See EVENTS_COMPARE[1] and TASKS_STOP
			Disabled	0	Disable shortcut
	DVA	COMPARES STOR	Enabled	1	Enable shortcut Shortcut between COMPART(2) event and CTOP task
J	KVV	COMPARE2_STOP			Shortcut between COMPARE[2] event and STOP task
					See EVENTS_COMPARE[2] and TASKS_STOP
			Disabled	0	Disable shortcut
.,			Enabled	1	Enable shortcut
K	RW	COMPARE3_STOP			Shortcut between COMPARE[3] event and STOP task
					See EVENTS_COMPARE[3] and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
L	RW	COMPARE4_STOP			Shortcut between COMPARE[4] event and STOP task
					See EVENTS_COMPARE[4] and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
М	RW	COMPARE5_STOP			Shortcut between COMPARE[5] event and STOP task
					See EVENTS_COMPARE[5] and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

24.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	r		31	. 30	29	28	27	26	25 :	24	23 2	22 2	1 2	0 1	9 1	8 1	7 1	5 15	14	13	12	11	10	9	8 7	' E	5	4	3	2	1 0
Id													F		E [) (СВ	β Δ														
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 0) (0 () (0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	COMPARE0									,	Wri	te '1	' to	En	abl	e in	terr	upt	for	СО	MP	٩RE	[0] 6	evei	nt						



Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0	$0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;$
Id RW Field	Value Id	Value	Description
			See EVENTS_COMPARE[0]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW COMPARE1			Write '1' to Enable interrupt for COMPARE[1] event
			See EVENTS_COMPARE[1]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW COMPARE2			Write '1' to Enable interrupt for COMPARE[2] event
			See EVENTS_COMPARE[2]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW COMPARE3			Write '1' to Enable interrupt for COMPARE[3] event
			See EVENTS_COMPARE[3]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW COMPARE4			Write '1' to Enable interrupt for COMPARE[4] event
			See EVENTS_COMPARE[4]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW COMPARES			Write '1' to Enable interrupt for COMPARE[5] event
			See EVENTS_COMPARE[5]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

24.5.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit r	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				FEDCBA
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW COMPAREO			Write '1' to Disable interrupt for COMPARE[0] event
				See EVENTS_COMPARE[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW COMPARE1			Write '1' to Disable interrupt for COMPARE[1] event
				See EVENTS_COMPARE[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW COMPARE2			Write '1' to Disable interrupt for COMPARE[2] event
				See EVENTS_COMPARE[2]
		Clear	1	Disable



Bit nur	mber		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C B A
Reset	0x0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id R	RW Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D R	RW COMPARE3			Write '1' to Disable interrupt for COMPARE[3] event
				See EVENTS_COMPARE[3]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E R	RW COMPARE4			Write '1' to Disable interrupt for COMPARE[4] event
				See EVENTS_COMPARE[4]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F R	RW COMPARE5			Write '1' to Disable interrupt for COMPARE[5] event
				See EVENTS_COMPARE[5]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

24.5.4 MODE

Address offset: 0x504 Timer mode selection

Bit	numb	er		31 3	30 2	9 2	8 27	7 26	5 25	24	23	22	21 2	20 1	L9 1	.8 1	7 1	6 1	5 14	13	12	11	10 !	9	8 7	7 6	5	4	3	2	1 0
Id																															А А
Res	et 0x(0000000		0	0 (0	0 0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						De	scri	ptio	n																	
Α	RW	MODE									Tir	mer	mod	de																	
			Timer	0							Se	lect '	Tim	er r	nod	e															
			Counter	1							Se	lect	Cou	inte	r m	ode	:												De	pred	ated
			LowPowerCounter	2							Se	lect	Low	/ Po	wei	· Co	unt	er r	nod	e											

24.5.5 BITMODE

Address offset: 0x508

Configure the number of bits used by the TIMER

Bit	numb	er		31	30	29	28 :	27 :	26	25 :	24	23 :	22 :	21 :	20 :	19	18 :	17 :	16	15	14 :	13 1	12 1	1 1	0 9	8	7	6	5	4	3	2	1 (
Id																																	A A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 (
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			ı
Α	RW	BITMODE										Tim	er b	bit v	wid	th																		
			16Bit	0								16 l	oit t	time	er b	it v	vidt	h																
			08Bit	1								8 bi	t tir	mei	bit	t wi	dth																	
			24Bit	2								24 l	oit t	time	er b	it v	vidt	h																
			32Bit	3								32 l	oit t	time	er b	it v	vidt	h																

24.5.6 PRESCALER

Address offset: 0x510 Timer prescaler register



Bit	numbe	er		31 30 29 28 2	7 26 25 24	1 23 22 2	1 20 19	18 1	7 16	15 14	13 1	2 11	10 9	9 8	7	6	5	4	3 2	2 1	0
Id																			A A	A	Α
Res	et 0x0	0000004		0 0 0 0 0	0 0 0	000	0 0	0 (0 (0 0	0	0 0	0 () (0	0	0	0	0 1	. 0	0
Id	RW	Field	Value Id	Value		Descrip	tion														
Α	RW	PRESCALER		[09]		Prescale	er value														_

24.5.7 CC[0]

Address offset: 0x540

Capture/Compare register 0

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id		A A A A A A A A A A A A A A A A A A A	A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id RW Field	Value Id	Value Description	
A RW CC		Capture/Compare value	

the TIMER.

24.5.8 CC[1]

Address offset: 0x544

Capture/Compare register 1

Bit	num	ber			31	1 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 1	7 16	5 15	14	13	12 1	.1 10	9	8	7	6	5	4	3	2 1	0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	4 4	4 Α	\ <i>A</i>	A A	Α	Α	Α	A A	4 А	Α	Α	Α	Α	Α	Α	Α	А А	Α
Re	set 0	x00	000000		0	0	0	0	0	0	0	0	0	0	0 (0 (0 0) (0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0
Id	RV	N	Field	Value Id	Va	alue							Des	crip	otio	n																	
Α	RV	N (СС										Cap	ture	e/Co	omp	oare	va	lue														

24.5.9 CC[2]

Address offset: 0x548

Capture/Compare register 2

Bit number		31 30	29	28	27	26	25 2	24 2	3 22	2 21	20	19	18 1	L7 1	6 1	5 14	13	12	11	10	9 1	3 7	6	5	4	3	2 :	1 0
Id		A A	Α	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α.	A A	Α Α	A	Α	Α	Α	Α	A ,	Α Α	A	Α	Α	Α .	A A	4 A
Reset 0x000000	00	0 0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0 (0 0
ld RW Field	Value Id	Value	9					D	esc	ripti	on																	
A RW CC								С	aptı	ıre/	Com	npai	e va	alue														
								С	nly	the	num	nbei	of	bits	indi	icat	ed b	у ВІ	тм	ODE	wi	l be	use	ed b	у			
								+H	ne T	IME	R																	

24.5.10 CC[3]

Address offset: 0x54C

Capture/Compare register 3

Bit	numbe	er		31	. 30	29	28	3 27	' 26	25	24	23	22 :	21 2	20 1	19 :	18	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	RW	CC										Cap	tur	e/C	om	par	e v	alue	Э															
												Onl	•			ber	of	bits	s in	dic	ate	d b	y BI	TM	10D	Εw	ill k	e u	ised	l by	,			



24.5.11 CC[4]

Address offset: 0x550

Capture/Compare register 4

Bitı	numbe	er		31	30	29	28	27	26 2	25	24	23 2	22 2:	1 20	19	18	17	16	15	14 1	13 1	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	A	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	Α.	А А	A	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cript	tion																		
Α	RW	CC										Cap	ture	/Co	mpa	re ۱	/alu	e														
												Onlv	/ the	nu	mhe	ır ol	f hit	c in	dica	ated	hv	RITN	4OD)F \A	ill h	ا ا ۵	has	hv				
												Om	, tile	· IIu	11100		ı Dit	3 111	iuice	icc	Бу	5111	no.	_ ~	111 1	c u.	scu	Бу				
											1	the	TIMI	ER.																		

24.5.12 CC[5]

Address offset: 0x554

Capture/Compare register 5

$23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
A A A A A A A A A A A A A A A A A A A
$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Description
Capture/Compare value
Only the number of bits indicated by BITMODE will be used by

24.6 Electrical Specification

24.6.1 Timers Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{TIMER_1M}	Run current with 1 MHz clock input (PCLK1M)	3	5	8	μΑ
I _{TIMER_16M}	Run current with 16 MHz clock input (PCLK16M)	50	70	120	μΑ
t _{TIMER,START}	Time from START task is given until timer starts counting		0.25		μs



25 RTC — Real-time counter

The Real-time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK).

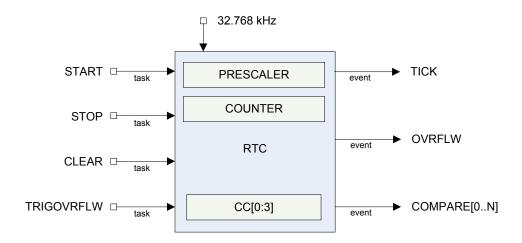


Figure 42: RTC block schematic

The RTC module features a 24-bit COUNTER, a 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

25.1 Clock source

The RTC will run off the LFCLK.

The COUNTER resolution will therefore be $30.517 \,\mu s$. Depending on the source, the RTC is able to run while the HFCLK is OFF and PCLK16M is not available.

The software has to explicitely start LFCLK before using the RTC.

See CLOCK — Clock control on page 98 for more information about clock sources.

25.2 Resolution versus overflow and the PRESCALER

Counter increment frequency:

```
f_{RTC} [kHz] = 32.768 / (PRESCALER + 1 )
```

The PRESCALER register is read/write when the RTC is stopped. The PRESCALER register is read-only once the RTC is STARTed. Writing to the PRESCALER register when the RTC is started has no effect.

The PRESCALER is restarted on START, CLEAR and TRIGOVRFLW, that is, the prescaler value is latched to an internal register (<<PRESC>>) on these tasks.

Examples:

1. Desired COUNTER frequency 100 Hz (10 ms counter period)

$$f_{RTC} = 99.9 \; Hz$$



10009.576 µs counter period

2. Desired COUNTER frequency 8 Hz (125 ms counter period)

PRESCALER = round(32.768 kHz / 8 Hz) - 1 = 4095

 $f_{RTC} = 8 Hz$

125 ms counter period

Table 40: RTC resolution versus overflow

Prescaler	Counter resolution	Overflow
0	30.517 μs	512 seconds
28-1	7812.5 μs	131072 seconds
2 ¹² -1	125 ms	582.542 hours

25.3 COUNTER register

The COUNTER increments on LFCLK when the internal PRESCALER register (<<PRESC>>) is 0x00. <<PRESC>> is reloaded from the PRESCALER register. If enabled, the TICK event occurs on each increment of the COUNTER. The TICK event is disabled by default.

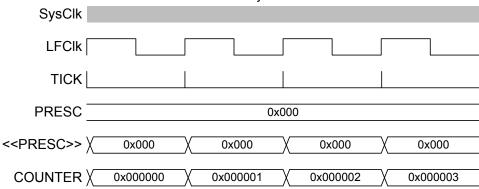


Figure 43: Timing diagram - COUNTER_PRESCALER_0

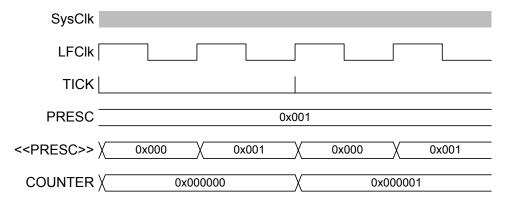


Figure 44: Timing diagram - COUNTER_PRESCALER_1

25.4 Overflow features

The TRIGOVRFLW task sets the COUNTER value to 0xFFFFF0 to allow SW test of the overflow condition. OVRFLW occurs when COUNTER overflows from 0xFFFFFF to 0.

Important: The OVRFLW event is disabled by default.



25.5 TICK event

The TICK event enables low power "tick-less" RTOS implementation as it optionally provides a regular interrupt source for a RTOS without the need to use the ARM® SysTick feature.

Using the RTC TICK event rather than the SysTick allows the CPU to be powered down while still keeping RTOS scheduling active.

Important: The TICK event is disabled by default.

25.6 Event control feature

To optimize RTC power consumption, events in the RTC can be individually disabled to prevent PCLK16M and HFCLK being requested when those events are triggered. This is managed using the EVTEN register.

For example, if the TICK event is not required for an application, this event should be disabled as it is frequently occurring and may increase power consumption if HFCLK otherwise could be powered down for long durations.

This means that the RTC implements a slightly different task and event system compared to the standard system described in *Figure 9: Tasks, events, shortcuts, and interrupts* on page 66. The RTC task and event system is illustrated in *Figure 45: Tasks, events and interrupts in the RTC* on page 240.

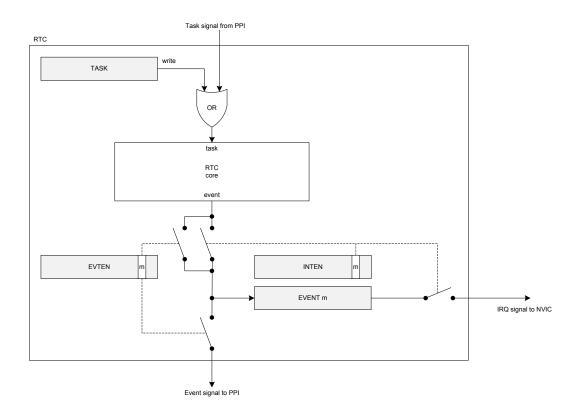


Figure 45: Tasks, events and interrupts in the RTC

25.7 Compare feature

There are a number of Compare registers.

For more information, see table *Instances*.

When setting a compare register, the following behavior of the RTC compare event should be noted:



If a CC register value is 0 when a CLEAR task is set, this will not trigger a COMPARE event.

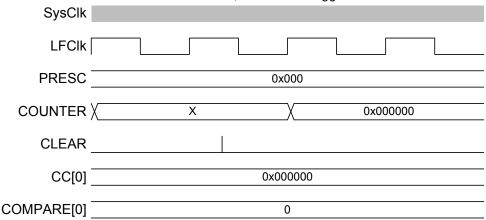


Figure 46: Timing diagram - COMPARE_CLEAR

 If a CC register is N and the COUNTER value is N when the START task is set, this will not trigger a COMPARE event.

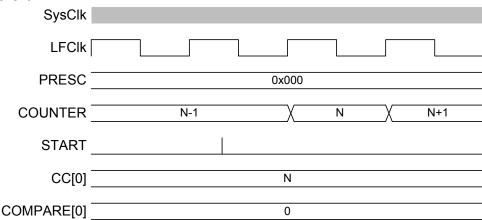


Figure 47: Timing diagram - COMPARE START

• COMPARE occurs when a CC register is N and the COUNTER value transitions from N-1 to N.

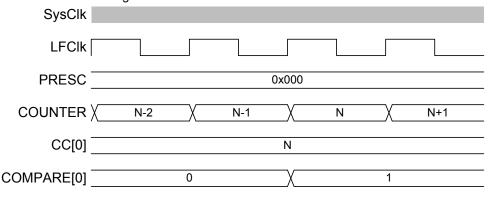


Figure 48: Timing diagram - COMPARE

• If the COUNTER is N, writing N+2 to a CC register is guaranteed to trigger a COMPARE event at N+2.



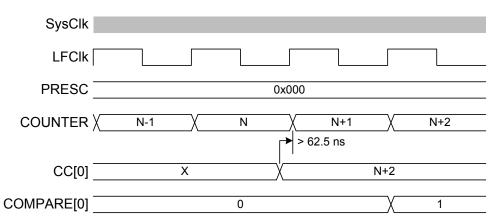


Figure 49: Timing diagram - COMPARE N+2

• If the COUNTER is N, writing N or N+1 to a CC register may not trigger a COMPARE event.

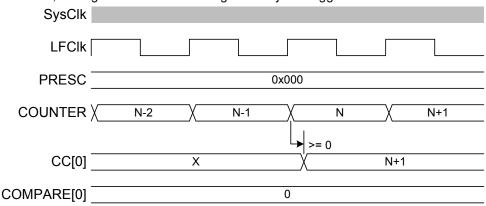


Figure 50: Timing diagram - COMPARE_N+1

• If the COUNTER is N and the current CC register value is N+1 or N+2 when a new CC value is written, a match may trigger on the previous CC value before the new value takes effect. If the current CC value greater than N+2 when the new value is written, there will be no event due to the old value.

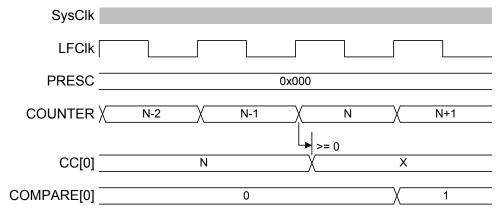


Figure 51: Timing diagram - COMPARE_N-1

25.8 TASK and EVENT jitter/delay

Jitter or delay in the RTC is due to the peripheral clock being a low frequency clock (LFCLK) which is not synchronous to the faster PCLK16M.

Registers in the peripheral interface, part of the PCLK16M domain, have a set of mirrored registers in the LFCLK domain. For example, the COUNTER value accessible from the CPU is in the PCLK16M domain and is latched on read from an internal register called COUNTER in the LFCLK domain. COUNTER is the register which is actually modified each time the RTC ticks. These registers must be synchronised between clock domains (PCLK16M and LFCLK).



The following is a summary of the jitter introduced on tasks and events. Figures illustrating jitter follow.

Table 41: RTC jitter magnitudes on tasks

Task	Delay
CLEAR, STOP, START, TRIGOVRFLOW	+15 to 46 μs

Table 42: RTC jitter magnitudes on events

Operation/Function	Jitter
START to COUNTER increment	+/- 15 μs
COMPARE to COMPARE ²¹	+/- 62.5 ns

1. CLEAR and STOP (and TRIGOVRFLW; not shown) will be delayed as long as it takes for the peripheral to clock a falling edge and rising of the LFCLK. This is between 15.2585 μ s and 45.7755 μ s – rounded to 15 μ s and 46 μ s for the remainder of the section.

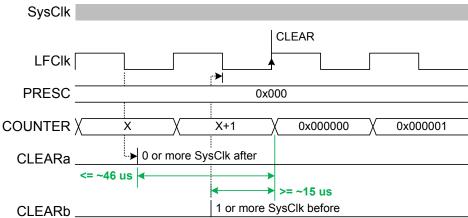


Figure 52: Timing diagram - DELAY_CLEAR

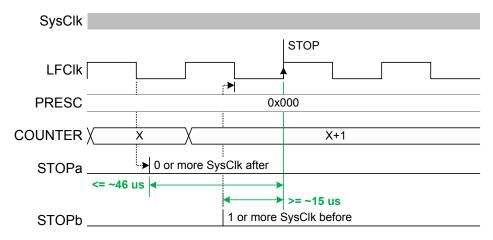


Figure 53: Timing diagram - DELAY_STOP

2. The START task will start the RTC. Assuming that the LFCLK was previously running and stable, the first increment of COUNTER (and instance of TICK event) will be typically after 30.5 μs +/-15 μs. In some cases, in particular if the RTC is STARTed before the LFCLK is running, that timing can be up to ~250 μs. The software should therefore wait for the first TICK if it has to make sure the RTC is running. Sending a TRIGOVRFLW task sets the COUNTER to a value close to overflow. However, since the update of COUNTER relies on a stable LFCLK, sending this task while LFCLK is not running will start LFCLK, but the update will then be delayed by the same amount of time of up to ~250 us. The figures show the smallest and largest delays to on the START task which appears as a +/-15 μs jitter on the first COUNTER increment.

Note: 32.768 kHz clock jitter is additional to the numbers provided above.

²¹ Assumes RTC runs continuously between these events.



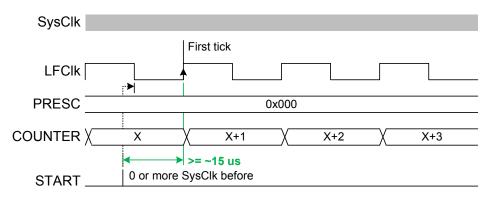


Figure 54: Timing diagram - JITTER_START-

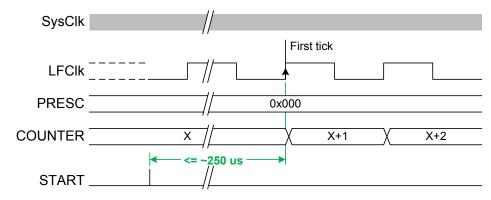


Figure 55: Timing diagram - JITTER_START+

25.9 Reading the COUNTER register

To read the COUNTER register, the internal <<COUNTER>> value is sampled.

To ensure that the <<COUNTER>> is safely sampled (considering an LFCLK transition may occur during a read), the CPU and core memory bus are halted for three cycles by lowering the core PREADY signal. The Read takes the CPU 2 cycles in addition resulting in the COUNTER register read taking a fixed five PCLK16M clock cycles.

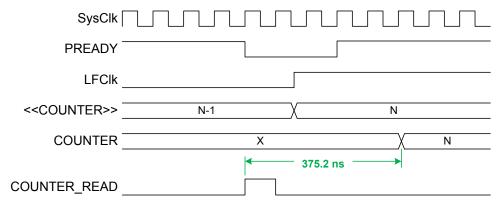


Figure 56: Timing diagram - COUNTER_READ

25.10 Registers

Table 43: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000B000	RTC	RTC0	Real-time counter 0	CC[02] implemented, CC[3] not
				implemented



Base address	Peripheral	Instance	Description	Configuration	
0x40011000	RTC	RTC1	Real-time counter 1	CC[03] implemented	
0x40024000	RTC	RTC2	Real-time counter 2.	CC[03] implemented	

Table 44: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start RTC COUNTER
TASKS_STOP	0x004	Stop RTC COUNTER
TASKS_CLEAR	0x008	Clear RTC COUNTER
TASKS_TRIGOVRFLW	0x00C	Set COUNTER to 0xFFFFF0
EVENTS_TICK	0x100	Event on COUNTER increment
EVENTS_OVRFLW	0x104	Event on COUNTER overflow
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
EVTEN	0x340	Enable or disable event routing
EVTENSET	0x344	Enable event routing
EVTENCLR	0x348	Disable event routing
COUNTER	0x504	Current COUNTER value
PRESCALER	0x508	12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is
		stopped
CC[0]	0x540	Compare register 0
CC[1]	0x544	Compare register 1
CC[2]	0x548	Compare register 2
CC[3]	0x54C	Compare register 3

25.10.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	TICK			Write '1' to Enable interrupt for TICK event
					See EVENTS_TICK
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	OVRFLW			Write '1' to Enable interrupt for OVRFLW event
					See EVENTS_OVRFLW
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	COMPARE0			Write '1' to Enable interrupt for COMPARE[0] event
					See EVENTS_COMPARE[0]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	COMPARE1			Write '1' to Enable interrupt for COMPARE[1] event
					See EVENTS_COMPARE[1]
			Set	1	Enable
			Disabled	0	Read: Disabled



Bit r	numbe	er		31	30 29	28 2	7 26	25 24	4 23 2	2 2	1 20	19	18	17	16	15	14 1	13 1	2 1:	1 10	9	8	7	6	5 4	1 3	2	1	0
Id												F	Е	D	С													В	Α
Res	et OxO	0000000		0	0 0	0 (0 0	0 0	0 0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Val	ue				Desc	ript	tion																		
			Enabled	1					Reac	d: Er	nabl	ed																	
Е	RW	COMPARE2							Writ	e '1	' to	Ena	ble	inte	rru	pt f	or C	OM	PAR	E[2]	eve	ent							
									See	EVE	NTS	_cc	МР	ARE	[2]														
			Set	1					Enab	ole																			
			Disabled	0					Read	d: D	isab	led																	
			Enabled	1					Read	d: Er	nabl	ed																	
F	RW	COMPARE3							Writ	e '1	' to	Ena	ble	inte	rru	pt f	or C	OM	PAR	E[3]	eve	ent							
									See	EVE	NTS	_cc	MP	ARE	[3]														
			Set	1					Enab	ole																			
			Disabled	0					Read	d: D	isab	led																	
			Enabled	1					Read	d: Er	nabl	ed																	

25.10.2 INTENCLR

Address offset: 0x308

Disable interrupt

D1.	Jubi	e interrupt																																	
Bit	numbe	er		3	1 30	29	28	27	26	25	24	2	3 22	21 2	0 :	19 1	8	17 :	16	15	14	13	12	2 1	1 1	0 9	9 (3 7	, (6	5	4	3 2	2 :	1 (
Id																F	Ε	D	С															ı	3 <i>A</i>
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	C	0 0	0 (0	0 (0	0	0	0	0	0	0	(0	0) () () (0	0	0) () (0 (
Id	RW	Field	Value Id	٧	alue	2						D	escri	iption	n																				
Α	RW	TICK										V	√rite	'1' to	Di	isab	le i	inte	rrı	upt	foi	· TI	CK	ev	ent										
												S	ee <i>EV</i>	/ENT.	s_:	TICK																			
			Clear	1									isabl		Ī																				
			Disabled	0								R	ead:	Disal	ble	d																			
			Enabled	1								R	ead:	Enab	oled	d																			
В	RW	OVRFLW										W	Vrite	'1' to	Di	isab	le i	inte	rrı	upt	foi	۰ 0۱	/RF	LV	V ev	ent	t								
												S	ee <i>EV</i>	/ENT	5 (OVR	FL	w																	
			Clear	1									isabl		_																				
			Disabled	0								R	ead:	Disal	ble	d																			
			Enabled	1								R	ead:	Enab	oled	d																			
С	RW	COMPARE0										W	√rite	'1' to	Di	isab	le i	inte	rrı	upt	foi	· cc	M	PΑ	RE[0] e	eve	nt							
												S	ee <i>E</i> V	/ENT	s (CON	1P)	4RE	[O	1															
			Clear	1									isabl		_				,																
			Disabled	0								R	ead:	Disal	ble	d																			
			Enabled	1								R	ead:	Enab	oled	d																			
D	RW	COMPARE1										W	V rite	'1' to	Di	isab	le i	inte	rrı	upt	foi	· cc	M	PΑ	RE[1] e	eve	nt							
												S	ee <i>EV</i>	/ENT	5 (CON	1P)	4RE	[1	1															
			Clear	1									isabl		_																				
			Disabled	0								R	ead:	Disal	ble	d																			
			Enabled	1								R	ead:	Enab	oled	b																			
Ε	RW	COMPARE2										W	√rite	'1' to	Di	isab	le i	inte	rrı	upt	foi	· cc	M	PΑ	RE[2] e	eve	nt							
												S	ee <i>EV</i>	/ENT.	· ·	CON	1P)	4RE	[2]	1															
			Clear	1									isabl		_																				
			Disabled	0								R	ead:	Disal	ble	d																			
			Enabled	1								R	ead:	Enab	oled	b																			
F	RW	COMPARE3										W	√rite	'1' to	Di	isab	le i	inte	rrı	upt	foi	· CC	M	PA	RE[3] e	eve	nt							
												S	ee <i>EV</i>	/ENT	5 (CON	1P)	4RE	[3]	1															
			Clear	1									isabl						,																
			Disabled	0									ead:		ble	d																			
			Enabled	1								R	ead:	Enab	oled	b																			



25.10.3 EVTEN

Address offset: 0x340

Enable or disable event routing

Bit	numbe	er		31 30	29 :	28 27	7 26	25	24 2	23	22 21	20) 19	18	3 17	16	5 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id													F	Ε	D	С														В	3 A
Res	et 0x0	0000000		0 0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value					ı	Des	scripti	on																			
Α	RW	TICK							1	Ena	able o	r di	sab	le e	evei	nt r	out	ing	for	TIC	Кe	ven	t								
									9	See	e <i>EVEN</i>	ITS		CK																	
			Disabled	0					1	Dis	able		_																		
			Enabled	1					1	Ena	able																				
В	RW	OVRFLW							ı	Ena	able o	r di	sab	le e	eve	nt r	out	ing	for	٥٧	RFL	.W	eve	nt							
									9	See	e <i>EVEN</i>	ITS	_01	VRF	LW																
			Disabled	0					ı	Dis	able																				
			Enabled	1					ı	Ena	able																				
С	RW	COMPARE0							1	Ena	able o	r di	sab	le e	evei	nt r	out	ing	for	СО	MP	ARI	[0]	eve	nt						
									9	See	e <i>EVEN</i>	ITS	_cc	ЭМІ	PAR	RE[C	0]														
			Disabled	0					ı	Dis	able																				
			Enabled	1					ŀ	Ena	able																				
D	RW	COMPARE1							1	Ena	able o	r di	sab	le e	evei	nt r	out	ing	for	СО	MP	ARI	[1]	eve	nt						
									9	See	e <i>EVEN</i>	ITS	_cc	ЭМІ	PAR	?E[1	1]														
			Disabled	0					ı	Dis	able																				
			Enabled	1					1	Ena	able																				
Ε	RW	COMPARE2							1	Ena	able o	r di	sab	le e	eve	nt r	out	ing	for	CO	MP	ARI	[2]	eve	nt						
									9	See	e <i>EVEN</i>	ITS	_cc	ЭМІ	PAR	RE[2	2]														
			Disabled	0					1	Dis	able																				
			Enabled	1					1	Ena	able																				
F	RW	COMPARE3							ı	Ena	able o	r di	sab	le e	ever	nt r	out	ing	for	СО	MP	ARI	[3]	eve	nt						
									9	See	e <i>EVEN</i>	ITS	_cc	ЭМ	PAR	RE[3	3]														
			Disabled	0					ı	Dis	able																				
			Enabled	1					1	Ena	able																				

25.10.4 EVTENSET

Address offset: 0x344 Enable event routing

Bit r	number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C B A
Res	et 0x00000000		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field	Value Id	Value	Description
Α	RW TICK			Write '1' to Enable event routing for TICK event
				See EVENTS_TICK
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW OVRFLW			Write '1' to Enable event routing for OVRFLW event
				See EVENTS_OVRFLW
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW COMPAREO			Write '1' to Enable event routing for COMPARE[0] event
				See EVENTS_COMPARE[0]
		Set	1	Enable



Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	COMPARE1			Write '1' to Enable event routing for COMPARE[1] event
					See EVENTS_COMPARE[1]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Ε	RW	COMPARE2			Write '1' to Enable event routing for COMPARE[2] event
					See EVENTS_COMPARE[2]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	COMPARE3			Write '1' to Enable event routing for COMPARE[3] event
					See EVENTS COMPARE[3]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

25.10.5 EVTENCLR

Address offset: 0x348 Disable event routing

Bit r	numbe	r		31 30	29	9 28	27	26	25	24 2	23 2	22 2	1 2	0 1	19 1	8 1	7 1	6 1	5 14	4 13	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id															F E	Ξ [) (В	Α
Rese	et 0x0	0000000		0 0	0	0	0	0	0	0 (0	0 (0) (0 0) (0	0	0	0	0	0	0	0	0 (0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Valu	е					C	Des	crip	tion	ı																		
Α	RW	TICK								٧	Vrit	te '1	' to	Di	sabl	e e	ven	t ro	utii	ng f	or T	ICK	eve	nt								
										S	iee	EVE	NTS	5_7	ГІСК																	
			Clear	1						C	Disa	ble																				
			Disabled	0						R	Rea	d: D	isab	ole	d																	
			Enabled	1						R	Rea	d: Eı	nab	led	ł																	
В	RW	OVRFLW								٧	Vrit	te '1	' to	Di	sabl	e e	ven	t ro	utii	ng f	or C	VRI	LW	eve	ent							
										S	ee	EVE	NTS	s_c	OVR	FLV	v															
			Clear	1						C	Disa	ble																				
			Disabled	0						R	Rea	d: D	isab	ole	d																	
			Enabled	1						R	Rea	d: Eı	nab	led	ł																	
С	RW	COMPARE0								٧	Vrit	te '1	' to	Di	sabl	e e	ven	t ro	utii	ng f	or C	OM	PAF	RE[O)] ev	ent	t					
										S	ee	EVE	NTS	s_c	СОМ	1PA	RE[0]														
			Clear	1						C	Disa	ble																				
			Disabled	0						R	Rea	d: D	isab	ole	d																	
			Enabled	1						R	Rea	d: Eı	nab	led	ł																	
D	RW	COMPARE1								٧	Vrit	te '1	' to	Di	sabl	e e	ven	t ro	utii	ng f	or C	OM	PAF	RE[1	.] ev	ent	t					
										S	ee	EVE	NTS	s_c	СОМ	1PA	RE[:	1]														
			Clear	1						C	Disa	ble																				
			Disabled	0						R	Rea	d: D	isab	ole	d																	
			Enabled	1						R	Rea	d: Eı	nab	led	t																	
E	RW	COMPARE2								٧	Vrit	te '1	' to	Di	sabl	e e	ven	t ro	utii	ng f	or C	OM	PAF	RE[2] ev	ent	t					
										S	ee	EVE	NTS	s_c	СОМ	IPA	RE[2	2]														
			Clear	1							Disa	ble																				
			Disabled	0						R	Rea	d: D	isab	ole	d																	
			Enabled	1						R	Rea	d: Eı	nab	led	ł																	



Bit	numbe	er		31	30	29	28	27	26	25	24	4 2	3 2:	2 2	1 2	0 1	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	F	E	D	С															В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0) (0) (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							D	esc	rip	tio	n																				
F	RW	COMPARE3										V	/rite	e '1	l' to	Di	isak	le	eve	nt	rοι	itin	g fo	r C	OM	PAI	RE[3	8] e	ver	it						
												S	ee E	VE	NT.	s_(coi	ИΡ	ARE	[3]																
			Clear	1								D	isak	ole																						
			Disabled	0								R	ead	l: D	isal	ble	d																			
			Enabled	1								R	ead	l: Ei	nab	lec	t																			

25.10.6 COUNTER

Address offset: 0x504

Current COUNTER value

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	R	COUNTER		Counter value

25.10.7 PRESCALER

Address offset: 0x508

12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is stopped

Bit	numbe	r		31	30	29	28	3 27	26	25	24	23 :	22 2	21 2	20 2	L9 1	18 1	17 1	16 :	15 1	l4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																							Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Δ	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue	:						Des	crip	tio	n																		
Α	RW	PRESCALER										Pre	cal	er v	/alu	e																	

25.10.8 CC[0]

Address offset: 0x540 Compare register 0

Bit r	numbe	r		31	. 30	29	28	27	26	25	24 :	23 :	22	21	20	19	18	17	16	15 :	14 :	13 1	12 1	11 1	LO !	9	8	7	6	5	4	3 2	! 1	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	Α.	Α,	Α	Α.	Α	Α	Α	Α	A A		A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	alue	:					ı	Des	cri	ptic	n																			
Α	RW	COMPARE									(Con	npa	re '	valı	ue																		

25.10.9 CC[1]

Address offset: 0x544 Compare register 1

Bit r	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scri	iptio	on																			
Α	RW	COMPARE										Coi	mp	are	val	ue																		

25.10.10 CC[2]

Address offset: 0x548 Compare register 2



Bit n	umbe	r		31	1 30	29	2	8 2	7 26	5 25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α,	А А
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alu	2						De	scri	ptic	on																			
Α	RW	COMPARE										Со	mp	are	val	ue																		

25.10.11 CC[3]

Address offset: 0x54C Compare register 3

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	on																			
Α	RW	COMPARE										Cor	npa	are	val	ue																		

25.11 Electrical Specification

25.11.1 RTC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
Into	Run current Real Time Counter (LECLK source)		0.1		пΑ



26 RNG — Random number generator

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

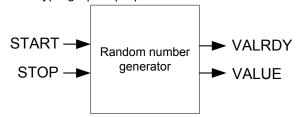


Figure 57: Random number generator

The RNG is started by triggering the START task and stopped by triggering the STOP task. When started, new random numbers are generated continuously and written to the VALUE register when ready. A VALRDY event is generated for every new random number that is written to the VALUE register. This means that after a VALRDY event is generated the CPU has the time until the next VALRDY event to read out the random number from the VALUE register before it is overwritten by a new random number.

26.1 Bias correction

A bias correction algorithm is employed on the internal bit stream to remove any bias toward '1' or '0'. The bits are then queued into an eight-bit register for parallel readout from the VALUE register.

It is possible to enable bias correction in the CONFIG register. This will result in slower value generation, but will ensure a statistically uniform distribution of the random values.

26.2 Speed

The time needed to generate one random byte of data is unpredictable, and may vary from one byte to the next. This is especially true when bias correction is enabled.

26.3 Registers

Table 45: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000D000	RNG	RNG	Random Number Generator	

Table 46: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the random number generator
TASKS_STOP	0x004	Task stopping the random number generator
EVENTS_VALRDY	0x100	Event being generated for every new random number written to the VALUE register
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG	0x504	Configuration register
VALUE	0x508	Output random number

26.3.1 SHORTS

Address offset: 0x200



Shortcut register

Bi	numb	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	9 8	. 7	' 6	5	4	3	2	1	0
Id																																		Α
Re	set 0x	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							De	scr	ipti	on																			
Α	RW	VALRDY_STOP										Sh	ort	cut	bet	wee	en V	/AL	RD۱	ev /	ent	an	d S1	OP	tasl	(
												Se	e <i>E</i> '	VEN	ITS_	_VA	LRE	γ a	nd	TAS	KS_	ST	ЭP											
			Disabled	0								Dis	ab	le sl	hor	tcut																		
			Enabled	1								En	abl	e sh	ort	cut																		

26.3.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	r		31	1 30	29	2	8 2	7 2	26	25	24	23	22	21	. 20	19	9 1	8 1	.7 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	C) (0	0	0	0	0	0	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•							De	scr	ipt	ion																					
Α	RW	VALRDY											W	rite	'1'	to	Ena	abl	e ir	iter	ru	pt f	or	VA	LRD	Y e	ven	t									
													Se	e <i>E</i>	VEI	VTS	_ <i>V</i>	ALF	RDY	/																	
			Set	1									En	abl	e																						
			Disabled	0									Re	ad:	Dis	sab	led																				
			Enabled	1									Re	ad:	En	abl	ed																				

26.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Dit.		_		21	20	20	20	27	, 20	25	. 24	22		21	20	11	10	2 1.	7 1	C 1	г 1	1 1	2 .	12	11	10	0	0	7	_	_	4	2	2	1	0
BIL	numbe	?r		31	. 30	29	28	27	26	25	24	- 23	22	21	. 20) 15	9 TS	5 I.	/ 1	ЬΙ	5 1	4 1	. ð .	12	11	10	9	8	/	ь	5	4	3	2	1	U
Id																																				Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () () ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	escr	ipti	ion																					
Α	RW	VALRDY										W	rite	'1'	to	Dis	abl	e in	nter	rup	ot f	or \	/AL	.RD	Y e	ver	it									
												Se	e <i>E</i>	VEN	VTS	_ <i>V</i>	4 <i>LR</i>	DΥ																		
			Clear	1								Di	sab	le																						
			Disabled	0								Re	ad:	Dis	sab	led																				
			Enabled	1								Re	ad:	En	abl	ed																				

26.3.4 CONFIG

Address offset: 0x504 Configuration register

Bit number				31 30	29	28	27 2	26 2	25 24	1 23	22	21 2	20 19	9 18	3 17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																													Α	
Reset 0x00000000			0 0	0	0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	
Id	RW	Field	Value Id	Value					De	Description																				
Α	RW	DERCEN								Bias correction																				
			Disabled	0				Di	Disabled																					
			Enabled	1				En	Enabled																					

26.3.5 VALUE

Address offset: 0x508 Output random number



Bit number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A R VALUE		[0. 255]	Generated random number

26.4 Electrical Specification

26.4.1 RNG Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{RNG}	Run current, CPU sleeping.		500		μΑ
t _{RNG,START}	Time from setting the START task to generation begins. This is		128		μs
	a one-time delay on START signal and does not apply between				
	samples.				
t _{RNG,RAW}	Run time per byte without bias correction. Uniform distribution		30		μs
	of 0 and 1 is not guaranteed.				
t _{RNG,BC}	Run time per byte with bias correction. Uniform distribution		120		μs
	of 0 and 1 is guaranteed. Time to generate a byte cannot be				
	guaranteed.				



27 TEMP — Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- Temperature range is greater than or equal to operating temperature of the device
- · Resolution is 0.25 degrees

TEMP is started by triggering the START task.

When the temperature measurement is completed, a DATARDY event will be generated and the result of the measurement can be read from the TEMP register.

To achieve the measurement accuracy stated in the electrical specification, the crystal oscillator must be selected as the HFCLK source, see *CLOCK* — *Clock control* on page 98 for more information.

When the temperature measurement is completed, TEMP analog electronics power down to save power.

TEMP only supports one-shot operation, meaning that every TEMP measurement has to be explicitly started using the START task.

27.1 Registers

Table 47: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000C000	TEMP	TEMP	Temperature Sensor	

Table 48: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start temperature measurement
TASKS_STOP	0x004	Stop temperature measurement
EVENTS_DATARDY	0x100	Temperature measurement complete, data ready
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
TEMP	0x508	Temperature in °C (0.25° steps)
A0	0x520	Slope of 1st piece wise linear function
A1	0x524	Slope of 2nd piece wise linear function
A2	0x528	Slope of 3rd piece wise linear function
A3	0x52C	Slope of 4th piece wise linear function
A4	0x530	Slope of 5th piece wise linear function
A5	0x534	Slope of 6th piece wise linear function
B0	0x540	y-intercept of 1st piece wise linear function
B1	0x544	y-intercept of 2nd piece wise linear function
B2	0x548	y-intercept of 3rd piece wise linear function
В3	0x54C	y-intercept of 4th piece wise linear function
B4	0x550	y-intercept of 5th piece wise linear function
B5	0x554	y-intercept of 6th piece wise linear function
<i>TO</i>	0x560	End point of 1st piece wise linear function
T1	0x564	End point of 2nd piece wise linear function
T2	0x568	End point of 3rd piece wise linear function
<i>T3</i>	0x56C	End point of 4th piece wise linear function
T4	0x570	End point of 5th piece wise linear function



27.1.1 INTENSET

Address offset: 0x304

Enable interrupt

Bitı	numbe	er		31	1 30	29	2	8 2	7 2	26 :	25	24	23	22	21	20	19	18	3 1	7 1	6 1	L5 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	(0)	0	0	0	0	0	0	0	0	0	C) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	:							Des	scri	ipti	on																					
Α	RW	DATARDY											Wr	ite	'1'	to I	Ena	ble	in	ter	rup	ot f	or (DA ⁻	ΓAR	DY	eve	ent									Γ
													See	ε Ε \	/EΝ	ITS_	_D/	4 <i>T</i> /	RE	ΟY																	
			Set	1									Ena	able	е																						
			Disabled	0									Rea	ad:	Dis	abl	ed																				
			Enabled	1									Rea	ad:	Ena	able	ed																				

27.1.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		31	30	29	28	3 27	26	25	24	23	3 22	2 2	1 2	0 1	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	C) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							D	esc	ript	tio	ı																			
Α	RW	DATARDY										W	/rite	e '1	' to	Di	sab	le	int	erri	ıpt	for	DΑ	TΑ	RDY	ev ev	ent								
												Se	ee E	VE	NT.	S_ <i>L</i>	DA1	AF	DY																
			Clear	1								Di	isak	ole																					
			Disabled	0								Re	ead	: D	isal	ole	d																		
			Enabled	1								Re	ead	: Er	nab	lec	t																		

27.1.3 TEMP

Address offset: 0x508

Temperature in °C (0.25° steps)

Bit	numbe	er		31	30	29	28	27	26 2	:5 2	4 23	22	21	20	19	18	17 :	16	15 1	14 1	3 12	11	10	9	8	7 6	5 5	5 4	3	2	1	0
Id				Α	Α	Α	Α	Α	A	4 Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α	Α	Α	A	4 Α	A A	A A	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 () (0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	on																		
Α	R	TEMP									Te	mpe	erat	ure	in '	°C (0.25	5° s	tep:	s)												Τ
																				eme teps		Die '	tem	per	atur	e in	°C,	. 2's				
											De	cisio	on p	ooir	nt: C)AT	ARE	ΟY														

27.1.4 A0

Address offset: 0x520

Slope of 1st piece wise linear function

Bit number		31 30 29 28 27 20	5 25 24 23 22 21 20 19 18 17 16 15 :	14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				A A A A A A A A A A A A A A A A A A A
Reset 0x00000320		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 0 0 1 0 0 0 0
Id RW Field	Value Id	Value	Description	
A RW A0			Slope of 1st piece wise linear	function

27.1.5 A1

Address offset: 0x524



Slope of 2nd piece wise linear function

Е	Bit nui	mbe	r		31	. 30	29	28	27 2	26	25	24	23	22 2	21 2	20 1	.9 1	18 1	.7 1	16 1	15 :	14	13	12 1	1 1) 9	8	7	6	5	4	3	2	1	0
10	d																								A A	. 4	. 4	A	Α	Α	Α	Α	Α	Α.	Α
F	Reset	0x0	0000343		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	1	. 1	. 0	1	0	0	0	0	1	1
1	d F	RW	Field	Value Id	Va	lue							Des	crip	tio	n																			
A	\ F	RW	A1										Sloi	oe o	f 2	nd p	iec	e w	ise	line	ear	fur	ncti	on											

27.1.6 A2

Address offset: 0x528

Slope of 3rd piece wise linear function

Bit	numbe	er		31 30 29 28 27	26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12	11 10 9 8	7 6	5	4 3	2 1	0
Id							A A A A	A A	Α	АА	А А	Α
Res	et 0x0	000035D		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 1 1	0 1	0	1 1	1 0	1
Id	RW	Field	Value Id	Value	Description							
Α	RW	A2			Slope of 3rd piec	e wise linear function						

27.1.7 A3

Address offset: 0x52C

Slope of 4th piece wise linear function

Bit	nu	mbe	er		31	30	29	28 2	7 26	5 25	24	23	22	21	20	19	18	17	16	15	14	13 1	12 1	1 1	9	8	7	6	5	4	3	2	1 0
Id																							,	A A	A	Α	Α	Α	Α	Α	Α	Α /	A A
Re	set	0x0	0000400		0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 1	0	0	0	0	0	0	0	0 (0 0
Id	- 1	RW	Field	Value Id	Va	lue						De	scri	pti	on																		
Α		RW	A3									Slo	pe	of 4	lth i	piec	e w	/ise	lin	ear	fun	ctio	n										

27.1.8 A4

Address offset: 0x530

Slope of 5th piece wise linear function

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8	8 7 6 5 4 3 2 1 0
Id				A A A /	A A A A A A A A
Reset 0x0000047F		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 0	0 0 1 1 1 1 1 1 1
ld RW Field	Value Id	Value	Description		

27.1.9 A5

Address offset: 0x534

Slope of 6th piece wise linear function

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A
Reset 0x0000037B		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 1 1 1 1 0 1 1
Id RW Field	Value Id	Value	Description
A RW A5			Slope of 6th piece wise linear function

27.1.10 B0

Address offset: 0x540

y-intercept of 1st piece wise linear function



Bitı	numbe	er		31	30 2	9 2	28 2	27 20	5 25	5 24	23	22	21 :	20 1	19 1	8 1	7 1	6 15	14	13	12	11	10	9	8	7	6	5	4 3	3 2	1	0
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	. A	Α
Res	et 0x0	0003FCC		0	0 ()	0	0 0	0	0	0	0	0	0	0 (0 (0	0	0	1	1	1	1	1	1	1	1	0	0 1	l 1	0	0
Id	RW	Field	Value Id	Va	ue						De	scri	ptio	n																		
Α	RW	В0									y-i	nter	сер	t of	1st	pie	ce v	vise	line	ar f	unc	tior	1									

27.1.11 B1

Address offset: 0x544

y-intercept of 2nd piece wise linear function

Bit number	•		31	30 2	9 2	8 27	26	25	24 2	23 2	2 21	20	19 3	18 1	7 10	5 15	14	13	12 1	.1 10	9	8	7	6	5	4	3 2	2 1	0
Id																		Α	Α.	ДД	Α	Α	Α	Α	Α	Α	ΑА	A	Α
Reset 0x00	0003F98		0	0 (0 (0 0	0	0	0	0 0	0	0	0	0	0 0	0	0	1	1	1 1	1	1	1	0	0	1	1 0	0	0
ld RW	Field \	Value Id	Val	lue						Desc	ripti	on																	
A RW	B1								У	-int	erce	pt o	f 2n	d pi	ece	wise	line	ear i	unc	tion									

27.1.12 B2

Address offset: 0x548

y-intercept of 3rd piece wise linear function

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id	A A A A A A A A A A A A A A A A A A A	АА
Reset 0x00003F98	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 0 0 1 1 0	0 0
Id RW Field Value Id	Value Description	
A RW B2	y-intercept of 3rd piece wise linear function	

27.1.13 B3

Address offset: 0x54C

y-intercept of 4th piece wise linear function

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id																						Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ ,	А А
Rese	t 0x0	0000012		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0 (0 :	1 0
Id	RW	Field	Value Id	Va	lue	;						De	scri	otic	n																			
Α	RW	В3										y-ir	nter	сер	t of	f 4t	h p	iece	e wi	ise l	ine	ar f	un	ctio	n									

27.1.14 B4

Address offset: 0x550

y-intercept of 5th piece wise linear function

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id				AAAAA	. A A A A A A A A
Reset 0x0000006A		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 1 1 0 1 0 1 0
ld RW Field	Value Id	Value	Description		
A RW B4			y-intercept of 5th pie	ece wise linear function	

27.1.15 B5

Address offset: 0x554

y-intercept of 6th piece wise linear function

Bit	numb	er			31 30 29 28 27	26 25	24	23 2	2 21	20	19 1	l8 1	7 16	5 15	14	13	12	11	10 !	9	8 7	7 6	5	4	3	2	1 0
Id																Α	Α	Α	A	Δ.	Δ ,	Α Α	A	Α	Α	Α	АА
Res	et 0x	000030	D0		0 0 0 0 0	0 0	0	0 (0	0	0	0 0	0	0	0	1	1	1	1	0	1 1	L 1	. 0	1	0	0	0 0
Id	RW	/ Field		Value Id	Value			Desc	ripti	on																	

RW B5 y-intercept of 6th piece wise linear function



27.1.16 TO

Address offset: 0x560

End point of 1st piece wise linear function

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 1	.8 17 16 15 14 13 12	2 11 10 9 8	7 6	5	4 3	2 1	. 0
Id						A A	Α	А А	A A	A
Reset 0x00000	E2	0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0	1 1	1	0 0	0 1	. 0
Id RW Field	Value Id	Value	Description							
A RW TO			End point of 1st p	iece wise linear func	tion					

27.1.17 T1

Address offset: 0x564

End point of 2nd piece wise linear function

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1
Id					A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0000000
ld RW Field	Value Id	Value	Description		
A RW T1			End point of 2nd pied	ce wise linear function	

27.1.18 T2

Address offset: 0x568

End point of 3rd piece wise linear function

Bit	numbe	er		31	30 2	9 :	28	27 2	26	25	24	23	22 2	1 2	0 1	9 1	8 17	7 16	15	14	13	12 :	1 1	0 9	8	7	6	5	4	3	2 :	1 0
Id																										Α	Α	Α	Α	Α .	Δ ,	А А
Res	et 0x0	0000014		0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0 0	0	0	0	0	0	1	0	1 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	T2										End	poi	nt d	of 3	rd p	iece	e wi	se li	nea	r fu	ncti	on									

27.1.19 T3

Address offset: 0x56C

End point of 4th piece wise linear function

Bit	t nu	ımbe	er		31	30 2	9 2	28 2	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																												Α	Α	Α	Α	Α	Α	А А
Re	set	0x0	0000019		0	0 ()	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0 1
Id		RW	Field	Value Id	Val	ue						De	scri	ptic	on																			
Α		RW	T3									En	d po	oint	of	4th	pie	ece	wis	e lii	nea	r fu	nct	ion										

27.1.20 T4

Address offset: 0x570

End point of 5th piece wise linear function

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000050		0 0 0 0 0	0000000000	000000000	0 0 1 0 1 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW T4			End point of 5th piece	e wise linear function	

End point of 5th piece wise linear function



27.2 Electrical Specification

27.2.1 Temperature Sensor Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{TEMP}	Time required for temperature measurement		36		μs
T _{TEMP,RANGE}	Temperature sensor range	-40		85	°C
T _{TEMP,ACC}	Temperature sensor accuracy	-5		5	°C
T _{TEMP,RES}	Temperature sensor resolution		0.25		°C
T _{TEMP,STB}	Sample to sample stability at constant device temperature		+/-0.25		°C
T _{TEMP,OFFST}	Sample offset at 25°C	-2.5		2.5	°C



28 ECB — AES electronic codebook mode encryption

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128 bit AES encryption (encryption only, not decryption).

AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks and is an asynchronous operation which may not complete if the AES core is busy.

AES ECB features:

- 128 bit AES encryption
- · Supports standard AES ECB block encryption
- Memory pointer support
- DMA data transfer

AES ECB performs a 128 bit AES block encrypt. At the STARTECB task, data and key is loaded into the algorithm by EasyDMA. When output data has been written back to memory, the ENDECB event is triggered.

AES ECB can be stopped by triggering the STOPECB task.

28.1 Shared resources

The ECB, CCM, and AAR share the same AES module. The ECB will always have lowest priority and if there is a sharing conflict during encryption, the ECB operation will be aborted and an ERRORECB event will be generated.

28.2 EasyDMA

The ECB implements an EasyDMA mechanism for reading and writing to the Data RAM. This DMA cannot access the program memory or any other parts of the memory area except RAM.

If the ECBDATAPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The EasyDMA will have finished accessing the Data RAM when the ENDECB or ERRORECB is generated.

28.3 ECB data structure

Input to the block encrypt and output from the block encrypt are stored in the same data structure. ECBDATAPTR should point to this data structure before STARTECB is initiated.

Table 49: ECB data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
CLEARTEXT	16	16 byte AES cleartext input block
CIPHERTEXT	32	16 byte AES ciphertext output block

28.4 Registers

Table 50: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x4000E000	ECB	ECB	AES ECB Mode Encryption		



Table 51: Register Overview

Register	Offset	Description
TASKS_STARTECB	0x000	Start ECB block encrypt
TASKS_STOPECB	0x004	Abort a possible executing ECB operation
EVENTS_ENDECB	0x100	ECB block encrypt complete
EVENTS_ERRORECB	0x104	ECB block encrypt aborted because of a STOPECB task or due to an error
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ECBDATAPTR	0x504	ECB block encrypt memory pointers

28.4.1 INTENSET

Address offset: 0x304

Enable interrupt

<u> </u>			
Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			В А
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW ENDECB			Write '1' to Enable interrupt for ENDECB event
			See EVENTS_ENDECB
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW ERRORECB			Write '1' to Enable interrupt for ERRORECB event
			See EVENTS_ERRORECB
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

28.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		31	1 30	29	28 2	27 2	26 2	5 2	24 2	3 22	21	20	19	18	17	16	15	14 1	13	12 1	1 1	.0 9) 8	3 7	6	5	4	3 2	1	. 0
Id																															В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0 (0 0	0	0	0	0	0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue						D	escr	iptic	n																		
Α	RW	ENDECB									٧	Vrite	'1' t	o D	isak	ole	inte	rru	pt 1	for I	ENE	DECE	3 ev	ent								
											S	ee <i>E</i> '	/EN	TS_	ENE	DEC	B															
			Clear	1							D	isab	e																			
			Disabled	0							R	ead:	Disa	ble	d																	
			Enabled	1							R	ead:	Ena	ble	d																	
В	RW	ERRORECB									٧	Vrite	'1' t	o D	isak	ole	inte	rru	pt i	for I	ERR	ORE	СВ	eve	nt							
											S	ee <i>E</i>	/EN	TS_	ERR	OR	ECE	3														
			Clear	1							D	isab	e																			
			Disabled	0							R	ead:	Disa	ble	d																	
			Enabled	1							R	ead:	Ena	ble	d																	

28.4.3 ECBDATAPTR

Address offset: 0x504

ECB block encrypt memory pointers



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	13 :	12 :	11 :	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۸ ۸	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	ECBDATAPTR										Poi	nte	r to	th	e EC	СВс	lata	str	uct	ure	(se	e T	abl	e 1	ECE	3 da	ata						

structure overview)

28.5 Electrical Specification

28.5.1 ECB Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{ECB}	Run time per 16 byte block in all modes		6		μs



29 CCM — AES CCM mode encryption

Cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication. The CCM terminology "Message authentication code (MAC)" is called the "Message integrity check (MIC)" in 'Bluetooth' terminology and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the Radio. All operations can complete within the packet RX or TX time. CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF *RFC3610*, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in *NIST Special Publication 800-38C*. The *Bluetooth* specification describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

The AES CCM supports three operations: key-stream generation, packet encryption, and packet decryption. All these operations are done in compliance with the *Bluetooth* specification. ²²A new key-stream must be generated before a new packet encryption or packet decryption operation can be started.

A key-stream is generated by triggering the KSGEN task. An ENDKSGEN event will be generated when the new key-stream has been generated. The key-stream will be stored in the AES CCM's temporary memory area, specified by the SCRATCHPTR, where it will be used in subsequent encryption and decryption operations.

Encryption is started by triggering the CRYPT task with the MODE register set to ENCRYPTION. Similarly, decryption is started by triggering the same task with MODE set to DECRYPTION. An ENDCRYPT event will be generated when packet encryption is completed as well as when packet decryption is completed, see *Figure 58: Key-stream generation followed by encryption or decryption. The shortcut is optional.* on page 263.

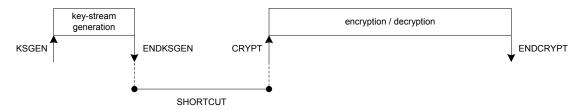


Figure 58: Key-stream generation followed by encryption or decryption. The shortcut is optional.

Key-stream generation, packet encryption, and packet decryption operations utilize the configuration specified in the data structure pointed to by the CNFPTR pointer. It is necessary to configure this pointer and its underlying data structure, and the MODE register before the KSGEN task is triggered. It is also necessary to configure the INPTR pointer and the OUTPTR pointer before the CRYPT task is triggered.

If a shortcut is used between ENDKSGEN event and CRYPT task, the INPTR pointer and the OUTPTR pointer must be configured before the KSGEN task is triggered.

The AES CCM supports different packet lengths, this is configured via the PACKETLENGTH field in the MODE register.

Bluetooth AES CCM 128 bit block encryption, see Bluetooth Core specification Version 4.0.



29.1 Shared resources

The CCM shares registers and other resources with other peripherals that have the same ID as the CCM. The user must therefore disable all peripherals that have the same ID as the CCM before the CCM can be configured and used.

Disabling a peripheral that have the same ID as the CCM will not reset any of the registers that are shared with the CCM. It is therefore important to configure all relevant CCM registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

29.2 Encryption

During packet encryption, the AES CCM will read the unencrypted packet located in RAM at the address specified in the INPTR pointer, encrypt the packet and append a four byte long Message Integrity Check (MIC) field to the packet.

The AES CCM will also modify the length field of the packet to adjust for the appended MIC field, that is, add four bytes to the length, and store the resulting packet back into RAM at the address specified in the OUTPTR pointer, see *Figure 59: Encryption* on page 264.

Empty packets (length field is set to 0) will not be encrypted but instead moved unmodified through the AES CCM.

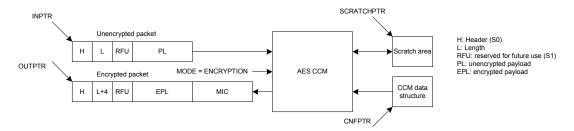


Figure 59: Encryption

29.3 Decryption

During packet decryption, the AES CCM will read the encrypted packet located in RAM at the address specified in the INPTR pointer, decrypt the packet, authenticate the packet's MIC field and generate the appropriate MIC status.

The AES CCM will also modify the length field of the packet to adjust for the MIC field, that is, subtract four bytes from the length, and then store the decrypted packet into RAM at the address pointed to by the OUTPTR pointer, see *Figure 60: Decryption* on page 265.

The CCM is only able to decrypt packets that are at least 5 bytes long, that is, 1 byte or more encrypted payload (EPL) and 4 bytes of MIC. The CCM will therefore generate a MIC error for packets where the length field is set to 1, 2, 3 or 4.

Empty packets (length field is set to 0) will not be decrypted but instead moved unmodified through the AES CCM, these packets will always pass the MIC check.



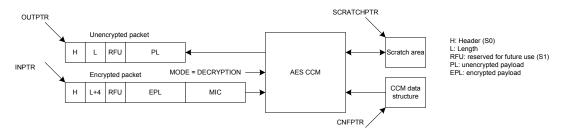


Figure 60: Decryption

29.4 AES CCM and RADIO concurrent operation

The AES CCM is designed to run in parallel with the RADIO to enable on-the-fly encryption and decryption of RADIO packets without CPU involvement. To facilitate this, the RADIO has to be configured with specific settings.

Table 52: Radio configuration settings

Radio parameter	Value	Description
PCNF0.SOLEN	1	Length of HEADER field in: <i>Table 54: Data structure for unencrypted packet</i> on page 267 and <i>Table 55: Data structure for encrypted packet</i> on page 267.
PCNF0.LFLEN	5 or 8	Length of LENGTH field in: <i>Table 54: Data structure for unencrypted packet</i> on page 267 and <i>Table 55: Data structure for encrypted packet</i> on page 267.
PCNF0.S1LEN	3 or 0	Length of the RFU field in: <i>Table 54: Data structure for unencrypted packet</i> on page 267 and <i>Table 55: Data structure for encrypted packet</i> on page 267. The combined length of LENGTH and RFU must always be 8 bit.
PCNF0.S1	Include	Always include the S1 field (RFU field) in RAM to secure that the same data structure can be used for PCNF0.S1LEN = 3 and PCNF0.S1LEN = 0: Table 54: Data structure for unencrypted packet on page 267 and Table 55: Data structure for encrypted packet on page 267.
MODE	Ble_1Mbit	Data rate. Must match CCM->MODE.DATARATE
PCNF1.BALEN	3	Length of address (32 bit)
CRCCNF.LEN	3	Length of CRC (24 bit)

29.5 Encrypting packets on-the-fly in radio transmit mode

When the AES CCM is encrypting a packet on-the-fly at the same time as the RADIO is transmitting it, the RADIO must read the encrypted packet from the same memory location as the AES CCM is writing to.

The OUTPTR pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 61: Configuration of on-the-fly encryption* on page 265.

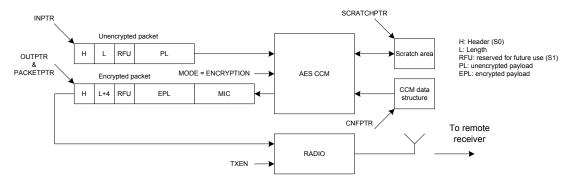


Figure 61: Configuration of on-the-fly encryption

In order to match the RADIO's timing, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered, in addition the shortcut between the ENDKSGEN event and the CRYPT task must be enabled. This use-case is illustrated in *Figure 62: On-the-fly encryption using a PPI connection* on page 266 using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM.



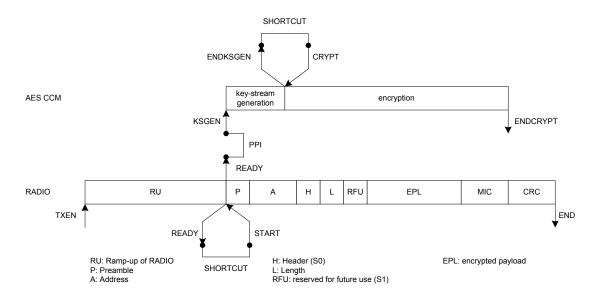


Figure 62: On-the-fly encryption using a PPI connection

29.6 Decrypting packets on-the-fly in radio receive mode

When the AES CCM is decrypting a packet on-the-fly at the same time as the RADIO is receiving it, the AES CCM must read the encrypted packet from the same memory location as the RADIO is writing to.

The INPTR pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 63: Configuration of on-the-fly decryption* on page 266.

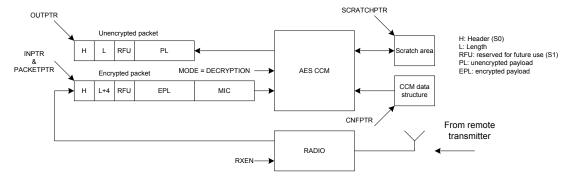


Figure 63: Configuration of on-the-fly decryption

In order to match the RADIO's timing, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition, the CRYPT task must be triggered no earlier than when the ADDRESS event is generated by the RADIO.

If the CRYPT task is triggered exactly at the same time as the ADDRESS event is generated by the RADIO, the AES CCM will guarantee that the decryption is completed no later than when the END event in the RADIO is generated.

This use-case is illustrated in *Figure 64: On-the-fly decryption using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM* on page 267 using a PPI connection between the ADDRESS event in the RADIO and the CRYPT task in the AES CCM. The KSGEN task is triggered from the READY event in the RADIO through a PPI connection.



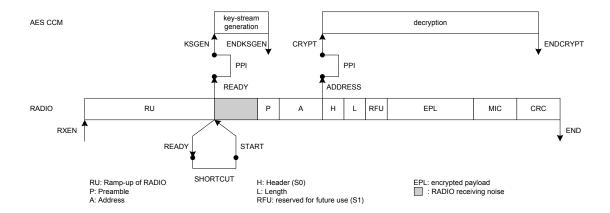


Figure 64: On-the-fly decryption using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM

29.7 CCM data structure

The CCM data structure is located in Data RAM at the memory location specified by the CNFPTR pointer register.

Table 53: CCM data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
PKTCTR	16	Octet0 (LSO) of packet counter
	17	Octet1 of packet counter
	18	Octet2 of packet counter
	19	Octet3 of packet counter
	20	Bit 6 – Bit 0: Octet4 (7 most significant bits of packet counter, with Bit 6 being the most significant
		bit) Bit7: Ignored
	21	Ignored
	22	Ignored
	23	Ignored
	24	Bit 0: Direction bit Bit 7 – Bit 1: Zero padded
IV	25	8 byte initialization vector (IV) Octet0 (LSO) of IV, Octet1 of IV,, Octet7 (MSO) of IV

The NONCE vector (as specified by the *Bluetooth* Core Specification) will be generated by hardware based on the information specified in the CCM data structure from *Table 53: CCM data structure overview* on page 267.

Table 54: Data structure for unencrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in unencrypted payload
RFU	2	Reserved Future Use
PAYLOAD	3	Unencrypted payload

Table 55: Data structure for encrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in encrypted payload including length of MIC
		Important: LENGTH will be 0 for empty packets since the MIC is not added to empty
		packets
RFU	2	Reserved Future Use
PAYLOAD	3	Encrypted payload



Property	Address offset	Description
MIC	3 + payload length	ENCRYPT: 4 bytes encrypted MIC

Important: MIC is not added to empty packets

29.8 EasyDMA and ERROR event

The CCM implements an EasyDMA mechanism for reading and writing to the RAM.

In some scenarios where the CPU and other DMA enabled peripherals are accessing the RAM at the same time, the CCM DMA could experience some bus conflicts which may also result in an error during encryption. If this happens, the ERROR event will be generated.

The EasyDMA will have finished accessing the RAM when the ENDKSGEN and ENDCRYPT events are generated.

If the CNFPTR, SCRATCHPTR, INPTR and the OUTPTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

29.9 Registers

Table 56: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	CCM	CCM	AES CCM Mode Encryption	

Table 57: Register Overview

Register	Offset	Description
TASKS_KSGEN	0x000	Start generation of key-stream. This operation will stop by itself when completed.
TASKS_CRYPT	0x004	Start encryption/decryption. This operation will stop by itself when completed.
TASKS_STOP	0x008	Stop encryption/decryption
EVENTS_ENDKSGEN	0x100	Key-stream generation complete
EVENTS_ENDCRYPT	0x104	Encrypt/decrypt complete
EVENTS_ERROR	0x108	CCM error event
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
MICSTATUS	0x400	MIC check result
ENABLE	0x500	Enable
MODE	0x504	Operation mode
CNFPTR	0x508	Pointer to data structure holding AES key and NONCE vector
INPTR	0x50C	Input pointer
OUTPTR	0x510	Output pointer
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

29.9.1 SHORTS

Address offset: 0x200

Shortcut register

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 1	.6 1	L5 1	.4 1	L3 1	.2 1	11 10	9	8	7	6	5	4	3	2	1 0)
Id																																	A	
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			ı
Α	RW	ENDKSGEN_CRYPT										Sho	ortc	ut b	etv	vee	n El	NDK	SG	EN	eve	nt a	and	CR\	/PT	task								
												See	e EV	'EN	TS_	ENE	KS	GEN	an	nd 7	ASK	(S_(CRY	PT.										
			Disabled	0								Dis	able	e sh	ort	cut																		



Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Enabled	1	Enable shortcut

29.9.2 INTENSET

Address offset: 0x304

Enable interrupt

																									_		_			
Bit nu	umbe	r		31	30	29	28 2	2/2	26 2	5 24	1 23 2	.2 21	L 20	19	18	1/:	16	15	14 :	13 1	2 1:	1 10	9	8	/	6	5 4	4 3	_	1 (
Id																													С	B A
Reset	t 0x0	0000000		0	0	0	0	0	0 0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0 0
Id	RW	Field	Value Id	Va	lue						Desc	ript	ion																	
Α	RW	ENDKSGEN									Writ	e '1'	to E	nab	le i	nte	rru	pt f	or E	NDk	SGI	EN e	ven	t						
											See	EVEI	NTS_	ENL	DKS	GEI	٧													
			Set	1							Enal	ole																		
			Disabled	0							Read	d: Di	sabl	ed																
			Enabled	1							Read	d: En	able	d																
В	RW	ENDCRYPT									Writ	e '1'	to E	nab	le i	nte	rru	pt f	or E	NDC	RYI	PT e	vent	:						
											See	EVEI	NTS_	ENL	DCR	RYPT	г													
			Set	1							Enal	ole																		
			Disabled	0							Read	d: Di	sabl	ed																
			Enabled	1							Read	d: En	able	d																
С	RW	ERROR									Writ	e '1'	to E	nab	le i	nte	rru	pt f	or E	RRC	R e	vent	t							
											See	EVEI	NTS_	ERF	ROR	?														
			Set	1							Enal	ole																		
			Disabled	0							Read	d: Di	sabl	ed																
			Enabled	1							Read	d: En	able	d																

29.9.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit no	umbe	r		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					СВА
Rese	t 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	ENDKSGEN			Write '1' to Disable interrupt for ENDKSGEN event
					See EVENTS_ENDKSGEN
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ENDCRYPT			Write '1' to Disable interrupt for ENDCRYPT event
					See EVENTS_ENDCRYPT
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	ERROR			Write '1' to Disable interrupt for ERROR event
					See EVENTS_ERROR
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled



29.9.4 MICSTATUS

Address offset: 0x400

MIC check result

В	t nu	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																				Α
R	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id		RW	Field	Value Id	Va	lue							De	scr	ipti	on																				
Α	ı	R	MICSTATUS										Th	e re	esul	t of	the	M	C c	hec	k p	erf	orm	ied	dur	ing	the	pr	evi	ous	5					
													de	cry	ptio	n o	per	atic	n																	
				CheckFailed	0								МІ	Сс	hec	k fa	iled																			
				CheckPassed	1								MI	C c	hec	k pa	asse	d																		

29.9.5 **ENABLE**

Address offset: 0x500

Enable

Bit	numl	ber			31 3	0 2	9 2	8 2	7 20	6 25	5 24	1 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																	Δ	А
Res	et 0	x00	000000		0 (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RV	N	Field	Value Id	Valu	e						D	escr	ripti	on																			
Α	RV	Ν	ENABLE									Er	nabl	le o	r dis	abl	e C	СМ																
				Disabled	0							Di	isab	le																				
				Enabled	2							Er	nabl	le																				

29.9.6 MODE

Address offset: 0x504 Operation mode

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		C B
Reset 0x00000001		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value Description
A RW MODE		The mode of operation to be used
	Encryption	0 AES CCM packet encryption mode
	Decryption	1 AES CCM packet decryption mode
B RW DATARATE		Data rate that the CCM shall run in synch with
	1Mbit	0 In synch with 1 Mbit data rate
	2Mbit	1 In synch with 2 Mbit data rate
C RW LENGTH		Packet length configuration
	Default	0 Default length. Effective length of LENGTH field is 5-bit
	Extended	1 Extended length. Effective length of LENGTH field is 8-bit

29.9.7 CNFPTR

Address offset: 0x508

Pointer to data structure holding AES key and NONCE vector

Bit r	num	nbei	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	А А
Res	et 0)x00	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	R۱	W	CNFPTR										Poi	nte	r to	th	e da	ata	stru	ıctı	ıre	hol	ldin	g th	ne A	٩ES	kev	/ an	d tl	ne (CCN	1			

NONCE vector (see Table 1 CCM data structure overview)



29.9.8 INPTR

Address offset: 0x50C

Input pointer

Bit num	ber		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15 :	14	13	12 :	11 1	0	9	8	7	6	5	4	3 2	2 1	1 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	Α	Α.	Α	Α	Α	Α	A A	A A	4 A
Reset 0	x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id R	N Field	Value Id	Va	lue							De	scri	ptic	on																			
A R	W INPTR										Ing	ut i	ooir	nter																			

29.9.9 OUTPTR

Address offset: 0x510

Output pointer

Bit n	um	ber			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	O
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4
Rese	t O	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	כ
ld	RV	V	Field	Value Id	Va	lue							De	scr	iptio	on																				
Α	RV	V	OUTPTR										Οu	ıtnı	ıt po	oint	er																			

29.9.10 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit	numbe	er		31	1 30	29	28	27	26 2	25 2	24 2	3 22	2 21	. 20	19	18	17 1	.6 :	15 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	A	A A	4 A	Α	Α	Α	Α	Α /	Д	A A	A А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue						D	esci	ripti	ion																		
Α	RW	SCRATCHPTR									Р	oint	er t	o a	"scra	atcl	n" da	ata	are	a us	ed f	or t	emp	oor	ary s	sto	rage	e				
											d	urin	g ke	ey-s	trea	m g	gene	rat	ion,	MIC	gei	nera	atio	n aı	nd e	ncr	rypt	ion	1/			
											d	ecry	/ptic	on.																		
											Т	he s	crat	tch a	area	is ı	used	fo	r tei	npo	rary	stc	rag	e o	f dat	ta d	duri	ing				
											k	ey-s	trea	am g	gene	rati	ion a	and	l en	cryp	tion	١.										
											А	spa	ice c	of 4	3 by	tes	mus	t b	e re	serv	ed.											



30 AAR — Accelerated address resolver

Accelerated address resolver is a cryptographic support function for implementing the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core specification* v4.0. "Resolvable private address generation" should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

30.1 Shared resources

The AAR shares registers and other resources with the peripherals that have the same ID as the AAR. The user must therefore disable all peripherals that have the same ID as the AAR before the AAR can be configured and used.

Disabling a peripheral that have the same ID as the AAR will not reset any of the registers that are shared with the AAR. It is therefore important to configure all relevant AAR registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

30.2 EasyDMA

The AAR implements EasyDMA for reading and writing to the RAM. The EasyDMA will have finished accessing the RAM when the END, RESOLVED, and NOTRESOLVED events are generated.

If the IRKPTR, ADDRPTR and the SCRATCHPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

30.3 Resolving a resolvable address

As per Bluetooth specification, a private resolvable address is composed of six bytes.

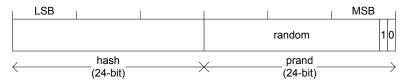


Figure 65: Resolvable address

To resolve an address the ADDRPTR register must point to the start of packet. The resolver is started by triggering the START task. A RESOLVED event is generated when the AAR manages to resolve the address using one of the Identity Resolving Keys (IRK) found in the IRK data structure. The AAR will use the IRK specified in the register IRK0 to IRK15 starting from IRK0. How many to be used is specified by the NIRK register. The AAR module will generate a NOTRESOLVED event if it is not able to resolve the address using the specified list of IRKs.

The AAR will go through the list of available IRKs in the IRK data structure and for each IRK try to resolve the address according to the Resolvable Private Address Resolution Procedure described in the *Bluetooth* Specification²³. The time it takes to resolve an address may vary depending on where in the list the

²³ Bluetooth Specification Version 4.0 [Vol 3] chapter 10.8.2.3.



resolvable address is located. The resolution time will also be affected by RAM accesses performed by other peripherals and the CPU. See the *Electrical specifications* for more information about resolution time.

The AAR will only do a comparison of the received address to those programmed in the module. And not check what type of address it actually is.

The AAR will stop as soon as it has managed to resolve the address, or after trying to resolve the address using NIRK number of IRKs from the IRK data structure. The AAR will generate an END event after it has stopped.

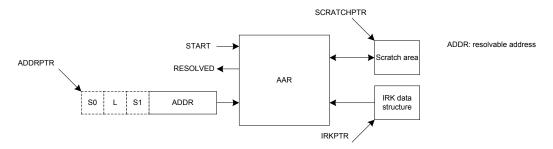


Figure 66: Address resolution with packet preloaded into RAM

30.4 Use case example for chaining RADIO packet reception with address resolution using AAR

The AAR may be started as soon as the 6 bytes required by the AAR have been received by the RADIO and stored in RAM. The ADDRPTR pointer must point to the start of packet.

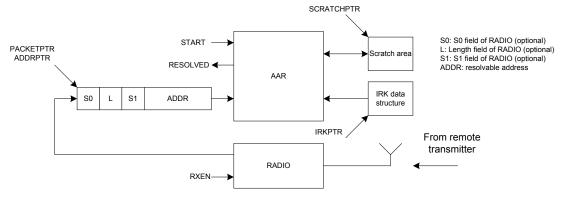


Figure 67: Address resolution with packet loaded into RAM by the RADIO

30.5 IRK data structure

The IRK data structure is located in RAM at the memory location specified by the CNFPTR pointer register.

Table 58: IRK data structure overview

Property	Address offset	Description
IRK0	0	IRK number 0 (16 - byte)
IRK1	16	IRK number 1 (16 - byte)
IRK15	240	IRK number 15 (16 - byte)



30.6 Registers

Table 59: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	AAR	AAR	Accelerated Address Resolver	

Table 60: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start resolving addresses based on IRKs specified in the IRK data structure
TASKS_STOP	0x008	Stop resolving addresses
EVENTS_END	0x100	Address resolution procedure complete
EVENTS_RESOLVED	0x104	Address resolved
EVENTS_NOTRESOLVED	0x108	Address not resolved
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Resolution status
ENABLE	0x500	Enable AAR
NIRK	0x504	Number of IRKs
IRKPTR	0x508	Pointer to IRK data structure
ADDRPTR	0x510	Pointer to the resolvable address
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

30.6.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	er		31	30	29	28 2	27 2	26 25	5 24	4 23 :	22 2	21 2	0 1	9 18	3 17	7 16	5 15	5 14	13	12	11	10	9	8	7 6	5 5	4	3	2	1 0
Id																														С	В А
Res	et 0x0	0000000		0	0	0	0	0	0 0	0	0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Des	crip	otior	1																	
Α	RW	END									Wri	te '	1' to	En	able	int	terr	upt	for	EN	D e	ven	t								
											See	EV	ENT	S_ <i>E</i>	ND																
			Set	1							Ena	ble																			
			Disabled	0							Rea	d: [Disab	oled	ł																
			Enabled	1							Rea	d: E	Enab	led																	
В	RW	RESOLVED									Wri	te '	1' to	En	able	int	terr	upt	for	RE	SOL	VEC	ev	ent							
											See	EV	ENT	S_R	ESO	LVE	ED														
			Set	1							Ena	ble																			
			Disabled	0							Rea	d: [Disab	oled	ł																
			Enabled	1							Rea	d: E	nab	led																	
С	RW	NOTRESOLVED									Wri	te '	1' to	En	able	int	terr	upt	for	NC	TR	ESO	LVE	D e	vent						
											See	EV	ENT	S_Λ	ОТР	RES	OLV	'ED													
			Set	1							Ena	ble																			
			Disabled	0							Rea	d: E	Disab	oled	i																
			Enabled	1							Rea	d: E	Enab	led																	

30.6.2 INTENCLR

Address offset: 0x308 Disable interrupt



																												_				
Bit	numbe	er		31	. 30	29	28	27	26 2	25 2	24 2	3 22	21	20	19 1	18	17 1	16	15	14	13 1	2 1	1 10) 9	8	7	6	5	4 3	_	1	0
Id																														С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0 (0 0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	iptio	on																		
Α	RW	END									۷	Vrite	'1' t	o D	isab	ole i	inte	rru	ıpt 1	for	END	ev	ent									
											S	ee <i>E</i>	VEN	TS_	ENL)																
			Clear	1							D	isab	le																			
			Disabled	0							R	lead:	Disa	able	d																	
			Enabled	1							R	lead:	Ena	ble	d																	
В	RW	RESOLVED									٧	Vrite	'1' t	:o D	isab	ole i	inte	rru	ıpt 1	for	RESC	OLV	ED 6	ever	nt							
											S	ee <i>E</i>	VEN	TS_	RES	OLI	VED	1														
			Clear	1							D	isab	le																			
			Disabled	0							R	lead:	Disa	able	d																	
			Enabled	1							R	lead:	Ena	ble	d																	
С	RW	NOTRESOLVED									۷	Vrite	'1' t	:o D	isab	ole i	inte	rru	ıpt 1	for	NOT	RES	SOL\	/ED	eve	nt						
											S	ee <i>E</i> '	VEN	TS_	NO	TRE	SOL	.VE	D													
			Clear	1							D	isab	le																			
			Disabled	0							R	lead:	Disa	able	d																	
			Enabled	1							R	lead:	Ena	ble	d																	

30.6.3 STATUS

Address offset: 0x400

Resolution status

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААА
Reset 0x00000000		0 0 0 0 0 0	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field	Value Id	Value	Description
A R STATUS		[015]	The IRK that was used last time an address was resolved

30.6.4 ENABLE

Address offset: 0x500

Enable AAR

Bit	numb	er		31 30	29	28 2	27 2	26 2	5 24	1 23	3 22	21	20 1	9 1	8 1	7 1	5 15	14	13	12	11 1	.0 9	9 8	7	6	5	4	3	2 1	. 0
Id																													A	A A
Res	et 0x	0000000		0 0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Value						De	escri	ptic	n																	
Α	RW	ENABLE								En	able	or	disa	ble	AAI	3														
			Disabled	0						Di	sable	е																		
			Enabled	3						En	able	9																		

30.6.5 NIRK

Address offset: 0x504

Number of IRKs

Bit number	31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000001	0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value	Description
A RW NIRK	[116]	Number of Identity root keys available in the IRK data structure

30.6.6 IRKPTR

Address offset: 0x508



Pointer to IRK data structure

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW IRKPTR		Pointer to the IRK data structure

30.6.7 ADDRPTR

Address offset: 0x510

Pointer to the resolvable address

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW ADDRPTR		Pointer to the resolvable address (6-bytes)

30.6.8 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit	numbe	er		31	1 30	29	28	8 27	7 2	6 25	5 24	4 23	22	21	20	19	18 1	L7 1	6 15	5 14	13	12	11 1	0 9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	. A	A	Α Α	A	A	A	Α	Α	Α	Α	Α .	A A	4 A	Α	Α	Α	Α /	Α Α	A	Α	Α	Α	Α	A A	. Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0 () (0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue	:						De	scr	iptio	on																	
Α	RW	SCRATCHPTR										Pc	inte	er to	a "	scr	atch	" da	ita a	rea	use	d fo	r tei	npc	rary	sto	rag	e				
												dι	ring	g res	olu	tior	n.A s	spac	e of	mir	nimu	ım 3	by	es i	nus	t be						
												re	serv	ed.																		

30.7 Electrical Specification

30.7.1 AAR Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{AAR,8}	Time for address resolution of 8 IRKs		48		μs



31 SPIM — Serial peripheral interface master with EasyDMA

The SPI master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus.

Listed here are the main features for the SPIM

- · Three SPIM instances
- SPI mode 0-3
- EasyDMA direct transfer to/from RAM for both SPI Slave and SPI Master
- Individual selection of IO pin for each SPI signal

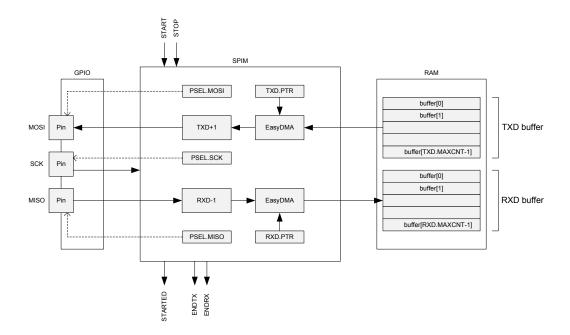


Figure 68: SPIM — SPI master with EasyDMA

The SPIM does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPIM supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 61: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA
SPI_MODI	0 (Leading)	0 (Active High)
SPI_MODE	E 0 (Leading)	1 (Active Low)
SPI_MODI	1 (Trailing)	0 (Active High)
SPI_MODE	1 (Trailing)	1 (Active Low)

31.1 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.



Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

31.2 EasyDMA

The SPI master implements EasyDMA for reading and writing of data packets from and to the DATA RAM without CPU involvement.

The RXD.PTR and TXD.PTR point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively, see *Figure 68: SPIM — SPI master with EasyDMA* on page 277. RXD.MAXCNT and TXD.MAXCNT specify the maximum number of bytes allocated to the buffers.

The SPI master will automatically stop transmitting after TXD.MAXCNT bytes have been transmitted and RXD.MAXCNT bytes have been received. If TXD.MAXCNT is larger than RXD.MAXCNT, the superfluous received bytes will be ignored. If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register.

If the RXD.PTR and the TXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next transmission immediately after having received the STARTED event.

The ENDRX/ENDTX event indicate that EasyDMA has finished accessing respectively the RX/TX buffer in RAM. The END event gets generated when both RX and TX are finished accessing the buffers in RAM.

31.2.1 EasyDMA list

EasyDMA supports one list type.

The supported list type is:

Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type.

For illustration, see the code example below. This data structure includes only a buffer with size equal to Channel.MAXCNT. EasyDMA will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.

The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
  uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type MyArrayList[3];
```



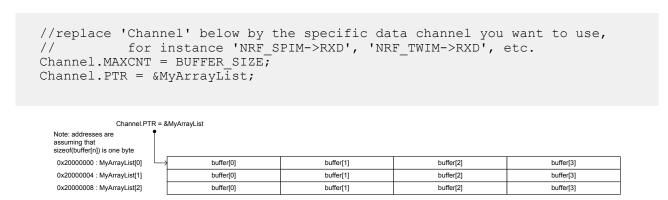


Figure 69: EasyDMA array list

31.3 SPI master transaction sequence

An SPI master transaction consists of a sequence started by the START task followed by a number of events, and finally the STOP task.

An SPI master transaction is started by triggering the START task. The ENDTX event will be generated when the transmitter has transmitted all bytes in the TXD buffer as specified in the TXD.MAXCNT register. The ENDRX event will be generated when the receiver has filled the RXD buffer, i.e. received the last possible byte as specified in the RXD.MAXCNT register.

Following a START task, the SPI master will generate an END event when both ENDRX and ENDTX have been generated.

The SPI master is stopped by triggering the STOP task. A STOPPED event is generated when the SPI master has stopped.

If the ENDRX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDRX event explicitly even though the RX buffer is not full.

If the ENDTX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 70: SPI master transaction* on page 280.



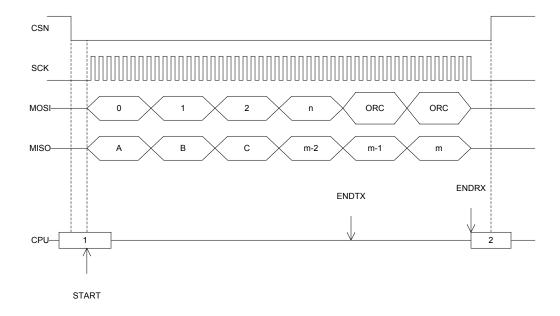


Figure 70: SPI master transaction

31.4 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

31.5 Master mode pin configuration

The SCK, MOSI, and MISO signals associated with the SPI master are mapped to physical pins according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively.

The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 62: GPIO configuration* on page 280 prior to enabling the SPI. The SCK must always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 62: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value	Comments
SCK	As specified in PSEL.SCK	Output	Same as CONFIG.CPOL	
MOSI	As specified in PSEL.MOSI	Output	0	
MISO	As specified in PSEL.MISO	Input	Not applicable	



31.6 Registers

Table 63: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPIM	SPIM0	SPI master 0		
0x40004000	SPIM	SPIM1	SPI master 1		
0x40023000	SPIM	SPIM2	SPI master 2.		

Table 64: Register Overview

Register	Offset	Description
TASKS_START	0x010	Start SPI transaction
TASKS_STOP	0x014	Stop SPI transaction
TASKS_SUSPEND	0x01C	Suspend SPI transaction
TASKS_RESUME	0x020	Resume SPI transaction
EVENTS_STOPPED	0x104	SPI transaction has stopped
EVENTS_ENDRX	0x110	End of RXD buffer reached
EVENTS_END	0x118	End of RXD buffer and TXD buffer reached
EVENTS_ENDTX	0x120	End of TXD buffer reached
EVENTS_STARTED	0x14C	Transaction started
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPIM
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI signal
PSEL.MISO	0x510	Pin select for MISO signal
FREQUENCY	0x524	SPI frequency
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
CONFIG	0x554	Configuration register
ORC	0x5C0	Over-read character. Character clocked out in case and over-read of the TXD buffer.

31.6.1 SHORTS

Address offset: 0x200 Shortcut register

	Bit n	umbe	r		31	. 30	29	28	3 27	26	25	5 24	1 23	22	2 21	. 20	0 1	9 1	8 :	17	16	15	5 1	4 1	.3	12	11	10	9	8	7	6	5	4	3	2	1	0
	ld																			Α																		
	Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	C)	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	ld	RW	Field	Value Id	Va	lue							De	esc	ript	ion	ı																					
Ī	A	RW	END_START										Sh	ort	tcut	be	twe	eer	ı El	ND	ev	/en	t a	nd	ST	AR'	Гtа	sk										
													Se	e E	VEI	VTS	_ <i>E</i>	ND	ar	nd :	TAS	SKS	_s	TΑ	RT													
				Disabled	0								Di	sak	ole s	ho	rtcı	ut																				
				Enabled	1								En	ab	le s	nor	tcu	t																				

31.6.2 INTENSET

Address offset: 0x304 Enable interrupt



Bit num	ber		31 30	29 28	3 27 :	26 2	5 24	23	22 21	20	19 1	.8 17	7 16	15	14	13	12 1	1 10	9	8	7	6	5 4	4 3	2	1	0
Id											Е									D		С	E	3		Α	
Reset 0	<00000000		0 0	0 0	0	0 0	0	0	0 0	0	0	0 0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0
Id RV	V Field	Value Id	Value					De	escripti	on																	
A RV	V STOPPED							W	rite '1'	to E	nabl	e int	terr	upt	for :	STO	PPE	D ev	ent								
								Se	e <i>EVEN</i>	ITS_	STO	PPEL)														
		Set	1					En	able																		
		Disabled	0					Re	ad: Dis	able	ed																
		Enabled	1					Re	ad: Ena	able	d																
B RV	V ENDRX							W	rite '1'	to E	nabl	e int	terr	upt	for	END	ORX 6	even	t								
								Se	e <i>EVEN</i>	ITS_	END	RX															
		Set	1					En	able																		
		Disabled	0					Re	ad: Dis	able	ed																
		Enabled	1					Re	ad: Ena	able	d																
C RV	V END							W	rite '1'	to E	nabl	e int	terr	upt	for	ENC	eve	nt									
								Se	e <i>EVEN</i>	ITS_	END																
		Set	1					En	able																		
		Disabled	0					Re	ad: Dis	able	ed																
		Enabled	1					Re	ad: Ena	able	d																
D RV	V ENDTX							W	rite '1'	to E	nabl	e int	terr	upt	for	END	OTX 6	even	t								
								Se	e <i>EVEN</i>	ITS_	END	TX															
		Set	1					En	able																		
		Disabled	0					Re	ad: Dis	able	ed																
		Enabled	1					Re	ad: Ena	able	d																
E RV	V STARTED							W	rite '1'	to E	nabl	e int	terr	upt	for :	STA	RTE) ev	ent								
								Se	e <i>EVEN</i>	ITS_	STA	RTEL)														
		Set	1					En	able																		
		Disabled	0					Re	ad: Dis	able	ed																
		Enabled	1					Re	ad: Ena	able	d																

31.6.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id		E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW STOPPED		Write '1' to Disable interrupt for STOPPED event
		See EVENTS_STOPPED
	Clear	1 Disable
	Disabled	
	Enabled	1 Read: Enabled
B RW ENDRX		Write '1' to Disable interrupt for ENDRX event
		See EVENTS_ENDRX
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
C RW END		Write '1' to Disable interrupt for END event
		See EVENTS_END
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
D RW ENDTX		Write '1' to Disable interrupt for ENDTX event
		CONFINENCE FAIRTY
		See EVENTS_ENDTX



Bit number		31	30	29 :	28 2	27 :	26 2	25 2	24 2	23 2	2 2	21 2	0 2	19 1	18 1	L7 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id														Ε										D		С		В		Α	
Reset 0x00000000		0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id RW Field	Value Id	Va	lue						0	Desc	rip	tio	n																		
	Clear	1							0	Disal	ble																				
	Disabled	0							F	Reac	l: D	Disa	ble	d																	
	Enabled	1							F	Reac	1: E	nat	oled	b																	
E RW STARTED									٧	Vrit	e '1	1' to) Di	isab	le i	nte	rru	pt f	or S	TAR	TED	eve	nt								
									S	See I	EVE	ENT	S_5	STAI	RTE	D															
	Clear	1								Disal	ble																				
	Disabled	0							F	Reac	d: D	Disa	ble	d																	
	Enabled	1							F	Reac	d: E	nak	oled	d																	

31.6.4 ENABLE

Address offset: 0x500

Enable SPIM

Bit n	umbe	er		31 30	29	28	27	26	25	24	23 :	22 2	21 2	0 1	9 1	.8 1	.7 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																															Д Д	Α.	Α
Rese	t 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value							Des	crip	tio	n																			
Α	RW	ENABLE									Ena	ble	or c	lisa	ble	SP	M																
			Disabled	0							Disa	ble	SPI	M																			
			Enabled	7							Ena	ble	SPI	M																			
			Disabled								Ena Disa	ble able	or o	lisa M	ble	SP	М																

31.6.5 PSEL.SCK

Address offset: 0x508 Pin select for SCK

Bit r	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

31.6.6 PSEL.MOSI

Address offset: 0x50C Pin select for MOSI signal

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

31.6.7 PSEL.MISO

Address offset: 0x510 Pin select for MISO signal



Bit	numbe	er		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

31.6.8 FREQUENCY

Address offset: 0x524

SPI frequency

Bit number		3	1 3	30 2	29 2	28 :	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	. 1	. 0
Id		Α		A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	4 Α	. 4	A A
Reset 0x04000000		0		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id RW Field	Value Id	٧	alı	ıe							De	scri	ptic	n																			
A RW FREQUENCY											SPI	ma	ste	r da	ata	rat	е																
	K125	0:	x0:	200	000	00					125	5 kb	ps																				
	K250	0:	x04	400	000	00					250) kb	ps																				
	K500	0:	x0	800	000	00					500) kb	ps																				
	M1	0:	x1(000	000	00					1 N	Лbр	s																				
	M2	0:	x2(000	000	00					2 N	Лbр	S																				
	M4	0:	x4(000	000	00					4 N	Лbр	s																				
	M8	0:	x8(000	000	00					8 N	Лbр	S																				

31.6.9 RXD.PTR

Address offset: 0x534

Data pointer

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	17 1	16 1	L5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	A A	A	. A	Α	Α	Α	Α	Α	Α	Α	А А	Α	Α
Reset 0x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
ld RW	Field Val	ue Id	Va	lue							Des	cri	ptic	n																		
A RW	PTR										Dat	a p	oin	ter																		

31.6.10 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8	3 7 6 5 4 3	3 2 1 0
Id					A A A A A	AAAA
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	000000000	00000	0 0 0
ld RW Field	Value Id	Value	Description			
A RW MAXCNT			Maximum number of	bytes in receive buffer		

31.6.11 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	00000000	0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A R AMOUNT			Number of bytes trans	sferred in the last transaction	n



31.6.12 RXD.LIST

Address offset: 0x540 EasyDMA list type

Bitı	num	nber			31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 3	17 1	6 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Id																																A	A /	А А
Res	et 0)x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	R۱	W	Field	Value Id	Va	alue	!						De	scri	ptic	n																		
Α	R۱	W	LIST										List	typ	эe																			
				Disabled	0								Dis	able	e Ea	syD	MA	\ lis	t															
				ArrayList	1								Use	e ar	ray	list																		

31.6.13 TXD.PTR

Address offset: 0x544

Data pointer

F	Bit n	um	bei			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 1	14	13 1	12	11 1	0 9) 8	. 7	6	5	4	3	2	1	0
		٠																																		
1	d					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	\ <i>A</i>	۱ A	Α	. A	Α	Α	Α	Α .	А
1	Rese	t O	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	0
ı	ld	RV	N	Field	Value Id	Va	lue							De	scri	ptic	on																			
7	4	RV	٧	PTR										Dat	ta p	oin	ter																			_

31.6.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	7 6	5 4	3 2 1	1 0
Id					АА	АА	A A A	A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0000000000	0 0	0 0	0 0 0	0 (
Id RW Field	Value Id	Value	Description					
A RW MAXCNT			Maximum number of	bytes in transmit buffer				

31.6.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit r	numbe	er		31	30 2	29 2	28 27	7 26	25	24	23 2	22 2	21 2	20 1	9 1	8 1	7 1	5 15	5 14	13	12	11	10	9	8 7	7 6	5 5	5 4	3	2	1	0
Id																									1	A A	Δ Δ	A	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0
Id	RW	Field	Value Id	Val	ue						Des	crip	otio	n																		
Α	R	AMOUNT									Nur	nbe	r of	by	tes 1	trar	nsfe	rred	d in	the	last	tra	nsa	ctio	n							7

31.6.16 TXD.LIST

Address offset: 0x550 EasyDMA list type

Bi	t nı	ımbe	r		31	30	29	28	27	26	25	24	23	3 22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																																	Α.	А А
Re	ese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id		RW	Field	Value Id	Va	lue							De	escri	iptio	on																		
Α		RW	LIST										Lis	st ty	pe																			
				Disabled	0								Di	sabl	e Ea	asyl	OM	A lis	ŧ															
				ArrayList	1								Us	se ai	rray	list																		



31.6.17 CONFIG

Address offset: 0x554 Configuration register

Bit r	numbe	r		31	30 2	9 2	28 2	27 2	26 2	5 2	24 2	23 2	2 2	1 20	19	9 18	8 17	7 16	15	14	13	12	11 :	10	9	8	7	5 5	4	3	2	1 0
Id																															C I	ВА
Res	et 0x0	0000000		0	0	0	0	0	0 0) (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Desc	ript	tion																		
Α	RW	ORDER									E	3it o	rde	r																		
			MsbFirst	0							ſ	Mos	t sig	gnifi	can	ıt bi	it sh	ifte	d o	ut f	rst											
			LsbFirst	1							l	_eas	t sig	gnifi	can	ıt bi	it sh	ifte	d o	ut f	rst											
В	RW	СРНА									9	Seria	ıl cl	ock	(SC	K) p	oha	se														
			Leading	0							9	Sam	ple	on l	eac	ling	g ed	ge c	of cl	ock	, shi	ft s	eria	l da	ita	on t	rail	ing				
											e	edge	:																			
			Trailing	1							9	Sam	ple	on t	rail	ling	ed	ge o	f cl	ock,	shi	ft se	eria	da	ta d	on le	ad	ing				
											e	edge	:																			
С	RW	CPOL									9	Seria	ıl cl	ock	(SC	K) p	oola	rity														
			ActiveHigh	0							A	Activ	e h	igh																		
			ActiveLow	1							A	Activ	e lo	w																		

31.6.18 ORC

Address offset: 0x5C0

Over-read character. Character clocked out in case and over-read of the TXD buffer.

Bitı	numbe	er		31	30	29	28 2	7 26	25	24	23	22 2	21 2	20 1	9 1	8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id																										Α	Α	Α.	Α	A A	. 4	AA
Res	et OxO	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						De	scrip	tio	n																		
A RW ORC									Ov	er-re	ad	cha	rac	ter.	Cha	irac	ter	cloc	ked	ou	t in	cas	e a	nd (ove	r-						
			read of the TXD buffer.																													

31.7 Electrical Specification

31.7.1 SPIM master interface

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIM}	Bit rates for SPIM ²⁴			8 ²⁵	Mbps
I _{SPIM,2Mbps}	Run current for SPIM, 2 Mbps		50		μΑ
I _{SPIM,8Mbps}	Run current for SPIM, 8 Mbps		50		μΑ
I _{SPIM,IDLE}	Idle current for SPIM (STARTed, no CSN activity)		1		μΑ
$t_{SPIM,START,LP}$	Time from START task to transmission started, low power mode		t _{SPIM,STA}	RT,	μs
			+		
			t _{START_H}	FIN	
t _{SPIM,START,CL}	Time from START task to transmission started, constant latency		1		μs
	mode				

31.7.2 Serial Peripheral Interface Master (SPIM) electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIM} ,CSCK,8Mbps	SCK period at 8Mbps		125		ns
t _{SPIM} ,CSCK,4Mbps	SCK period at 4Mbps		250		ns
t _{SPIM} ,CSCK,2Mbps	SCK period at 2Mbps		500		ns

Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.



Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIM,RSCK,LD}	SCK rise time, low drive ^a			t _{RF,25pF}	
t _{SPIM,RSCK,HD}	SCK rise time, high drive ^a			t _{HRF,25pF}	
t _{SPIM,FSCK,LD}	SCK fall time, low drive ^a			t _{RF,25pF}	
t _{SPIM,FSCK,HD}	SCK fall time, high drive ^a			t _{HRF,25pF}	
t _{SPIM,WHSCK}	SCK high time ^a	(0.5*t _{CSC}	κÌ		
		- t _{RSCK}			
t _{SPIM,WLSCK}	SCK low time ^a	(0.5*t _{CSC}	κÌ		
		- t _{FSCK}			
t _{SPIM,SUMI}	MISO to CLK edge setup time	19			ns
t _{SPIM,HMI}	CLK edge to MISO hold time	18			ns
t _{SPIM,VMO}	CLK edge to MOSI valid			59	ns
t _{SPIM,HMO}	MOSI hold time after CLK edge	20			ns

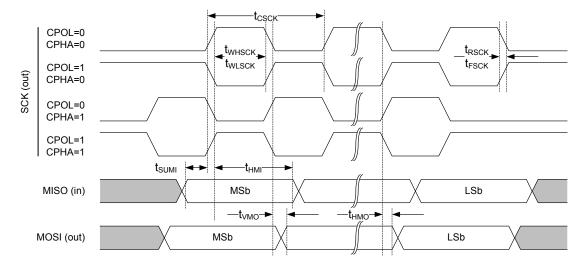


Figure 71: SPIM timing diagram

^a At 25pF load, including GPIO pin capacitance, see GPIO spec.



32 SPIS — Serial peripheral interface slave with EasyDMA

SPI slave (SPIS) is implemented with EasyDMA support for ultra low power serial communication from an external SPI master. EasyDMA in conjunction with hardware-based semaphore mechanisms removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

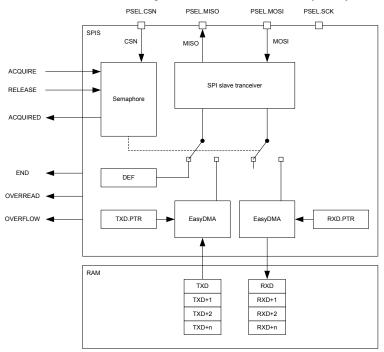


Figure 72: SPI slave

The SPIS supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 65: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA
SPI_MODE0	0 (Leading)	0 (Active High)
SPI_MODE1	0 (Leading)	1 (Active Low)
SPI_MODE2	1 (Trailing)	0 (Active High)
SPI_MODE3	1 (Trailing)	1 (Active Low)

32.1 Shared resources

The SPI slave shares registers and other resources with other peripherals that have the same ID as the SPI slave. Therefore, you must disable all peripherals that have the same ID as the SPI slave before the SPI slave can be configured and used.

Disabling a peripheral that has the same ID as the SPI slave will not reset any of the registers that are shared with the SPI slave. It is important to configure all relevant SPI slave registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 21 shows which peripherals have the same ID as the SPI slave.



32.2 EasyDMA

The SPI slave implements EasyDMA for reading and writing to and from the RAM. The END event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

32.3 SPI slave operation

SPI slave uses two memory pointers, RXD.PTR and TXD.PTR, that point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively. Since these buffers are located in RAM, which can be accessed by both the SPI slave and the CPU, a hardware based semaphore mechanism is implemented to enable safe sharing.

See Figure 73: SPI transaction when shortcut between END and ACQUIRE is enabled on page 290.

Before the CPU can safely update the RXD.PTR and TXD.PTR pointers it must first acquire the SPI semaphore. The CPU can acquire the semaphore by triggering the ACQUIRE task and then receiving the ACQUIRED event. When the CPU has updated the RXD.PTR and TXD.PTR pointers the CPU must release the semaphore before the SPI slave will be able to acquire it. The CPU releases the semaphore by triggering the RELEASE task. This is illustrated in *Figure 73: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 290. Triggering the RELEASE task when the semaphore is not granted to the CPU will have no effect.

The semaphore mechanism does not, at any time, prevent the CPU from performing read or write access to the RXD.PTR register, the TXD.PTR registers, or the RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

The semaphore is by default assigned to the CPU after the SPI slave is enabled. No ACQUIRED event will be generated for this initial semaphore handover. An ACQUIRED event will be generated immediately if the ACQUIRE task is triggered while the semaphore is assigned to the CPU.

The SPI slave will try to acquire the semaphore when CSN goes low. If the SPI slave does not manage to acquire the semaphore at this point, the transaction will be ignored. This means that all incoming data on MOSI will be discarded, and the DEF (default) character will be clocked out on the MISO line throughout the whole transaction. This will also be the case even if the semaphore is released by the CPU during the transaction. In case of a race condition where the CPU and the SPI slave try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in *Figure 73: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 290, the semaphore will be granted to the CPU.

If the SPI slave acquires the semaphore, the transaction will be granted. The incoming data on MOSI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on MISO.

When a granted transaction is completed and CSN goes high, the SPI slave will automatically release the semaphore and generate the END event.

As long as the semaphore is available the SPI slave can be granted multiple transactions one after the other. If the CPU is not able to reconfigure the TXD.PTR and RXD.PTR between granted transactions, the same TX data will be clocked out and the RX buffers will be overwritten. To prevent this from happening, the END_ACQUIRE shortcut can be used. With this shortcut enabled the semaphore will be handed over to the CPU automatically after the granted transaction has completed, giving the CPU the ability to update the TXPTR and RXPTR between every granted transaction.

If the CPU tries to acquire the semaphore while it is assigned to the SPI slave, an immediate handover will not be granted. However, the semaphore will be handed over to the CPU as soon as the SPI slave has released the semaphore after the granted transaction is completed. If the END_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.



The MAXRX register specifies the maximum number of bytes the SPI slave can receive in one granted transaction. If the SPI slave receives more than MAXRX number of bytes, an OVERFLOW will be indicated in the STATUS register and the incoming bytes will be discarded.

The MAXTX parameter specifies the maximum number of bytes the SPI slave can transmit in one granted transaction. If the SPI slave is forced to transmit more than MAXTX number of bytes, an OVERREAD will be indicated in the STATUS register and the ORC character will be clocked out.

The RXD.AMOUNT and TXD.AMOUNT registers are updated when a granted transaction is completed. The TXD.AMOUNT register indicates how many bytes were read from the TX buffer in the last transaction, that is, ORC (over-read) characters are not included in this number. Similarly, the RXD.AMOUNT register indicates how many bytes were written into the RX buffer in the last transaction.

The ENDRX event is generated when the RX buffer has been filled.

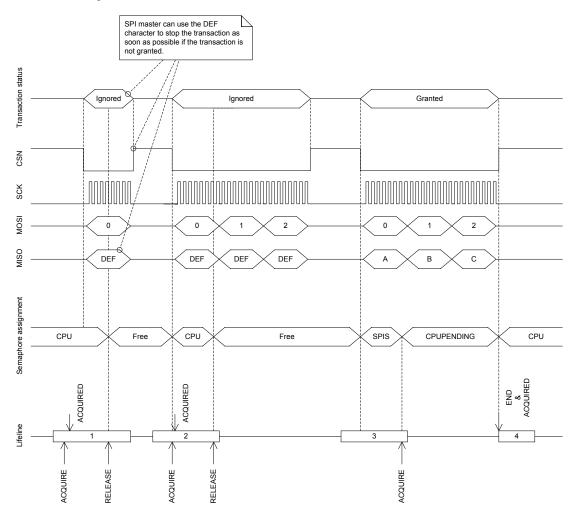


Figure 73: SPI transaction when shortcut between END and ACQUIRE is enabled

32.4 Slave mode pin configuration

The CSN, SCK, MOSI, and MISO signals associated with the SPI slave are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of any of these registers is set to Disconnected, the associated SPI slave signal will not be connected to any physical pins.

The PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI slave is enabled, and retained only as long as the device is in System ON mode, see *POWER* chapter for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n]



register. PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI slave is disabled.

To secure correct behavior in the SPI slave, the pins used by the SPI slave must be configured in the GPIO peripheral as described in *Table 66: GPIO configuration before enabling peripheral* on page 291 before enabling the SPI slave. This is to secure that the pins used by the SPI slave are driven correctly if the SPI slave itself is temporarily disabled, or if the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI slave is to be recognized by an external SPI master.

The MISO line is set in high impedance as long as the SPI slave is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 66: GPIO configuration before enabling peripheral

SPI signal	SPI pin	Direction	Output value	Comment
CSN	As specified in PSEL.CSN	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
MOSI	As specified in PSEL.MOSI	Input	Not applicable	
MISO	As specified in PSEL.MISO	Input	Not applicable	Emulates that the SPI slave is not selected.

32.5 Registers

Table 67: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	SPIS	SPIS0	SPI slave 0.	
0x40004000	SPIS	SPIS1	SPI slave 1	
0x40023000	SPIS	SPIS2	SPI slave 2	

Table 68: Register Overview

Register	Offset	Description	
TASKS_ACQUIRE	0x024	Acquire SPI semaphore	
TASKS_RELEASE	0x028	Release SPI semaphore, enabling the SPI slave to acquire it	
EVENTS_END	0x104	Granted transaction completed	
EVENTS_ENDRX	0x110	End of RXD buffer reached	
EVENTS_ACQUIRED	0x128	Semaphore acquired	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
SEMSTAT	0x400	Semaphore status register	
STATUS	0x440	Status from last transaction	
ENABLE	0x500	Enable SPI slave	
PSELSCK	0x508	Pin select for SCK	Deprecated
PSELMISO	0x50C	Pin select for MISO	Deprecated
PSELMOSI	0x510	Pin select for MOSI	Deprecated
PSELCSN	0x514	Pin select for CSN	Deprecated
PSEL.SCK	0x508	Pin select for SCK	
PSEL.MISO	0x50C	Pin select for MISO signal	
PSEL.MOSI	0x510	Pin select for MOSI signal	
PSEL.CSN	0x514	Pin select for CSN signal	
RXDPTR	0x534	RXD data pointer	Deprecated
MAXRX	0x538	Maximum number of bytes in receive buffer	Deprecated
AMOUNTRX	0x53C	Number of bytes received in last granted transaction	Deprecated
RXD.PTR	0x534	RXD data pointer	
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer	
RXD.AMOUNT	0x53C	Number of bytes received in last granted transaction	
TXDPTR	0x544	TXD data pointer	Deprecated



Register	Offset	Description	
MAXTX	0x548	Maximum number of bytes in transmit buffer	Deprecated
AMOUNTTX	0x54C	Number of bytes transmitted in last granted transaction	Deprecated
TXD.PTR	0x544	TXD data pointer	
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer	
TXD.AMOUNT	0x54C	Number of bytes transmitted in last granted transaction	
CONFIG	0x554	Configuration register	
DEF	0x55C	Default character. Character clocked out in case of an ignored transaction.	
ORC	0x5C0	Over-read character	

32.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23 :	22 2	1 2	0 19	9 18	3 17	16	15	14	13	12 1	11 10	9	8	7	6	5	4 3	2	1	0
Id																														Α		
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	alue	:						Des	crip	tior	1																	
Α	RW	END_ACQUIRE										Sho	rtcu	t be	etwe	een	ENI) ev	ent	and	d AC	QU	IRE t	ask								
												See	EVE	NTS	S_EI	ND :	and	TAS	KS_	AC	QUI	RE										
			Disabled	0								Disa	able	sho	rtcı	ut																
			Enabled	1								Ena	ble	sho	rtcu	t																

32.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bitı	numbe	er		31 3	30 2	9 28	27 2	26 25	5 24	23 2	22 21	1 20	19	18	17 1	16 1	L5 1	4 1	3 12	2 11	. 10	9	8	7	6	5	4 3	2	1	0
Id																					С						В		Α	
Res	et 0x0	0000000		0	0 0	0 0	0	0 0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Valu	ıe					Des	cript	ion																		
Α	RW	END								Writ	te '1'	to I	Enab	le i	nter	rup	t fo	r EN	ND 6	ever	nt									
										See	EVE	NTS_	ENL)																
			Set	1						Enal	ble																			
			Disabled	0						Read	d: Di	sabl	led																	
			Enabled	1						Read	d: En	nable	ed																	
В	RW	ENDRX								Writ	te '1'	to I	Enab	le i	nter	rup	t fo	r EN	NDR	X e	vent									
										See	EVE	NTS_	ENL	ORX	(
			Set	1						Enal	ble																			
			Disabled	0						Read	d: Di	sabl	led																	
			Enabled	1						Read	d: En	nable	ed																	
С	RW	ACQUIRED								Writ	te '1'	to I	Enab	le i	nter	rup	t fo	r A(CQL	IIRE	D ev	ent								
										See	EVE	NTS_	_ACC	วบเ	RED															
			Set	1						Enal	ble																			
			Disabled	0						Read	d: Di	sabl	led																	
			Enabled	1						Read	d: En	nable	ed																	

32.5.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit nur	mbe	r		31	30 2	29 2	8 27	7 26	25	24	23 2	2 21	1 20	19	18	17	16	15 1	14 1	.3 1	2 1:	1 10	9	8	7	6 5	4	3	2 1	. 0
Id																						С					В		Δ	
Reset	0x0	0000000		0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0 0	0
Id R	RW	Field	Value Id	Val	lue						Desc	ript	ion																	
A R	RW	END									Write	e '1'	to [Disa	ble	inte	erru	ıpt f	or E	ND	eve	nt								
											See £	EVE	NTS_	_EN	D															
			Clear	1							Disab	ble																		
			Disabled	0							Read	l: Di	sabl	led																
			Enabled	1							Read	l: En	nable	ed																
B R	RW	ENDRX									Write	e '1'	to [Disa	ble	inte	erru	ıpt f	or E	ND	RX e	even	t							
											See E	EVE	NTS_	_EN	DRX	(
			Clear	1							Disab	ble																		
			Disabled	0							Read	l: Di	sabl	led																
			Enabled	1							Read	l: En	nable	ed																
C R	RW	ACQUIRED									Write	e '1'	to [Disa	ble	inte	erru	ıpt f	or A	ACQ	UIR	ED e	ven	t						
											See £	EVE	NTS_	AC	QUI	REL)													
			Clear	1							Disab	ble																		
			Disabled	0							Read	l: Di	sabl	led																
			Enabled	1							Read	l: En	nable	ed																

32.5.4 SEMSTAT

Address offset: 0x400 Semaphore status register

Bit	numbe	er		31	1 30	29	28	8 27	7 26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	5 14	1 1	3 12	2 1:	10	9	8	7	6	5	4	3	2	1 0	,
Id																																		А А	Ĺ
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 1	
Id	RW	Field	Value Id	Va	alue							De	escri	iptio	on																				ı
Α	R	SEMSTAT										Se	ma	oho	re s	tat	us																		
			Free	0								Se	ma	oho	re i	s fr	ee																		
			CPU	1								Se	ma	oho	re i	s as	ssig	ne	d to	CI	PU														
			SPIS	2								Se	ma	oho	re i	s as	ssig	ne	d to	SF	l sl	ave	•												
			CPUPending	3								Se	ma	oho	re i	s as	ssig	ne	d to	SF	d I	ut a	ha	ndo	ver	to	the	CPl	J is						
												ре	endi	ng																					

32.5.5 STATUS

Address offset: 0x440

Status from last transaction

Individual bits are cleared by writing a '1' to the bits that shall be cleared

Rit I	numbe	ar.		21	30	20	20.	77 1	26.2	5 3	04.5		າາ [.]	21	20	10	10	17	16	15	1/	1 1:	2 11	2 11	10	۱۵	Q	7	6	5	1	2 -	,	1 0
	iuiiibe	:1		31	30	23	20 .	Z / Z	20 2		14 Z	20 2	ZZ .	21	20	13	10	1/	10	13	14	1.) 12	۷ 1.	1 10	, 3	0	,	U	J	7	<i>J</i> 2	٠.	
Id																																	- 1	ВА
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																			
Α	RW	OVERREAD									7	ΓX Ł	buff	fer	ove	er-r	ead	d de	etec	tec	l, a	nd	pre	ver	ited									
			NotPresent	0							F	Rea	ıd: e	erro	r n	ot	pre	ser	nt															
			Present	1							F	Rea	d: e	erro	or p	res	en	t																
			Clear	1							١	۷ri	te:	cle	ar e	erro	or c	n v	vriti	ng	'1'													
В	RW	OVERFLOW									F	RX b	buf	fer	ove	erfl	ow	de	tect	ed,	, ar	nd p	rev	ven	ted									
			NotPresent	0							F	Rea	ıd: e	erro	r n	ot	pre	ser	nt															
			Present	1							F	Rea	ıd: e	erro	or p	res	en	t																
			Clear	1							١	۷ri	te:	cle	ar e	erro	or c	n v	vriti	ng	'1'													

32.5.6 ENABLE

Address offset: 0x500



Enable SPI slave

Bit	numbe	er		31 3	30 2	9 2	8 2	7 2	6 25	5 24	1 23	3 22	21	20	19	18	17 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																														A A	Α Δ	A
Res	et 0x0	0000000		0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Valu	ıe						De	escri	ipti	on																		
Α	RW	ENABLE									En	nable	e or	dis	able	SP	I sla	ive														
			Disabled	0							Di	sabl	le S	PI sl	ave																	
			Enabled	2							En	nable	e SF	PI sla	ave																	

32.5.7 PSELSCK (Deprecated)

Address offset: 0x508 Pin select for SCK

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22 :	21 :	20 1	19 1	18 1	7 1	6 1	.5 1	4 1	3 1	12 1	11 1	0 9	9 .	3 7	7 (6 !	5 4	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ /	4 /	Δ.	Δ ,	Δ,	Α.	A ,	A A	Δ.	A A	۱ ۸	Δ ,	A A	A /	A	Α	Α
Re	set 0x	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 :	1	1 :	1	1	1	1 :	1	1 1	ι :	1 :	L 1	L 1	. 1	1	1
Id	RW	Field	Value Id	Va	lue							De	crip	otio	n																			
Α	RW	PSELSCK		[0	31]						Pin	nur	mbe	er co	onfi	igur	atic	n f	or S	SPI S	SCK	sig	nal										
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t:																			

32.5.8 PSELMISO (Deprecated)

Address offset: 0x50C Pin select for MISO

Bit r	numb	er		31	L 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	4 A	Α	Α	Α	Α	Α	A	A /	A	Α	Α	Α	Α	Α	Α	A A	. Α	A A
Res	et Oxl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1 :	L 1	1	1	1	1	1	1	1	1 1	. 1	. 1
Id	RW	Field	Value Id	Va	alue	•						Des	crip	tio	n																	
Α	RW	PSELMISO		[0	31	.]						Pin	nun	nbe	r coi	nfig	urat	ion	for	SPI	MIS	O si	gna									
			Disconnected	0x	FFF	FFF	FF					Disc	conr	nect																		

32.5.9 PSELMOSI (Deprecated)

Address offset: 0x510 Pin select for MOSI

Bit	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A	A A A A A A A A A A A A A A A A A A A
Res	et 0xFFFFFFF		1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW Field	Value Id	Value	Description
Α	RW PSELMOSI		[031]	Pin number configuration for SPI MOSI signal
		Disconnected	Oxeefeee	Disconnect

32.5.10 PSELCSN (Deprecated)

Address offset: 0x514 Pin select for CSN

Bit number		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 :	12 1	111	0 9	9 8	3 7	6	5	4	3	2	1 0	
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ ,	Α Α	A A	. A	A	Α	Α	Α	А А	
Reset 0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1 :	1 1	l 1	1	1	1	1	1	1 1	
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																			
A RW PSELCSN		[0.	31]							Pir	nu	mb	er c	onf	igu	rati	on	for	SPI	CSN	l się	gnal										
	Disconnected	0x	FFFI	FFF	FF					Dis	con	ne	ct																			

32.5.11 PSEL.SCK

Address offset: 0x508



Pin select for SCK

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Rese	t OxF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
ld	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

32.5.12 PSEL.MISO

Address offset: 0x50C Pin select for MISO signal

Bit r	numbe	r		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

32.5.13 PSEL.MOSI

Address offset: 0x510

Pin select for MOSI signal

Bitı	numbe	er		31 30	29	28	27	26 2	25 2	4 2	3 22	21	20	19 1	.8 17	7 16	15	14 1	3 12	11	10 9	9 8	7	6	5	4	3 2	1	0
Id				С																						Α	A A	Α	Α
Res	et 0xF	FFFFFF		1 1	1	1	1	1	1 1	L 1	l 1	1	1	1 :	1 1	1	1	1 :	l 1	1	1 :	1 1	. 1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value	•					D	escr	iptic	on																
Α	RW	PIN		[031	L]					Р	in nı	ımb	er																
С	RW	CONNECT								С	onn	ectio	n																
			Disconnected	1						D	isco	nned	ct																
			Connected	0						С	onn	ect																	

32.5.14 PSEL.CSN

Address offset: 0x514

Pin select for CSN signal

Bit	numbe	er		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

32.5.15 RXDPTR (Deprecated)

Address offset: 0x534 RXD data pointer



Bit nu	ımbe	•		31	. 30	29	28	27	' 26	25	24	23	22	21	20	19	18	17 1	16 :	15 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α /	4 4	А А
Reset	0x0	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	RXDPTR										RX	D da	ata	poi	nter	r																

32.5.16 MAXRX (Deprecated)

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit	numbe	er		31	30 2	9 2	28 27	7 26	25	24	23 2	22 2	1 2	0 1	9 18	3 17	16	15	14 1	3 12	2 11	10	9	8	7	6	5 -	4 :	3 2	1	0
Id																									Α	Α	Α .	Α ,	4 A	Α	Α
Res	et 0x0	0000000		0	0 () (0 0	0	0	0	0	0 (0 (0 (0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tior	n																	
Α	RW	MAXRX									Max	κimι	ım ı	nun	nbei	of	byte	s in	rec	eive	buf	fer									

32.5.17 AMOUNTRX (Deprecated)

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit r	numbe	er		31	30	29	28	27	26	25 :	24	23 :	22 2	21 2	20 1	L9 1	18 1	17 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2	1 ()
Id																											Α	Α	Α	Α	Α .	Δ.	A A	1
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue	:						Des	crip	tio	n																			
Α	R	AMOUNTRX										Nur	nbe	r o	f by	tes	rec	eive	ed i	n th	e la	st g	ran	ted	trai	nsa	ctio	n						-

32.5.18 RXD.PTR

Address offset: 0x534 RXD data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		RXD data pointer

32.5.19 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	00000000
Id RW Field	Value Id	Value	Description		
A RW MAXCNT			Maximum number of b	ytes in receive buffer	

32.5.20 RXD.AMOUNT

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit I	numb	er		31	30 2	9 2	8 27	26	25	24	23 2	22 2	21 2	20 1	19 1	8 1	7 10	5 15	14	13	12	11 :	10 9	8 (1 0 4 A
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 0	0				0 0
Id	RW	Field	Value Id	Val	lue						Des	crip	otio	n														
	_	AAAOUNIT																			. –							

R AMOUNT Number of bytes received in the last granted transaction



32.5.21 TXDPTR (Deprecated)

Address offset: 0x544
TXD data pointer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW TXDPTR	TXD data pointer

32.5.22 MAXTX (Deprecated)

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9	8 7 6	5 4	3 2 1 0
Id					АА	АА	A A A A
Reset 0x00000000		0 0 0 0 0	00000000000	000000000	0 0 0	0 0	0 0 0 0
ld RW Field	Value Id	Value	Description				
A RW MAXTX		Maximum number of bytes in transmit buffer					

32.5.23 AMOUNTTX (Deprecated)

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

Bit nu	ımbe	er		33	1 3	0 2	9 2	8 2	7 26	25	5 24	1 23	22	21	20	19	18	17	16	15	14	13	L2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id																											Α	Α	Α	Α	Α /	Α Α	А А
Reset	0x0	0000000		0	(0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0
ld I	RW	Field	Value Id	V	alu	e						D	escr	ipti	on																		
Α	R	AMOUNTTX		Number of bytes transmitted in last granted transaction																													

32.5.24 TXD.PTR

Address offset: 0x544
TXD data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Id		A A A A A A A A A A A A A A A A A A A		
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
ld RW Field	Value Id	Value Description		
A RW PTR	TXD data pointer			

32.5.25 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
ld	A A A A A	A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id RW Field Value Id	Value Description	
Δ RW MΔXCNT	Maximum number of bytes in transmit buffer	

32.5.26 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transmitted in last granted transaction



32.5.27 CONFIG

Address offset: 0x554 Configuration register

Bit r	umbe	r		31	30	29	28 :	27 :	26 2	5 2	4 2	23 22	21	20	19	18	17	16	15	14 1	.3 1	2 11	. 10	9	8	7	6	5	4 :	3 2	1	0
Id																														С	В	Α
Res	t 0x0	0000000		0	0	0	0	0	0	0 0)	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						0	Desci	ipti	on																		
Α	RW	ORDER									Е	Bit or	der																			
			MsbFirst	0							N	Иost	sign	ific	ant	bit	shif	ted	ou	t fir	st											
			LsbFirst	1							L	.east	sign	ific	ant	bit	shif	ted	ou	t fir	st											
В	RW	СРНА									S	eria	clo	ck (5	SCK) ph	ase															
			Leading	0							S	amp	le o	n le	adi	ng e	dge	e of	clc	ck,	shift	ser	ial d	lata	on 1	trai	iling	5				
											e	edge																				
			Trailing	1							S	amp	le o	n tr	ailiı	ng e	dge	of	clo	ck, s	hift	seri	al d	ata	on l	ead	ding	5				
											e	edge																				
С	RW	CPOL									S	eria	clo	ck (SCK) pc	lari	ty														
			ActiveHigh	0							A	Activ	e hig	h																		
			ActiveLow	1							A	Activ	e lov	v																		

32.5.28 DEF

Address offset: 0x55C

Default character. Character clocked out in case of an ignored transaction.

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW DEF			Default character. Character clocked out in case of an ignored
			transaction

32.5.29 ORC

Address offset: 0x5C0 Over-read character

Bit r	iumbe	er		31	30 2	9 2	28 2	7 2	6 2	5 24	1 23	22	21	20	19	18	17 :	16	15 1	.4 1	3 1	2 11	1 10	9	8	7	6	5	4	3 2	1	0
Id																										Α	Α	Α	A	4 А	Α	Α
Rese	et 0x0	0000000		0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																		
Α	RW	ORC									0	er-	read	d ch	ara	cte	r. Cł	nara	cte	r clo	ocke	ed o	ut a	fter	r an	ove	er-re	ad				

of the transmit buffer.



32.6 Electrical Specification

32.6.1 SPIS slave interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIS}	Bit rates for SPIS ²⁶			8 ²⁷	Mbps
I _{SPIS,2Mbps}	Run current for SPIS, 2 Mbps		45		μΑ
I _{SPIS,8Mbps}	Run current for SPIS, 8 Mbps		45		μΑ
I _{SPIS,IDLE}	Idle current for SPIS (STARTed, no CSN activity)		1		μΑ
t _{SPIS,LP,START}	Time from RELEASE task to ready to receive/transmit (CSN		t _{SPIS,CL,ST}	AR	μs
	active), Low power mode		+		
			t _{START_HF}	N	
t _{SPIS,CL,START}	Time from RELEASE task to receive/transmit (CSN active),		0.125		μs
	Constant latency mode				

32.6.2 Serial Peripheral Interface Slave (SPIS) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIS} ,CSCKIN,8Mbps	SCK input period at 8Mbps		125		ns
t _{SPIS} ,CSCKIN,4Mbps	SCK input period at 4Mbps		250		ns
t _{SPIS,CSCKIN,2Mbps}	SCK input period at 2Mbps		500		ns
t _{SPIS,RFSCKIN}	SCK input rise/fall time			30	ns
t _{SPIS,WHSCKIN}	SCK input high time	30			ns
t _{SPIS,WLSCKIN}	SCK input low time	30			ns
t _{SPIS,SUCSN,LP}	CSN to CLK setup time, Low power mode	t _{SPIS,SUCS}	N,		ns
		+			
		t _{START_HE}	IN		
t _{SPIS,SUCSN,CL}	CSN to CLK setup time, Constant latency mode	1000			ns
t _{SPIS,HCSN}	CLK to CSN hold time	2000			ns
t _{SPIS,ASO}	CSN to MISO driven ^a			1000	ns
t _{SPIS,DISSO}	CSN to MISO disabled ^a			68	ns
t _{SPIS,CWH}	CSN inactive time	300			ns
t _{SPIS,VSO}	CLK edge to MISO valid			19	ns
t _{SPIS,HSO}	MISO hold time after CLK edge	18 ²⁸			ns
t _{SPIS,SUSI}	MOSI to CLK edge setup time	59			ns
t _{SPIS,HSI}	CLK edge to MOSI hold time	20			ns

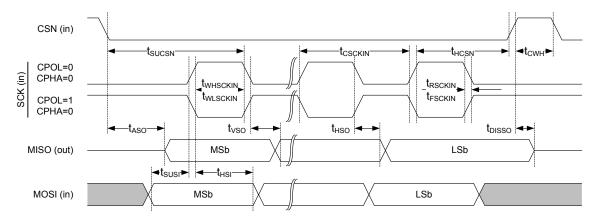


Figure 74: SPIS timing diagram

Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

²⁷ The actual maximum data rate depends on the master's CLK to MISO and MOSI setup and hold timings.

^a At 25pF load, including GPIO capacitance, see GPIO spec.

This is to ensure compatibility to SPI masters sampling MISO on the same edge as MOSI is output



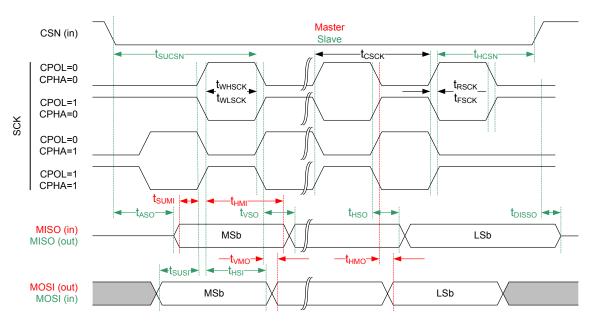


Figure 75: Common SPIM and SPIS timing diagram



33 TWIM — I²C compatible two-wire interface master with EasyDMA

TWI master with EasyDMA (TWIM) is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus

Listed here are the main features for TWIM:

- I²C compatible
- 100 kbps, 250 kbps, or 400 kbps
- · Support for clock stretching
- EasyDMA

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. TWIM is not compatible with CBUS.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

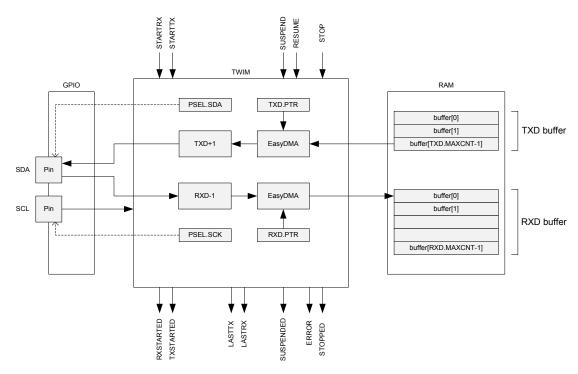


Figure 76: TWI master with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 77: A typical TWI setup comprising one master and three slaves* on page 301. This TWIM is only able to operate as a single master on the TWI bus. Multi-master bus configuration is not supported.

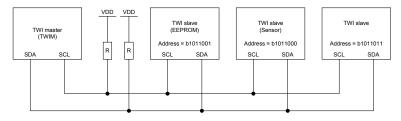


Figure 77: A typical TWI setup comprising one master and three slaves



This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task. The TWI master will generate a STOPPED event when it has stopped following a STOP task.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

After the TWI master is started, the STARTTX task or the STARTRX task should not be triggered again before the TWI master has stopped, i.e. following a LASTRX, LASTTX or STOPPED event.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

33.1 Shared resources

The TWI master shares registers and other resources with other peripherals that have the same ID as the TWI master. Therefore, you must disable all peripherals that have the same ID as the TWI master before the TWI master can be configured and used.

Disabling a peripheral that has the same ID as the TWI master will not reset any of the registers that are shared with the TWI master. It is therefore important to configure all relevant registers explicitly to secure that the TWI master operates correctly.

The Instantiation table in *Instantiation* on page 21 shows which peripherals have the same ID as the TWI.

33.2 EasyDMA

The TWI master implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

33.2.1 EasyDMA list

EasyDMA supports one list type.

The supported list type is:

Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type.

For illustration, see the code example below. This data structure includes only a buffer with size equal to Channel.MAXCNT. EasyDMA will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.

The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

#define BUFFER SIZE 4



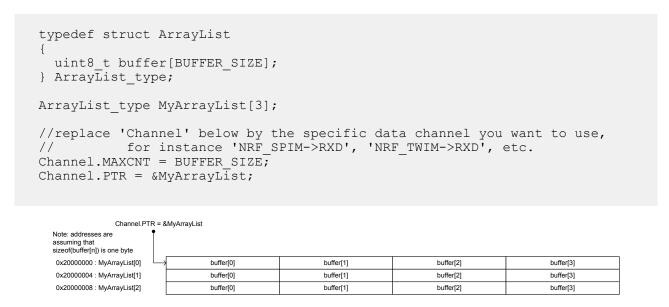


Figure 78: EasyDMA array list

33.3 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes found in the transmit buffer located in RAM at the address specified in the TXD.PTR register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave.

A typical TWI master write sequence is illustrated in *Figure 79: TWI master writing data to a slave* on page 303. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

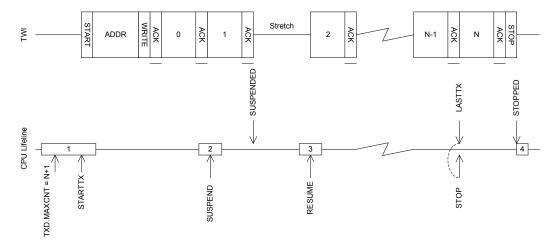


Figure 79: TWI master writing data to a slave

The TWI master will generate a LASTTX event when it starts to transmit the last byte, this is illustrated in *Figure 79: TWI master writing data to a slave* on page 303



The TWI master is stopped by triggering the STOP task, this task should be triggered during the transmission of the last byte to secure that the TWI will stop as fast as possible after sending the last byte. It is safe to use the shortcut between LASTTX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the whole RAM buffer has been sent, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

33.4 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1). The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

Data received will be stored in RAM at the address specified in the RXD.PTR register. The TWI master will generate an ACK after all but the last byte received from the slave. The TWI master will generate a NACK after the last byte received to indicate that the read sequence shall stop.

A typical TWI master read sequence is illustrated in *Figure 80: The TWI master reading data from a slave* on page 305. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

The TWI master will generate a LASTRX event when it is ready to receive the last byte, this is illustrated in *Figure 80: The TWI master reading data from a slave* on page 305. If RXD.MAXCNT > 1 the LASTRX event is generated after sending the ACK of the previously received byte. If RXD.MAXCNT = 1 the LASTRX event is generated after receiving the ACK following the address and READ bit.

The TWI master is stopped by triggering the STOP task, this task must be triggered before the NACK bit is supposed to be transmitted. The STOP task can be triggered at any time during the reception of the last byte. It is safe to use the shortcut between LASTRX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the RAM buffer is full, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.



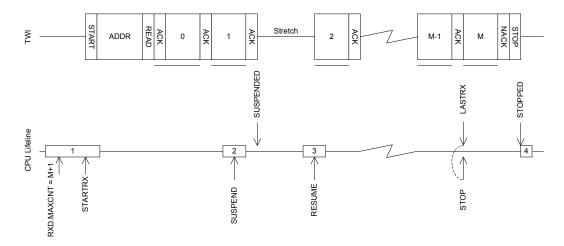


Figure 80: The TWI master reading data from a slave

33.5 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave. This example uses shortcuts to perform the simplest type of repeated start sequence, i.e. one write followed by one read. The same approach can be used to perform a repeated start sequence where the sequence is read followed by write.

The figure Figure 81: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave on page 305 illustrates this:

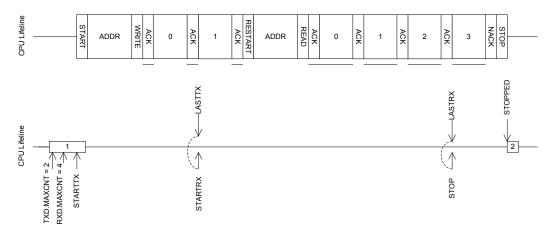


Figure 81: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave

If a more complex repeated start sequence is needed and the TWI firmware drive is serviced in a low priority interrupt it may be necessary to use the SUSPEND task and SUSPENDED event to guarantee that the correct tasks are generated at the correct time. This is illustrated in *Figure 82: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts* on page 306.



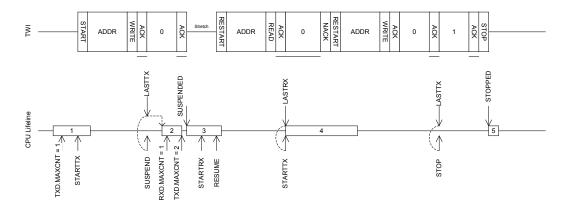


Figure 82: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts

33.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

33.7 Master mode pin configuration

The SCL and SDA signals associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL, PSEL.SDA must only be configured when the TWI master is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 69: GPIO configuration before enabling peripheral* on page 306.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 69: GPIO configuration before enabling peripheral

TWI master signal	TWI master pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	SOD1
SDA	As specified in PSEL.SDA	Input	Not applicable	S0D1

33.8 Registers

Table 70: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIM	TWIM0	Two-wire interface master 0	
0x40004000	TWIM	TWIM1	Two-wire interface master 1	

Table 71: Register Overview



Register	Offset	Description
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction. Must be issued while the TWI master is not suspended.
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_SUSPENDED	0x148	Last byte has been sent out after the SUSPEND task has been issued, TWI traffic is now suspended.
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_LASTRX	0x15C	Byte boundary, starting to receive the last byte
EVENTS_LASTTX	0x160	Byte boundary, starting to transmit the last byte
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWIM
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
FREQUENCY	0x524	TWI frequency
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
ADDRESS	0x588	Address used in the TWI transfer

33.8.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F D C B A
Res	set 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW LASTTX_STARTRX			Shortcut between LASTTX event and STARTRX task
				See EVENTS_LASTTX and TASKS_STARTRX
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
В	RW LASTTX_SUSPEND			Shortcut between LASTTX event and SUSPEND task
				See EVENTS_LASTTX and TASKS_SUSPEND
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
С	RW LASTTX_STOP			Shortcut between LASTTX event and STOP task
				See EVENTS_LASTTX and TASKS_STOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
D	RW LASTRX_STARTTX			Shortcut between LASTRX event and STARTTX task
				See EVENTS_LASTRX and TASKS_STARTTX
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
F	RW LASTRX_STOP			Shortcut between LASTRX event and STOP task



Bit number		31 3	30 29	9 28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	' 16	15	14	13	12 1	.1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																			F	D	С	В	Α						
Reset 0x00000000		0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id RW Field	Value Id	Valu	ıe						Des	crip	otio	n																	
									See	EV	ENT	rs_L	AST	RX a	nd	TAS	KS_	STO)P										
	Disabled	0							Disa	able	sh	orto	ut																
	Enabled	1							Ena	ble	sho	ortci	ut																

33.8.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	number			31 3	30 29	9 28 2	27 2	6 25	24	23 2:	2 21	20	19 1	18 1	17 1	.6 1	5 1	.4 1	.3 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id									J	1		Н	G	F								D							Α	
Res	et 0x00000000			0	0 0	0	0 (0	0	0 0	0	0	0	0	0 (0 () (0	0 () (0 0	0	0	0	0	0	0 0	0	0	0
ld	RW Field		Value Id	Valu	ue					Desc	riptio	on																		
Α	RW STOPPE	D								Enab	le or	dis	able	int	erru	upt	for	ST	OPP	ED	eve	nt								
										See £	VEN	TS_	STO	PPE	ED															
			Disabled	0						Disak	ole																			
			Enabled	1						Enab	le																			
D	RW ERROR									Enab	le or	dis	able	int	errı	upt	for	ER	ROF	≀ ev	/ent									
										See E	VEN	TS	ERR	OR																
			Disabled	0						Disak		Ī																		
			Enabled	1						Enab	le																			
F	RW SUSPEN	DED								Enab	le or	dis	able	int	errı	upt	for	SU	SPE	ND	ED e	ver	ıt							
										See E	VEN	TS	SUS	PEN	NDE	D														
			Disabled	0						Disak		_																		
			Enabled	1						Enab	le																			
G	RW RXSTAR	TED								Enab	le or	dis	able	int	erru	upt	for	RX	STA	RTE	ED e	ven	t							
									:	See £	VEN	TS	RXS	TAF	RTEL)														
			Disabled	0						Disab		Ī																		
			Enabled	1						Enab	le																			
Н	RW TXSTAR	TED								Enab	le or	dis	able	int	errı	upt	for	TX	STA	RTE	ED e	ven	t							
										See £	VEN	TS	TXS	TAF	RTEL)														
			Disabled	0						Disab		Ī																		
			Enabled	1						Enab	le																			
I	RW LASTRX									Enab	le or	dis	able	int	erru	upt	for	LA	STR:	X e	vent									
										See £	VEN	TS_	LAS	TRX	(
			Disabled	0						Disab		Ī																		
			Enabled	1						Enab	le																			
J	RW LASTTX									Enab	le or	dis	able	int	errı	upt	for	LA	STT	X e	vent									
										See E	VEN	TS	LAS	ттх																
			Disabled	0						Disak		_																		
			Enabled	1						Enab	le																			

33.8.3 INTENSET

Address offset: 0x304 Enable interrupt

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23 :	22 2	1 2	0 1	9 18	3 17	16	15	14	13	12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id											J	L		H	1 0	i F									D							Α	
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	ı																		
Α	RW	STOPPED										Wri	te '1	' to	Ena	able	int	err	upt	for	STC	PPI	Dε	ver	nt								



Bitı	numbe	r		31 30	29	28 2	27 26	25	24	23	22 21	. 20	0 19	18	8 17	1	5 15	14	1	3 1	2 1	1 1	0 9	9 8	3 7	6	5	4	3	2	1	0
Id									J	1		Н	I G	F									[)							Α	
Res	et 0x0(0000000		0 0	0	0	0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	() () () (0 (0	0	0	0	0	0	0	0
ld	RW	Field	Value Id	Value						Des	scripti	ion)																			
									:	See	e EVEN	VTS	S_ST	OF	PEC)																
			Set	1						Ena	able																					
			Disabled	0						Rea	ad: Dis	sab	led																			
			Enabled	1						Rea	ad: En	ab	led																			
D	RW	ERROR							,	Wri	ite '1'	to	Ena	ble	int	err	upt	for	EF	RC)R e	ever	nt									
									:	See	e EVEN	VTS	ER	RC)R																	
			Set	1						Ena	able																					
			Disabled	0						Rea	ad: Dis	sab	led																			
			Enabled	1						Rea	ad: En	ab	led																			
F	RW	SUSPENDED							,	Wri	ite '1'	to	Ena	ble	int	err	upt	for	S۱	JSP	EN	DEC) ev	/ent								
									:	See	e EVEN	VTS	_SL	ISP	ENE	EL)															
			Set	1						Ena	able																					
			Disabled	0						Rea	ad: Dis	sab	led																			
			Enabled	1						Rea	ad: En	ab	led																			
G	RW	RXSTARTED							,	Wri	ite '1'	to	Ena	ble	int	err	upt	for	R۷	(ST	AR	ΓED	ev	ent								
									:	See	e EVEN	VTS	S_RX	ST	ART	ΈD																
			Set	1						Ena	able																					
			Disabled	0						Rea	ad: Dis	sab	led																			
			Enabled	1							ad: En																					
Н	RW	TXSTARTED							,	Wri	ite '1'	to	Ena	ble	int	err	upt	for	· T>	ST	ART	ΓED	ev	ent								
											e EVEN	VTS	_TX	ST	ART	ED																
			Set	1							able																					
			Disabled	0							ad: Dis																					
			Enabled	1							ad: En																					
I	RW	LASTRX							,	Wri	ite '1'	to	Ena	ble	int	err	upt	for	· LA	ST	RX (eve	nt									
											e EVEN	VTS	_LA	ST	RX																	
			Set	1							able																					
			Disabled	0							ad: Dis																					
			Enabled	1							ad: En																					
J	RW	LASTTX							,	Wri	ite '1'	to	Ena	ble	int	err	upt	for	L/	ST	TX (eve	nt									
										See	e EVEN	VTS	_LA	ST	TX																	
			Set	1						Ena	able																					
			Disabled	0						Rea	ad: Dis	sab	led																			
			Enabled	1						Rea	ad: En	ab	led																			

33.8.4 INTENCLR

Address offset: 0x308 Disable interrupt

Bit r	umbe	r		31	30 2	29 :	28 2	27 2	26 2	:5 2	4 2	3 22	21	20	19	18	17 1	.6 1	L5 1	4 1	3 12	11	10	9 8	3 7	6	5	4	3 2	2 1	. 0
Id											J I			Н	G	F								D						Д	
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0	0 (0	0 0	0	0	0	0 (0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	n																	
Α	RW	STOPPED									٧	/rite	'1' t	o D	isal	ole i	inte	rru	pt f	or S	OPF	PED	eve	nt							
											S	ee <i>E</i>	VEN	TS_	STC	PP	ED														
			Clear	1							D	isab	le																		
			Disabled	0							R	ead:	Disa	able	ed																
			Enabled	1							R	ead:	Ena	ble	d																
D	RW	ERROR									٧	/rite	'1' t	o D	isal	ole i	inte	rru	pt f	or El	RROI	R ev	ent								
											S	ee <i>E</i>	VEN	TS_	ERF	ROR															
			Clear	1							D	isab	le																		

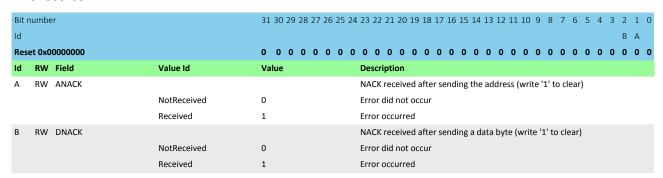


Bitı	number		31 30 29 28 27 26 25 24	\$ 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			J	I HGF D A
Res	set 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW SUSPENDED			Write '1' to Disable interrupt for SUSPENDED event
				See EVENTS_SUSPENDED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW RXSTARTED			Write '1' to Disable interrupt for RXSTARTED event
				See EVENTS_RXSTARTED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW TXSTARTED			Write '1' to Disable interrupt for TXSTARTED event
		Class	4	See EVENTS_TXSTARTED
		Clear Disabled	0	Disable Read: Disabled
		Enabled		
	RW LASTRX	Enableu	1	Read: Enabled Write '1' to Disable interrupt for LASTRX event
	NW LASINA			write 1 to disable interrupt for LASTAX event
				See EVENTS_LASTRX
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW LASTTX			Write '1' to Disable interrupt for LASTTX event
				See EVENTS_LASTTX
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

33.8.5 ERRORSRC

Address offset: 0x4C4

Error source



33.8.6 ENABLE

Address offset: 0x500

Enable TWIM



Bit	numbe	er		31 30	29	28 2	27 2	6 25	5 24	23	22 2	21 2	0 19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																												Α	A	4 А
Res	et 0x0	0000000		0 0	0	0	0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value						De	scrip	otior	1																	
Α	RW	ENABLE								Ena	able	or d	lisab	le T	WII	VI														
			Disabled	0						Dis	able	TW	ΊM																	
			Enabled	6						Ena	able	TW	М																	

33.8.7 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

33.8.8 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

Bitı	iumbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

33.8.9 FREQUENCY

Address offset: 0x524

TWI frequency

Е	Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	.7 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 4	A A
F	Rese	t 0x0	4000000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
ı	d	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
A	Ą	RW	FREQUENCY										ΤV	VI m	aste	er c	lock	fre	que	enc	у														
				K100	0x	019	800	000					10	0 kb	ps																				
				K250	0x	040	000	000					25	0 kb	ps																				
				K400	0x	064	000	000					40	0 kb	ps																				

33.8.10 RXD.PTR

Address offset: 0x534

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer



33.8.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit nur	mber		31 30 29 28 27 26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A
Reset	0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld F	RW Field	Value Id	Value Description	
A F	RW MAXCNT		[1255] Maximum number of	f bytes in receive buffer

33.8.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit r	iumb	er		31	30	29	28 :	27 2	26 2	25 2	24 2	23 2	22 2	1 2	0 1	9 18	3 17	7 16	5 15	14	13	12	11 :	10 !	9	8	7	6	5 4	1 3	3 2	1	0
Id																											Α.	A	A A	۱ ۸	A A	Α	Α
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tio	1																		
	R AMOUNT Number of bytes transferred in the last transaction. In case of																																
Α	R	AMOUNT									ı	Nun	nbe	r of	byt	es t	ran	ısfe	rrec	l in	the	last	tra	ารลด	ctio	n. I	n ca	ise	ot				

33.8.13 RXD.LIST

Address offset: 0x540 EasyDMA list type

Bit	numb	er		31 30	29	28 2	7 2	6 25	5 24	23	22 2	1 20) 19	18	17	16	15	14 1	3 1	2 11	10	9	8	7	6	5	4	3	2	1 0
Id																													Α	А А
Res	et Ox(0000000		0 0	0	0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value						De	scrip	tion																		
Α	RW	LIST								List	t type	ė																		
			Disabled	0						Dis	able	Eas	yDN	1A lis	st															
			ArrayList	1						Us	e arra	ay li:	st																	

33.8.14 TXD.PTR

Address offset: 0x544

Data pointer

Bit number		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	ĺ
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
Id RW Field	Value Id	Va	alue							De	scri	ptic	on																				l
A RW PTR										Dat	ta p	oin	ter																				1

33.8.15 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW MAXCNT		[1255]	Maximum number of bytes in transmit buffer



33.8.16 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit	numbe	er		31	. 30	29	28	27 2	6 2	5 2	4 2	3 22	2 21	. 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id																											Α	Α	Α	Α	A A	A /	A A
Res	et 0x0	0000000		0	0	0	0	0 0) (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	ion																			
Α	R	AMOUNT									Ν	lum	ber	of b	oyte	s tr	ans	ferr	ed	in t	he l	last	tra	nsa	ctio	n. I	ln c	ase	of				
																		•		121 -													

33.8.17 TXD.LIST

Address offset: 0x550 EasyDMA list type

Bit r	numbe	er		31 30	29	28	27 2	26 2	25 2	4 2	3 22	2 21	20	19	18 :	17 1	l6 1	.5 1	4 13	12	11 :	10 9	8	7	6	5	4	3	2	1 0
Id																													A	А А
Res	et 0x0	0000000		0 0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 (0 (0	0	0	0 (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	•					D	esci	ripti	ion																	
Α	RW	LIST								Li	st ty	ype																		
			Disabled	0						D	isab	le E	asyl	DM	A lis	t														
			ArrayList	1						U	se a	ırra	/ list	:																

33.8.18 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bitı	numbe	er		31 30 29 28 27	26 25 24	23 22 2	1 20 1	9 18	17 1	5 15	14 13	3 12 1	1 10	9	8 7	6	5	4	3 2	1 0
Id																Α	Α	Α	A A	A A
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	0 0 0	0 0	0 0	0 0	0	0 0	0 (0	0	0 0	0	0	0	0 0	0 0
Id	RW	Field	Value Id	Value		Descrip	tion													
Α	RW	ADDRESS				Address	used	in the	e TWI	trans	fer									

33.9 Electrical Specification

33.9.1 TWIM interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIM}	Bit rates for TWIM ²⁹	100		400	kbps
I _{TWIM,100kbps}	Run current for TWIM, 100 kbps		50		μΑ
I _{TWIM,400kbps}	Run current for TWIM, 400 kbps		50		μΑ
t _{TWIM,START,LP}	Time from STARTRX/STARTTX task to transmission started, Low		t _{TWIM,ST}	AR1	μs
	power mode		+		
			t _{START_H}	FIN	
t _{TWIM,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1.5		μs
	Constant latency mode				

33.9.2 Two Wire Interface Master (TWIM) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIM,SCL,100kbps}	SCL clock frequency, 100 kbps		100		kHz
f _{TWIM,SCL,250kbps}	SCL clock frequency, 250 kbps		250		kHz
f _{TWIM,SCL,400kbps}	SCL clock frequency, 400 kbps		400		kHz

Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIM,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWIM,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWIM,HD_STA,100kbps}	TWIM master hold time for START and repeated START	10000			ns
	condition, 100 kbps				
$t_{TWIM,HD_STA,250kbps}$	TWIM master hold time for START and repeated START	4000			ns
	condition, 250kbps				
$t_{TWIM,HD_STA,400kbps}$	TWIM master hold time for START and repeated START	2500			ns
	condition, 400 kbps				
$t_{TWIM,SU_STO,100kbps}$	TWIM master setup time from SCL high to STOP condition, 100	5000			ns
	kbps				
$t_{TWIM,SU_STO,250kbps}$	TWIM master setup time from SCL high to STOP condition, 250	2000			ns
	kbps				
$t_{TWIM,SU_STO,400kbps}$	TWIM master setup time from SCL high to STOP condition, 400	1250			ns
	kbps				
t _{TWIM,BUF,100kbps}	TWIM master bus free time between STOP and START	5800			ns
	conditions, 100 kbps				
t _{TWIM,BUF,250kbps}	TWIM master bus free time between STOP and START	2700			ns
	conditions, 250 kbps				
t _{TWIM,BUF,400kbps}	TWIM master bus free time between STOP and START	2100			ns
	conditions, 400 kbps				

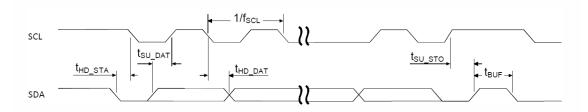


Figure 83: TWIM timing diagram, 1 byte transaction

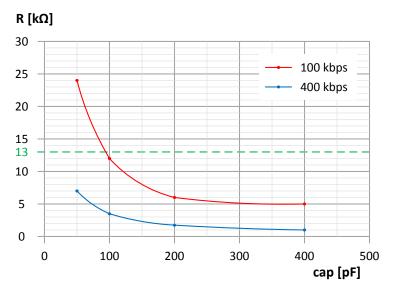


Figure 84: Recommended TWIM pullup value vs. line capacitance

- The I2C specification allows a line capacitance of 400 pF at most.
- The nRF52832 internal pullup has a fixed value of typ. 13 kOhm, see R_{PU} in the GPIO chapter.



34 TWIS — I²C compatible two-wire interface slave with EasyDMA

TWI slave with EasyDMA (TWIS) is compatible with I²C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

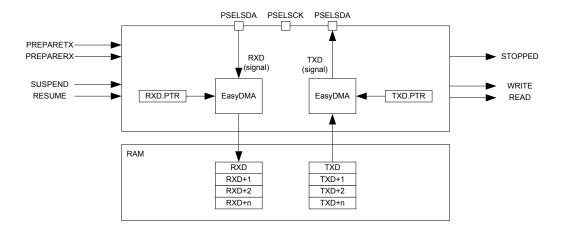


Figure 85: TWI slave with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 86: A typical TWI setup comprising one master and three slaves* on page 315. TWIS is only able to operate with a single master on the TWI bus.

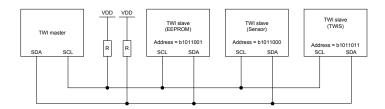


Figure 86: A typical TWI setup comprising one master and three slaves

The TWI slave state machine is illustrated in *Figure 87: TWI slave state machine* on page 316 and *Table 72: TWI slave state machine symbols* on page 316 is explaining the different symbols used in the state machine.



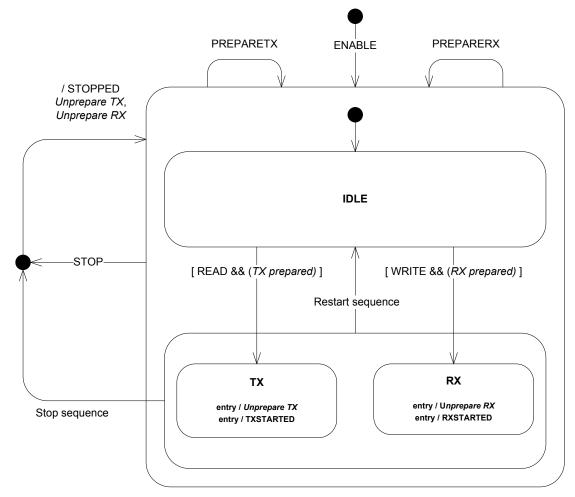


Figure 87: TWI slave state machine

Table 72: TWI slave state machine symbols

Symbol	Туре	Description
ENABLE	Register	The TWI slave has been enabled via the ENABLE register
PREPARETX	Task	The TASKS_PREPARETX task has been triggered
STOP	Task	The TASKS_STOP task has been triggered
PREPARERX	Task	The TASKS_PREPARERX task has been triggered
STOPPED	Event	The EVENTS_STOPPED event was generated
RXSTARTED	Event	The EVENTS_RXSTARTED event was generated
TXSTARTED	Event	The EVENTS_TXSTARTED event was generated
TX prepared	Internal	Internal flag indicating that a TASKS_PREPARETX task has been triggered. This flag is not visible to the user.
RX prepared	Internal	Internal flag indicating that a TASKS_PREPARERX task has been triggered. This flag is not visible to the user.
Unprepare TX	Internal	Clears the internal 'TX prepared' flag until next TASKS_PREPARETX task.
Unprepare RX	Internal	Clears the internal 'RX prepared' flag until next TASKS_PREPARERX task.
Stop sequence	TWI protocol	A TWI stop sequence was detected
Restart sequence	TWI protocol	A TWI restart sequence was detected

The TWI slave supports clock stretching performed by the master.

The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

To secure correct behaviour of the TWI slave, PSEL.SCL, PSEL.SDA, CONFIG and the ADDRESS[n] registers, must be configured prior to enabling the TWI slave through the ENABLE register. Similarly, changing these settings must be performed while the TWI slave is disabled. Failing to do so may result in unpredictable behaviour.



34.1 Shared resources

The TWI slave shares registers and other resources with other peripherals that have the same ID as the TWI slave.

Therefore, you must disable all peripherals that have the same ID as the TWI slave before the TWI slave can be configured and used. Disabling a peripheral that has the same ID as the TWI slave will not reset any of the registers that are shared with the TWI slave. It is therefore important to configure all relevant registers explicitly to secure that the TWI slave operates correctly.

The Instantiation table in *Instantiation* on page 21 shows which peripherals have the same ID as the TWI slave.

34.2 EasyDMA

The TWI slave implements EasyDMA for reading and writing to and from the RAM.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

34.3 TWI slave responding to a read command

Before the TWI slave can respond to a read command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{\rm IDLE}$.

A read command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the TWI slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the read command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a READ event when it acknowledges the read command.

The TWI slave is only able to detect a read command from the IDLE state.

The TWI slave will set an internal 'TX prepared' flag when the PREPARETX task is triggered.

When the read command is received the TWI slave will enter the TX state if the internal 'TX prepared' flag is set.

If the internal 'TX prepared' flag is not set when the read command is received, the TWI slave will stretch the master's clock until the PREPARETX task is triggered and the internal 'TX prepared' flag is set.

The TWI slave will generate the TXSTARTED event and clear the 'TX prepared' flag ('unprepare TX') when it enters the TX state. In this state the TWI slave will send the data bytes found in the transmit buffer to the master using the master's clock. The TWI slave will consume I_{TX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the TX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the 'TX prepared' flag ('unprepare TX') and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If the TWI master



forces the slave to send more than TXD.MAXCNT bytes, the slave will send the byte specified in the ORC register to the master instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see TXD.PTR etc., are latched when the TXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the 'TX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 320.

Each byte sent from the slave will be followed by an ACK/NACK bit sent from the master. The TWI master will generate a NACK following the last byte that it wants to receive to tell the slave to release the bus so that the TWI master can generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWI slave read command response is illustrated in *Figure 88: The TWI slave responding to a read command* on page 318. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

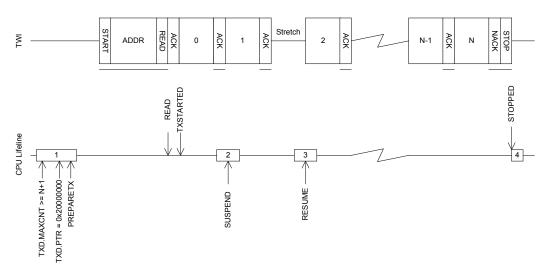


Figure 88: The TWI slave responding to a read command

34.4 TWI slave responding to a write command

Before the TWI slave can respond to a write command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{\rm IDLE}$.

A write command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the write command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a WRITE event if it acknowledges the write command.

The TWI slave is only able to detect a write command from the IDLE state.

The TWI slave will set an internal 'RX prepared' flag when the PREPARERX task is triggered.

When the write command is received the TWI slave will enter the RX state if the internal 'RX prepared' flag is set.

If the internal 'RX prepared' flag is not set when the write command is received, the TWI slave will stretch the master's clock until the PREPARERX task is triggered and the internal 'RX prepared' flag is set.



The TWI slave will generate the RXSTARTED event and clear the internal 'RX prepared' flag ('unprepare RX') when it enters the RX state. In this state the TWI slave will be able to receive the bytes sent by the TWI master. The TWI slave will consume I_{RX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the RX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the internal 'RX prepared' flag ('unprepare RX') and go back to the IDLE state when it has stopped.

The receive buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to receive as many bytes as specified in the RXD.MAXCNT register. If the TWI master tries to send more bytes to the slave than the slave is able to receive, these bytes will be discarded and the bytes will be NACKed by the slave. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see RXD.PTR etc., are latched when the RXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the internal 'RX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 320.

The TWI slave will generate an ACK after every byte received from the master. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWI slave write command response is illustrated in *Figure 89: The TWI slave responding to a write command* on page 319. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

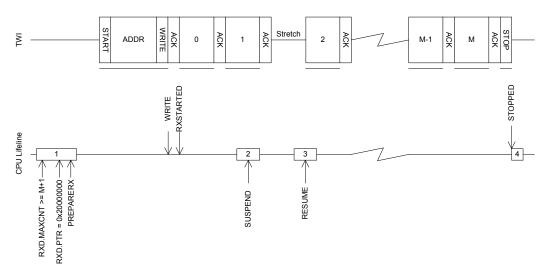


Figure 89: The TWI slave responding to a write command

34.5 Master repeated start sequence

An example of a repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave.

This is illustrated in Figure 90: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave on page 320.

It is here assumed that the receiver does not know in advance what the master wants to read, and that this information is provided in the first two bytes received in the write part of the repeated start sequence. To guarantee that the CPU is able to process the received data before the TWI slave starts to reply to the read command, the SUSPEND task is triggered via a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.



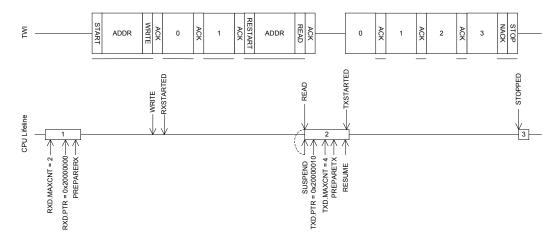


Figure 90: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave

34.6 Terminating an ongoing TWI transaction

In some situations, e.g. if the external TWI master is not responding correctly, it may be required to terminate an ongoing transaction.

This can be achieved by triggering the STOP task. In this situation a STOPPED event will be generated when the TWI has stopped independent of whether or not a STOP condition has been generated on the TWI bus. The TWI slave will release the bus when it has stopped and go back to its IDLE state.

34.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

34.8 Slave mode pin configuration

The SCL and SDA signals associated with the TWI slave are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI slave is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL and PSEL.SDA must only be configured when the TWI slave is disabled.

To secure correct signal levels on the pins used by the TWI slave when the system is in OFF mode, and when the TWI slave is disabled, these pins must be configured in the GPIO peripheral as described in *Table 73: GPIO configuration before enabling peripheral* on page 320.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 73: GPIO configuration before enabling peripheral

TWI slave signal	TWI slave pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	SOD1
SDA	As specified in PSEL.SDA	Input	Not applicable	SOD1



34.9 Registers

Table 74: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
0x40004000	TWIS	TWIS1	Two-wire interface slave 1	

Table 75: Register Overview

Register	Offset	Description
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
TASKS_PREPARERX	0x030	Prepare the TWI slave to respond to a write command
TASKS_PREPARETX	0x034	Prepare the TWI slave to respond to a read command
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_WRITE	0x164	Write command received
EVENTS_READ	0x168	Read command received
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4D0	Error source
MATCH	0x4D4	Status register indicating which address had a match
ENABLE	0x500	Enable TWIS
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
RXD.PTR	0x534	RXD Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in RXD buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last RXD transaction
TXD.PTR	0x544	TXD Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in TXD buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last TXD transaction
ADDRESS[0]	0x588	TWI slave address 0
ADDRESS[1]	0x58C	TWI slave address 1
CONFIG	0x594	Configuration register for the address match mechanism
ORC	0x5C0	Over-read character. Character sent out in case of an over-read of the transmit buffer.

34.9.1 SHORTS

Address offset: 0x200

Shortcut register

Bit r	numbe	er		3	1 30	29	2	8 2	7 2	6 2	5 2	24 :	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						В	Α													
Res	et 0x0	0000000		0	0	0	C	0) (0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	alue	•						- 1	Des	scr	ipti	on																				
Α	RW	WRITE_SUSPEND											Shc	orto	cut l	oetv	we	en '	WR	ITE	eve	nt	and	SU	SPE	ND	tas	k								
													See	E	VEN	TS_	W	RITI	ar	nd 7	ASI	(S	SUS	PEI	VD											
			Disabled	0								ı	Dis	ab	le sł	ort	cu	t																		
			Enabled	1								-	Ena	bl	e sh	ort	cut	:																		
В	RW	READ_SUSPEND										:	Shc	orto	cut l	oetv	we	en l	REA	D e	ver	nt a	nd :	SUS	PEN	ND t	ask	(
													See	. E	VEN	TS_	RE	AD	and	d TA	1 <i>5K</i> .	s_s	USF	PEN	D											



Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

34.9.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Rit	numbe	r _		31	30	29	28 1	27 1	26.2)5 :	04.2	3 2	2 21	20) 19	18	17	16	15	14	. 1:	3 1 1	2 1	1 1	0 9	9 5	ጻ 7	' 6	5 -	; <i>A</i>	3	2	1	0
Id	Tarribe			51	. 50	23	20 /		20 Z H (. T Z.	<i>J</i> 2			E .	10	/	10	. 10		1.	, 12	- 1	. 1	O 3		<i>J</i>	,	, ,	,	3	_	A	J
	at NvN	000000		0	٥	٥	0				0 0	, ,	0 0			٥	٥	٥	٥	٥	٥	۸		, ,			n n				٥	٥		0
Id		Field	Value Id		alue	Ŭ		Ĭ	•	•			cripti			Ŭ	Ŭ	Ŭ	Ŭ	Ŭ	Ĭ	Ĭ									ŭ	Ŭ	Ŭ	Ĭ
A		STOPPED	Value la		uc								ole o			le iı	nter	rup	ot f	or S	то	PPI	ED	eve	nt									
											Se	ee l	EVEN	VTS.	_ST	OPI	PED																	
			Disabled	0							D	isal	ble																					
			Enabled	1							Ei	nab	ole																					
В	RW	ERROR									Eı	nab	ole or	r di	sabl	le ii	nter	rup	ot f	or E	RR	OR	ev	ent										
											S	ee l	EVEN	VTS.	_ER	RO	R																	
			Disabled	0							D	isal	ble																					
			Enabled	1							E	nab	ole																					
Е	RW	RXSTARTED									Eı	nab	ole oi	r di	sabl	le ii	nter	rup	ot f	or F	RXS	TAF	RTE	Dε	ever	nt								
											S	ee l	EVEN	VTS.	_RX	STA	ART	ED																
			Disabled	0							D	isal	ble																					
			Enabled	1							E	nab	ole																					
F	RW	TXSTARTED									Eı	nab	ole or	r di	sabl	le ii	nter	rup	ot f	or 1	XS	TAF	RTE	Dε	ver	nt								
											Se	ee l	EVEN	VTS.	_TX	STA	\RT	ED																
			Disabled	0							D	isal	ble																					
			Enabled	1							E	nab	ole																					
G	RW	WRITE									Eı	nab	ole or	r di	sabl	le ii	nter	rup	ot f	or \	۷R	ITE	eve	ent										
											S	ee l	EVEN	VTS.	_W	RIT	E																	
			Disabled	0							D	isal	ble																					
			Enabled	1							Eı	nab	ole																					
Н	RW	READ									Eı	nab	ole or	r di	sabl	le ii	nter	rup	ot f	or F	REA	D e	eve	nt										
											S	ee l	EVEN	VTS.	_RE	AD																		
			Disabled	0							D	isal	ble																					
			Enabled	1							E	nab	ole																					

34.9.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	numbe	er		31	30 2	29	28 2	27	26 2	5 2	24 2	23 :	22 2	21 2	0 1	19 1	8 1	.7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id									Н	G				F		E									В							A	Д
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 0)	0 ()	0 () (0	0	0	0	0	0	0	0	0	0	0	0) (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otion	ı																		
Α	RW	STOPPED									١	Nri	te '	1' to	Er	nabl	e ir	iter	up	t for	ST	OPP	ED	evei	nt								
											9	See	EV	ENT	S_S	STO	PPE	D															
			Set	1							E	Ena	ble																				
			Disabled	0							F	Rea	ıd: E	Disab	ole	d																	
			Enabled	1							F	Rea	ıd: E	nab	lec	t																	
В	RW	ERROR									١	Wri	te '	1' to	Er	nabl	e ir	iter	up	t for	ER	ROR	ev	ent									



Bit number	31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	н	G F E B A
Reset 0x00000000	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
		See EVENTS_ERROR
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
E RW RXSTARTED		Write '1' to Enable interrupt for RXSTARTED event
		See EVENTS_RXSTARTED
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
F RW TXSTARTED		Write '1' to Enable interrupt for TXSTARTED event
		See EVENTS_TXSTARTED
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
G RW WRITE		Write '1' to Enable interrupt for WRITE event
		See EVENTS_WRITE
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
H RW READ		Write '1' to Enable interrupt for READ event
		See EVENTS_READ
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
Ellableu	1	Neau. Lilabieu

34.9.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit n	iumbe	er		31 3	30 29	9 28 2	27 2	26 25	24	23	3 22	2 21	20	19 1	8 1	7 16	5 15	14	13 1	2 1	1 10	9	8	7	6 5	5 4	3	2	1 0
Id								H G					F	Е								В							Α
Rese	et 0x0	0000000		0	0 0	0	0	0 0	0	0	0	0	0	0 0) (0	0	0	0 (0	0	0	0	0	0 (0 0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe					De	esci	riptic	on																
Α	RW	STOPPED								Wr	rite	e '1' t	to D	isabl	e ir	nter	upt	for	STO	PPEI	D ev	ent							
										Se	e E	VEN	TS	STOF	PE	D													
			Clear	1						Dis	sab	ole																	
			Disabled	0						Re	ad	: Disa	able	d															
			Enabled	1						Re	ad	: Ena	ble	d															
В	RW	ERROR								Wr	rite	e '1' t	to D	isabl	e ir	nter	upt	for	ERR	OR 6	even	t							
										Se	e E	VEN	TS_	ERRO	OR														
			Clear	1						Dis	sab	ole																	
			Disabled	0						Re	ad	: Disa	able	d															
			Enabled	1						Re	ad	: Ena	ble	d															
E	RW	RXSTARTED								Wr	rite	e '1' t	to D	isabl	e ir	nter	upt	for	RXST	ΓAR	TED	eve	nt						
										Se	e E	VEN	TS_	RXS1	AR	TED													
			Clear	1						Dis	sab	ole																	
			Disabled	0						Re	ad	: Disa	able	ed															
			Enabled	1						Re	ad	: Ena	ble	d															
F	RW	TXSTARTED								Wr	rite	e '1' t	to D	isabl	e ir	nter	upt	for	TXST	AR	ΓED	evei	nt						
										Se	e E	VEN	TS_	TXST	AR	TED													
			Clear	1							sab																		



Bit number	31 30 29 28 27 26	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	н	IG FE B A
Reset 0x00000000	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
G RW WRITE		Write '1' to Disable interrupt for WRITE event
		See EVENTS_WRITE
Clear	1	Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
H RW READ		Write '1' to Disable interrupt for READ event
		See EVENTS_READ
Clear	1	Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled

34.9.5 ERRORSRC

Address offset: 0x4D0

Error source

Bit r	numbe	r		31	. 30	29	28	27	26	25	24	23 2:	2 21	20	19	18	17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																														C E	3	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	alue							Desc	ripti	on																		
Α	RW	OVERFLOW										RX b	uffei	ov	erflo	ow (dete	ecte	ed,	and	pre	ver	ted									
			NotDetected	0								Error	did	not	oco	ur																
			Detected	1								Error	occ	urre	ed																	
В	RW	DNACK										NACI	< ser	nt a	fter	rec	eivi	ng a	a da	ita k	yte	:										
			NotReceived	0								Error	did	not	oco	ur																
			Received	1							Error occurred																					
С	RW	OVERREAD										TX bı	uffer	ove	er-r	ead	det	ect	ed,	and	l pr	eve	ntec	I								
			NotDetected	0								Error	did	not	oco	ur																
			Detected	1								Error	occ	urre	ed																	

34.9.6 MATCH

Address offset: 0x4D4

Status register indicating which address had a match

Bitı	numbe	er		31	30	29 :	28 2	27 26	5 25	5 24	23	22	21	20 :	19 1	8 1	7 1	6 15	14	13	12	11	10 !	9 :	3 7	6	5	4	3	2	1 0
Id																															Α
Res	et OxC	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0
ld	RW	Field	Value Id	Value		Description																									
Α	R	MATCH		[0.	1]						W	hich	of t	the	add	ress	es i	n {A	DD	RES	S} n	natc	hed	the	inc	om	ing				
											ad	dres	S																		

34.9.7 ENABLE

Address offset: 0x500

Enable TWIS

Bit	number		31 30 2	9 28 2	7 26	25 2	4 23	22 2	1 2	0 19	18 1	.7 1	6 15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																								A A	A	Α
Res	et 0x00000000		0 0 0	0 (0 0	0 0	0	0 (0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW Field	Value Id	Value				De	scrip	tion	ı																
Α	RW ENABLE			Enable or disable TWIS																						
		Disabled						able																		



	Value Id	Value	Description
ld RW Field	Malica Ial	Value	Description
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id			A A A
Bit number		31 30 29 28 27 20	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

34.9.8 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit r	numbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.9.9 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.9.10 RXD.PTR

Address offset: 0x534 RXD Data pointer

	Bit n	umb	er			31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16 :	15 :	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1 (O
	Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α.	A A	Δ
	Rese	t Ox(000	00000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (o
	ld	RW	F	ield	Value Id	Va	lue							Des	cri	ptic	on																				
ı	Α	RW	Ρ	TR										RXE) Da	ata	poi	nte	r																		_

34.9.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in RXD buffer

Bit	numbe	r		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value	Description
Α	RW	MAXCNT			Maximum number of bytes in RXD buffer

34.9.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last RXD transaction



Bit r	numbe	er		31	30 2	29	28 2	27 2	6 2	25 2	24 2	23 2	2 2	1 20	0 19	9 18	3 17	' 16	15	14	13	12 :	1 10	9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0 (0 (0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						1	Des	crip	tion	,																	
Α	R	AMOUNT									ı	Nun	nber	of	byt	es t	ran	sfer	red	in t	he l	ast	RXD	trar	ısad	ctio	ı					

34.9.13 TXD.PTR

Address offset: 0x544
TXD Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Dit Humber		31 30 23 26 27 20 23 24 23 22 21 20 13 16 17 16 13 14 13 12 11 16 3 6 7 6 7 6 3 4 3 2 1 6
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x0000	000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Fie	d Value Id	Value Description
A RW PT		TXD Data pointer

34.9.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in TXD buffer

Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW MAXCNT		Maximum number of bytes in TXD buffer

34.9.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last TXD transaction

Bit r	iumbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	.0 9	8	7	6	5	4	3	2	1 0
Id																											Α	Α	Α	Α	A	Δ.	A A
Rese	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alu	•						De	scri	otic	on																		
Α	R	AMOUNT										Nu	mbe	er c	of by	yte	s tra	ansi	ferr	ed	in t	ne I	ast	TXE	tra	nsa	ctio	า					

34.9.16 ADDRESS[0]

Address offset: 0x588 TWI slave address 0

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААААА
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW ADDRESS			TWI slave address

34.9.17 ADDRESS[1]

Address offset: 0x58C TWI slave address 1

Bit	numbe	er		31	30 2	9 2	28 27	7 26	25	24	23	22	21 2	20 :	19 1	8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																											Α	Α.	Α.	ДД	АА	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	cri	otio	n																		

RW ADDRESS TWI slave address



34.9.18 CONFIG

Address offset: 0x594

Configuration register for the address match mechanism

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	10 9	9 8	3 7	6	5	4	3	2	1 0
Id																																	3 A
Res	et OxO	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0 (0 (0 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	ADDRESS0										Ena	able	or	dis	abl	e a	ddr	ess	ma	tch	ing	on i	٩DD	RES	SS[0]						
			Disabled	0								Dis	abl	ed																			
			Enabled	1								Ena	able	ed																			
В	RW	ADDRESS1										Ena	able	or	dis	abl	e a	ddr	ess	ma	tch	ing	on i	ADD	RES	SS[1]						
			Disabled	0								Dis	abl	ed																			
			Enabled	1								Ena	ble	ed																			

34.9.19 ORC

Address offset: 0x5C0

Over-read character. Character sent out in case of an over-read of the transmit buffer.

Bit	numbe	er		3	1 30	29	28	27 2	6 2	5 2	4 2	3 22	21	20	19	18 1	17 1	L6 1	.5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																										Α	Α	Α	Α	A A	. Α	A
Res	et 0x0	0000000		0	0	0	0	0 0) (0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	٧	alue	:					D	escr	ipti	on																		
Α	RW	ORC									0	ver-	read	d ch	ara	cter	. Cł	nara	cte	r se	nt o	ut i	n ca	se o	of a	n o	ver-	rea	d			
											0	fthe	tra	ncn	nit k	uiffe	ar															

34.10 Electrical Specification

34.10.1 TWIS slave interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIS}	Bit rates for TWIS ³⁰	100		400	kbps
I _{TWIS,100kbps}	Run current for TWIS (Average current to receive and transfer a		45		μΑ
	byte to RAM), 100 kbps				
I _{TWIS,400kbps}	Run current for TWIS (Average current to receive and transfer a		45		μΑ
	byte to RAM), 400 kbps				
I _{TWIS,IDLE}	Idle current for TWIS		1		μΑ
t _{TWIS,START,LP}	Time from PREPARERX/PREPARETX task to ready to receive/		t _{TWIS,START}	г,	μs
	transmit, Low power mode		+		
			t _{START_HFI}	V	
t _{TWIS,START,CL}	Time from PREPARERX/PREPARETX task to ready to receive/		1.5		μs
	transmit, Constant latency mode				

34.10.2 TWIS slave timing specifications

	B 14	2.01	_		
Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIS,SCL,400kbps}	SCL clock frequency, 400 kbps			400	kHz
t _{TWIS,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWIS,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWIS,HD_STA,100kbps}	TWI slave hold time from for START condition (SDA low to SCL	5200			ns
	low), 100 kbps				
t _{TWIS,HD_STA,400kbps}	TWI slave hold time from for START condition (SDA low to SCL	1300			ns
	low), 400 kbps				

Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWIS,SU_STO,100kbps}	TWI slave setup time from SCL high to STOP condition, 100 kbps	5200			ns
t _{TWIS,SU_STO,400kbps}	TWI slave setup time from SCL high to STOP condition, 400 kbps	1300			ns
t _{TWIS,BUF,100kbps}	TWI slave bus free time between STOP and START conditions,		4700		ns
	100 kbps				
t _{TWIS,BUF,400kbps}	TWI slave bus free time between STOP and START conditions,		1300		ns
	400 khns				

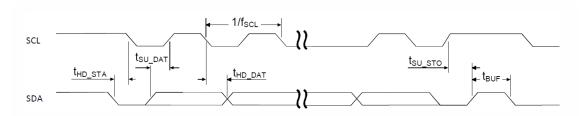


Figure 91: TWIS timing diagram, 1 byte transaction



35 UARTE — Universal asynchronous receiver/ transmitter with EasyDMA

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

Listed here are the main features for UARTE:

- Full-duplex operation
- · Automatic hardware flow control
- Parity checking and generation for the 9th data bit
- EasyDMA
- Up to 1 Mbps baudrate
- · Return to IDLE between transactions supported (when using HW flow control)
- One stop bit
- Least significant bit (LSB) first

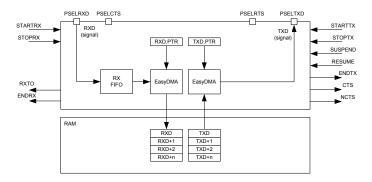


Figure 92: UARTE configuration

The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

35.1 Shared resources

The UARTE shares registers and other resources with other peripherals that have the same ID as the UARTE.

Therefore, you must disable all peripherals that have the same ID as the UARTE before the UARTE can be configured and used. Disabling a peripheral that has the same ID as the UARTE will not reset any of the registers that are shared with the UARTE. It is therefore important to configure all relevant UARTE registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

35.2 EasyDMA

The UARTE implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.



The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The ENDRX/ENDTX event indicates that EasyDMA has finished accessing respectively the RX/TX buffer in RAM.

35.3 Transmission

The first step of a DMA transmission is storing bytes in the transmit buffer and configuring EasyDMA. This is achieved by writing the initial address pointer to TXD.PTR, and the number of bytes in the RAM buffer to TXD.MAXCNT. The UARTE transmission is started by triggering the STARTTX task.

When all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have been transmitted, the UARTE transmission will end automatically and an ENDTX event will be generated.

A UARTE transmission sequence is stopped by triggering the STOPTX task, a TXSTOPPED event will be generated when the UARTE transmitter has stopped.

If the ENDTX event has not already been generated when the UARTE transmitter has come to a stop, the UARTE will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

If flow control is enabled, a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 93: UARTE transmission* on page 330. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

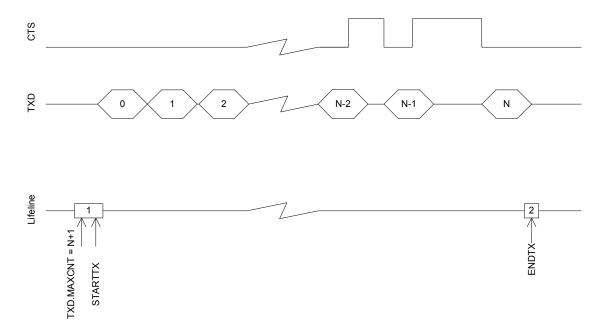


Figure 93: UARTE transmission

The UARTE transmitter will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTTX or after it has been stopped via STOPTX and the TXSTOPPED event has been generated. See *POWER* — *Power supply* on page 76 for more information about power modes.

35.4 Reception

The UARTE receiver is started by triggering the STARTRX task. The UARTE receiver is using EasyDMA to store incoming data in an RX buffer in RAM.



The RX buffer is located at the address specified in the RXD.PTR register. The RXD.PTR register is double-buffered and it can be updated and prepared for the next STARTRX task immediately after the RXSTARTED event is generated. The size of the RX buffer is specified in the RXD.MAXCNT register and the UARTE will generate an ENDRX event when it has filled up the RX buffer, see *Figure 94: UARTE reception* on page 331.

The RXD.AMOUNT register can be queried following an ENDRX event to see how many new bytes have been transferred to the RX buffer in RAM since the previous ENDRX event.

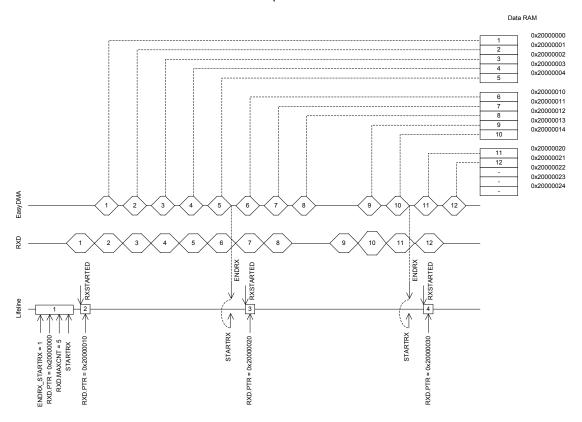


Figure 94: UARTE reception

The UARTE receiver is stopped by triggering the STOPRX task. An RXTO event is generated when the UARTE has stopped. The UARTE will make sure that an impending ENDRX event will be generated before the RXTO event is generated. This means that the UARTE will guarantee that no ENDRX event will be generated after RXTO, unless the UARTE is restarted or a FLUSHRX command is issued after the RXTO event is generated.

Important: If the ENDRX event has not already been generated when the UARTE receiver has come to a stop, which implies that all pending content in the RX FIFO has been moved to the RX buffer, the UARTE will generate the ENDRX event explicitly even though the RX buffer is not full. In this scenario the ENDRX event will be generated before the RXTO event is generated.

To be able to know how many bytes have actually been received into the RX buffer, the CPU can read the RXD.AMOUNT register following the ENDRX event or the RXTO event.

The UARTE is able to receive up to four bytes after the STOPRX task has been triggered as long as these are sent in succession immediately after the RTS signal is deactivated. This is possible because after the RTS is deactivated the UARTE is able to receive bytes for an extended period equal to the time it takes to send 4 bytes on the configured baud rate.

After the RXTO event is generated the internal RX FIFO may still contain data, and to move this data to RAM the FLUSHRX task must be triggered. To make sure that this data does not overwrite data in the RX buffer, the RX buffer should be emptied or the RXD.PTR should be updated before the FLUSHRX task is triggered. To make sure that all data in the RX FIFO is moved to the RX buffer, the RXD.MAXCNT register must be set to RXD.MAXCNT > 4, see *Figure 95: UARTE reception with forced stop via STOPRX* on page 332. The UARTE will generate the ENDRX event after completing the FLUSHRX task even if the RX FIFO was empty



or if the RX buffer does not get filled up. To be able to know how many bytes have actually been received into the RX buffer in this case, the CPU can read the RXD.AMOUNT register following the ENDRX event.

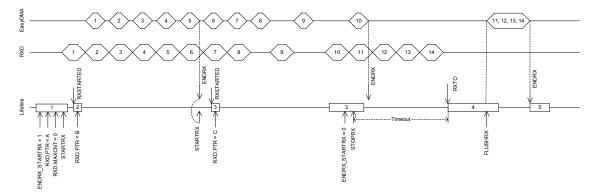


Figure 95: UARTE reception with forced stop via STOPRX

If HW flow control is enabled the RTS signal will be deactivated when the receiver is stopped via the STOPRX task or when the UARTE is only able to receive four more bytes in its internal RX FIFO.

With flow control disabled, the UARTE will function in the same way as when the flow control is enabled except that the RTS line will not be used. This means that no signal will be generated when the UARTE has reached the point where it is only able to receive four more bytes in its internal RX FIFO. Data received when the internal RX FIFO is filled up, will be lost.

The UARTE receiver will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTRX or after it has been stopped via STOPRX and the RXTO event has been generated. See *POWER — Power supply* on page 76 for more information about power modes.

35.5 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

An ERROR event will not stop reception. If the error was a parity error, the received byte will still be transferred into Data RAM, and so will following incoming bytes. If there was a framing error (wrong stop bit), that specific byte will NOT be stored into Data RAM, but following incoming bytes will.

35.6 Using the UARTE without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

35.7 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

35.8 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.



The STOPTX and STOPRX tasks may not be always needed (the peripheral might already be stopped), but if STOPTX and/or STOPRX is sent, software shall wait until the TXSTOPPED and/or RXTO event is received in response, before disabling the peripheral through the ENABLE register.

35.9 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UARTE are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.RTS, and PSEL.TXD registers respectively.

The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UARTE is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.RTS and PSEL.TXD must only be configured when the UARTE is disabled.

To secure correct signal levels on the pins by the UARTE when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Table 76: GPIO configuration before enabling peripheral* on page 333.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 76: GPIO configuration before enabling peripheral

UARTE signal	UARTE pin	Direction	Output value	Comments
RXD	As specified in PSEL.RXD	Input	Not applicable	
CTS	As specified in PSEL.CTS	Input	Not applicable	
RTS	As specified in PSEL.RTS	Output	1	
TXD	As specified in PSEL.TXD	Output	1	

35.10 Registers

Table 77: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40002000	UARTE	UARTE0	Universal Asynchronous Receiver/	
			Transmitter with EasyDMA	

Table 78: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_FLUSHRX	0x02C	Flush RX FIFO into RX buffer
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_ENDRX	0x110	Receive buffer is filled up
EVENTS_ENDTX	0x120	Last TX byte transmitted
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
EVENTS_RXSTARTED	0x14C	UART receiver has started
EVENTS_TXSTARTED	0x150	UART transmitter has started
EVENTS_TXSTOPPED	0x158	Transmitter stopped
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART



Register	Offset	Description
PSEL.RTS	0x508	Pin select for RTS signal
PSEL.TXD	0x50C	Pin select for TXD signal
PSEL.CTS	0x510	Pin select for CTS signal
PSEL.RXD	0x514	Pin select for RXD signal
BAUDRATE	0x524	Baud rate
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
CONFIG	0x56C	Configuration of parity and hardware flow control

35.10.1 SHORTS

Address offset: 0x200 Shortcut register

	numbe	er		31	1 30	29	28	27	26 2	25 2	4 23	22	21 2	20 1	L9 1	8 1	7 1	6 1	5 1	4 13	3 1	2 1:	1 10	9	8				4 3	3 2	1	0
Id																											D	С				
Res	et 0x0	0000000		0	0	0	0	0	0 (0 0	0	0	0	0	0 () (0) () (0	(0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	alue						De	scri	ptio	n																		
С	RW	ENDRX_STARTRX									Sh	orto	ut b	etw	/eer	EN	IDR:	X e	ven	t ar	nd S	TAI	RTR	X ta	sk							
											Se	e <i>E</i> l	/ENT	S_E	ND	RX	and	TA	SKS	_57	AR	TRX										
			Disabled	0							Di	sabl	e sh	orto	cut																	
			Enabled	1							En	able	sho	rtc	ut																	
D	RW	ENDRX_STOPRX									Sh	orto	ut b	etw	/eer	EN	IDR:	X e	ven	t ar	nd S	TOI	PRX	tasl	k							
											Se	e <i>E</i> l	/ENT	S_E	ND	RX	and	TA	SKS	_57	OP	RX										
			Disabled	0							Di	sabl	e sh	orto	ut																	
			Enabled	1							En	able	sho	rtc	ut																	

35.10.2 INTEN

Address offset: 0x300 Enable or disable interrupt

	iumbe	er		31	. 30	29	28 2	2/.	26 2	5 2	4 23	3 22						15	14	13	12 1	1 10			7	6 5		3		L 0
Id												J	H	1 (3	F							Ε	D			С		В	3 A
Res	et 0x0	0000000		0	0	0	0	0	0 0	0	0	0	0 0) (0	0	0	0	0	0	0 (0	0	0	0	0 0	0	0	0 0	0 (
Id	RW	Field	Value Id	Va	lue						De	escri	ptior	1																
Α	RW	CTS									En	able	or d	lisal	ble i	inte	errup	ot fo	or C	TS e	vent									
											Se	e <i>EV</i>	ENT	s_ <i>c</i>	TS															
			Disabled	0							Dis	sable	9																	
			Enabled	1							En	able	!																	
В	RW	NCTS									En	able	or d	lisal	ble i	inte	errup	ot fo	or N	CTS	evei	nt								
											Se	e <i>EV</i>	ENT	S_ N	ICTS	•														
			Disabled	0							Dis	sable	9																	
			Enabled	1							En	able																		
С	RW	ENDRX									En	able	or d	lisal	ble i	inte	errup	ot fo	or E	NDR	X ev	ent								
											Se	e <i>EV</i>	ENT	S_ <i>E</i>	NDF	RX														
			Disabled	0							Dis	sable	9																	
			Enabled	1							En	able	!																	
D	RW	ENDTX									En	able	or d	lisal	ble i	inte	errup	ot fo	or E	NDT	X ev	ent								
											Se	e <i>EV</i>	ENT	S_ <i>E</i>	NDT	ΓX														
			Disabled	0							Dis	sable	9																	
			Enabled	1							En	able																		



Bitı	numbe	er		31 30	0 29	9 28	3 27	26 2	25 2	24 2	3 22	2 2:	1 20	0 19	9 18	3 17	16	15	14	13 1	2 1	1 10	9	8	7	6 5	5 4	3	2	1	0
Id											J		Н	l G		F							Ε	D			(В	А
Res	et 0x0	0000000		0 0	0	0	0	0	0	0 0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 () (0	0	0	0
Id	RW	Field	Value Id	Valu	е					D	esci	ript	tion	1																	
Ε	RW	ERROR								Ei	nab	le c	or d	isab	le i	nte	rrup	t fo	r ER	ROI	R ev	ent									
										Se	ee E	EVE	NTS	5_ <i>EF</i>	RRO)R															
			Disabled	0						D	isab	ble																			
			Enabled	1						E	nab	le																			
F	RW	RXTO								Ei	nab	le c	or d	isab	le i	nte	rrup	t fo	r RX	то	eve	nt									
										Se	ee <i>E</i>	EVE	NTS	_R)	хто)															
			Disabled	0						D	isab	ble																			
			Enabled	1						Ei	nab	le																			
G	RW	RXSTARTED								Ei	nab	le c	or d	isab	le i	nte	rrup	t fo	r RX	STA	RTE	D ev	ent								
										Se	ee E	EVE	NTS		KSTA	ART	ED														
			Disabled	0						D	isab	ble																			
			Enabled	1						Ei	nab	le																			
Н	RW	TXSTARTED								Ei	nab	le o	or d	isab	le i	nte	rrup	t fo	r TX	STA	RTE	D ev	ent								
										Se	ee <i>E</i>	EVE	NTS		(STA	4RT	ED														
			Disabled	0						D	isab	ble																			
			Enabled	1						Ei	nab	le																			
J	RW	TXSTOPPED								Ei	nab	le c	or d	isab	le i	nte	rrup	t fo	r TX	STC	PPE	D ev	ent/								
										Se	ee <i>E</i>	EVE	NTS		(ST	OPP	ED														
			Disabled	0							isab			_																	
			Enabled	1						Ei	nab	le																			
			Enabled	1						Eı	nab	le																			

35.10.3 INTENSET

Address offset: 0x304

Enable interrupt

Dit mount on		21 20 20 20 27 27	C 25 24 22 22 24 20 40 40 47 40 45 44 42 42 44 40 0 0 7 6 5 4 2 2 4 0
Bit number		31 30 29 28 27 26	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			J H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0	
Id RW Field	Value Id	Value	Description
A RW CTS			Write '1' to Enable interrupt for CTS event
			See EVENTS_CTS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW NCTS			Write '1' to Enable interrupt for NCTS event
			See EVENTS_NCTS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW ENDRX			Write '1' to Enable interrupt for ENDRX event
			See EVENTS_ENDRX
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW ENDTX			Write '1' to Enable interrupt for ENDTX event
			·
	Cat	1	See EVENTS_ENDTX Enable
	Set Disabled	1	Enable Read: Disabled
		0	
5 800 5000	Enabled	1	Read: Enabled
E RW ERROR			Write '1' to Enable interrupt for ERROR event



Bitı	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			J H G F E D C B
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
			See EVENTS_ERROR
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
F	RW RXTO		Write '1' to Enable interrupt for RXTO event
			See EVENTS_RXTO
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
G	RW RXSTARTED		Write '1' to Enable interrupt for RXSTARTED event
			See EVENTS_RXSTARTED
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
Н	RW TXSTARTED		Write '1' to Enable interrupt for TXSTARTED event
			See EVENTS_TXSTARTED
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
J	RW TXSTOPPED		Write '1' to Enable interrupt for TXSTOPPED event
			See EVENTS_TXSTOPPED
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled

35.10.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		31 30 23 20 27 20 23 24	J H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	
	Value Id	Value	Description Description
A RW CTS	value lu	value	Write '1' to Disable interrupt for CTS event
A RW CIS			write 1 to bisable interrupt for C13 event
			See EVENTS_CTS
	Clear	1	Disable
1	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW NCTS			Write '1' to Disable interrupt for NCTS event
			See EVENTS_NCTS
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW ENDRX	Litablea	-	Write '1' to Disable interrupt for ENDRX event
C INV ENDINA			Write 1 to bisable interrupt for ENDIA event
			See EVENTS_ENDRX
(Clear	1	Disable
ı	Disabled	0	Read: Disabled
ı	Enabled	1	Read: Enabled
D RW ENDTX			Write '1' to Disable interrupt for ENDTX event
			See EVENTS_ENDTX
	Clear	1	Disable
	Cicai	1	Disable



Reset 0x00000000	Bit r	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value to Disabled 0 Read: Disabled E RW Enabled 1 Read: Disabled E RW ERROR Write "1" to Disable interrupt for ERROR event See EVENTS_ERROR See EVENTS_ERROR Clear 1 Disable Disabled 0 Read: Disabled E RW RXTO Write "1" to Disable interrupt for RXTO event See EVENTS_RXTO See EVENTS_RXTO Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled G RW RXSTARTED See EVENTS_RXTARTED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled H RW TXSTARTED TXSTARTED Clear 1 Disable Disabled 0 Read: Enabled J RW TXSTARTED TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled J Read: Enabled Read: Enabled J Read: Enabled Read: Enabled J <t< td=""><td>Id</td><td></td><td></td><td></td><td>J H G F E D C B A</td></t<>	Id				J H G F E D C B A
Disabled Enabled 1	Rese	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Enabled 1 Read: Enabled E RW ERROR Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RW RXTO Clear 1 Disable Disabled 1 Read: Enabled F RW RXTO Clear 1 Disable Disabled 0 Read: Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RW RXTO Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RXTO Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RXTO Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled F RXTO Clear 1 Disable Disabled 0 Read: Disable Enabled 1 Read: Enabled F RAW TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled F READ: TXSTARTED Clear 1 Read: Enabled F READ: TXSTOPPED Clear 1 Disable Enabled Clear 1 Disable Enabled F READ: TXSTOPPED	Id	RW Field	Value Id	Value	Description
E RW ERROR Clear			Disabled	0	Read: Disabled
Clear 1 Disabled Enabled 1 Read: Enabled F RW RXTO Clear 1 Disabled Clear 1 Clear Clear 1 Disabled Enabled 1 Read: Enabled F RW RXTO Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Clear 1 Read: Enabled F RW RXTO Clear 1 Read: Enabled G RW RXSTARTED Clear 1 Disable Clear 1 Disable Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Clear 1 Disabled Enabled 1 Read: Enabled Clear 1 Disabled Enabled 0 Read: Disabled Enabled 1 Read: Enabled F RW TXSTARTED Clear 1 Disabled Enabled 1 Read: Enabled Clear 1 Read: Enabled F Read: Enabled Clear 1 Disabled Enabled 1 Read: Enabled F Read: Enabled Clear 1 Disabled Enabled 1 Read: Enabled F Read			Enabled	1	Read: Enabled
Clear 1 Disable Read: Disabled Read: Disabled Read: Disabled Read: Enabled Read: Disabled interrupt for RXTO event See EVENTS_RXTO Clear 1 Disabled Read: Enabled Read: Enabled Read: Enabled Read: Enabled Read: Enabled Read: Disabled Read: Enabled Read: Disabled Read: Disabled Read: Enabled Read: Disabled Read: Disabled Read: Enabled Read: Disabled Read: Enabled Read: Enabled Read: Disabled Read: Disabled Read: Disabled Read: Disabled Read: Disabled	Ε	RW ERROR			Write '1' to Disable interrupt for ERROR event
Clear 1 Disable Read: Disabled Read: Disabled Read: Disabled Read: Enabled Read: Disabled interrupt for RXTO event See EVENTS_RXTO Clear 1 Disabled Read: Enabled Read: Enabled Read: Enabled Read: Enabled Read: Enabled Read: Disabled Read: Enabled Read: Disabled Read: Disabled Read: Enabled Read: Disabled Read: Disabled Read: Enabled Read: Disabled Read: Enabled Read: Enabled Read: Disabled Read: Disabled Read: Disabled Read: Disabled Read: Disabled					See EVENTS ERROR
F RW RXTO Clear Disabled Disable Disabled			Clear	1	——————————————————————————————————————
F RW RXTO Clear 1 Disable Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled G RW RXSTARTED Clear 1 Disable Enabled 0 Read: Disable interrupt for RXSTARTED event See EVENTS_RXSTARTED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for RXSTARTED event See EVENTS_RXSTARTED Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for TXSTARTED event See EVENTS_TXSTARTED Write '1' to Disable interrupt for TXSTARTED event See EVENTS_TXSTARTED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for TXSTOPPED event See EVENTS_TXSTOPPED Clear 1 Read: Enabled Write '1' to Disable interrupt for TXSTOPPED event See EVENTS_TXSTOPPED Clear 1 Disable Read: Disable OR Read: Disable Read: Disable Read: Disable			Disabled	0	Read: Disabled
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Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for RXSTARTED event See EVENTS_RXSTARTED Clear 1 Disable Enabled 1 Read: Enabled H RW TXSTARTED Clear 1 Read: Enabled TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for TXSTARTED event See EVENTS_TXSTARTED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for TXSTARTED event See EVENTS_TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for TXSTOPPED event See EVENTS_TXSTOPPED Clear 1 Disable Clear 1 Disable Read: Enabled Write '1' to Disable interrupt for TXSTOPPED event See EVENTS_TXSTOPPED Clear 1 Disable Read: Disabled	F	RW RXTO			Write '1' to Disable interrupt for RXTO event
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Disabled 0 Read: Disabled Enabled 1 Read: Enabled GRW RXSTARTED Clear 1 Disable Enabled 1 Read: Enabled Clear 1 Disable Enabled 1 Read: Disable Enabled 1 Read: Enabled HRW TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled Fixed Disable interrupt for TXSTARTED Clear 1 Disable Read: Disable interrupt for TXSTARTED Clear 1 Disable Enabled 1 Read: Enabled Fixed Disable Enabled Fixed Disable Enabled Fixed Disable Enabled Fixed Disable Enabled Clear 1 Disable Enabled 1 Read: Enabled Fixed Disable interrupt for TXSTOPPED Clear 1 Disable Fixed Disable Enabled Fixed Disable Enabled Fixed Disable Enabled Read: Disable Enabled Read: Disable Enabled Fixed Disable Enabled Read: Disable Clear 1 Disable Read: Disabled Read: Disabled			Clear	1	-
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Enabled 1 Read: Enabled H RW TXSTARTED Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled J RW TXSTOPPED Clear 1 Disable Enabled 1 Read: Enabled Finabled 1 Read: Enabled Disable Disable interrupt for TXSTOPPED Write '1' to Disable interrupt for TXSTOPPED Clear 1 Disable Clear 1 Disable Read: Disabled					
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Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled J RW TXSTOPPED Write '1' to Disable interrupt for TXSTOPPED event See EVENTS_TXSTOPPED Clear 1 Disable Disabled 0 Read: Disabled	П	KW IXSTANTED			write 1 to disable interrupt for TASTAKTED event
Disabled 0 Read: Disabled Enabled 1 Read: Enabled J RW TXSTOPPED Clear 1 Disable Disabled 0 Read: Disabled					_
Enabled 1 Read: Enabled J RW TXSTOPPED Write '1' to Disable interrupt for TXSTOPPED event See EVENTS_TXSTOPPED Clear 1 Disable Disabled 0 Read: Disabled					
J RW TXSTOPPED Write '1' to Disable interrupt for TXSTOPPED event See EVENTS_TXSTOPPED Clear 1 Disable Disabled 0 Read: Disabled					
See EVENTS_TXSTOPPED Clear 1 Disable Disabled 0 Read: Disabled			Enabled	1	
Clear 1 Disable Disabled 0 Read: Disabled	J	RW TXSTOPPED			Write '1' to Disable interrupt for TXSTOPPED event
Disabled 0 Read: Disabled					See EVENTS_TXSTOPPED
			Clear	1	Disable
			Disabled	0	Read: Disabled
Enabled 1 Read: Enabled			Enabled	1	Read: Enabled

35.10.5 ERRORSRC

Address offset: 0x480

Error source

Bit	numbe	er		31	30	29	28	27	26 2	5 24	4 23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4 3	3 2	1	0
Id																													[) C	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						De	escri	ptic	on																		
Α	RW	OVERRUN									Ov	/erru	ın e	rro	r																	_
											A s	start	t bit	is r	ece	ive	d w	hile	e th	e p	revi	ous	dat	a sti	II lie	es in	RX	D.				
											(Pr	revi	ous	dat	a is	los	t.)															
			NotPresent	0							Re	ad:	erro	or n	ot p	ores	sen	t														
			Present	1							Re	ad:	erro	or p	res	ent																
В	RW	PARITY									Pa	rity	erro	or																		
											Αc	char	acte	er w	vith	ba	d pa	arit	y is	rec	eive	d, i	f HV	V pa	rity	che	eck i	is				
											en	able	ed.																			
			NotPresent	0							Re	ad:	erro	or n	ot p	ores	sen	t														
			Present	1							Re	ad:	erro	or p	res	ent																
С	RW	FRAMING									Fra	amir	ng e	rro	r oc	cur	red															
											A۷	valid	sto	p b	it is	s no	ot d	ete	cte	o b	the	e se	rial	data	inp	out	afte	r all				
											bit	ts in	a cl	hara	acte	er h	ave	be	en	rec	eive	d.										
			NotPresent	0							Re	ad:	erro	or n	ot p	ores	sen	t														
			Present	1							Re	ad:	erro	or p	res	ent																



Bit r	numbe	er		31 30	29	28	3 27	26	25	24	23 :	22	21 2	0 1	9 1	8 1	7 16	5 15	14	13	12	11 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																													D (СВ	3 A
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Valu	9					ı	Des	scri	ptio	า																	
D	RW	BREAK								ı	Bre	ak	cond	litio	n																
											The	e se	rial c	lata	a inp	out	is '0	' fo	r loı	ngei	tha	n th	e ler	gth	of	a da	ata				
										1	frar	me.	(The	e da	ata f	ran	ne le	engi	th is	10	bits	with	out	par	ity	bit,	and	ł			
										:	11 l	bits	with	n pa	arity	/ bit	.).														
			NotPresent	0							Rea	ad:	erro	r no	ot pr	ese	nt														
			Present	1						ı	Rea	ad:	erro	pr	ese	nt															

35.10.6 ENABLE

Address offset: 0x500

Enable UART

Bitı	numb	er			3	1 30	29	28	3 27	26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id																																	A A	4 Δ	АА
Res	et 0x	0000	0000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	/ Fie	ld	Value Id	٧	alue	2						De	escri	ipti	on																			
Α	RW	EN.	ABLE										En	able	e or	dis	able	e U	ART	Έ															
				Disabled	0								Di	sabl	e U	AR1	Έ																		
				Enabled	8								En	able	e U	٩RT	E																		

35.10.7 PSEL.RTS

Address offset: 0x508

Pin select for RTS signal

Bit	numbe	er		31 30 29 28 27 26 25 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.10.8 PSEL.TXD

Address offset: 0x50C Pin select for TXD signal

Bit	numbe	er		31 30 29 28 27 26	5 25 2	4 23	22 2	21 2	0 19	18 3	17 16	5 15	14 1	13 12	11 1	9	8	7	6	5 4	1 3	2	1	0
Id				С																A	A A	Α	Α	Α
Res	et 0xF	FFFFFF		1 1 1 1 1 1	1 1	1 1	1	1 :	1 1	1	1 1	1	1	1 1	1 1	. 1	1	1	1	1 1	۱ 1	1	1	1
Id	RW	Field	Value Id	Value		De	scrip	otio	n															
Α	RW	PIN		[031]		Pir	nun	nbe	r															
С	RW	CONNECT				Co	nnec	ction	า															
			Disconnected	1		Dis	con	nect	t															
			Connected	0		Co	nnec	ct																

35.10.9 PSEL.CTS

Address offset: 0x510 Pin select for CTS signal



Bit r	umbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	t OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.10.10 PSEL.RXD

Address offset: 0x514

Pin select for RXD signal

Bit	numbe	er		31 30	29	28	27	26 2	25 2	24 2	23 2	2 21	20	19	18 1	17 1	6 15	14	13 1	2 11	10	9	8	7	6 !	5 4	1 3	2	1 0
Id				С																						A	A A	Α	A A
Res	et 0xF	FFFFFF		1 1	1	1	1	1	1	1	1 1	l 1	1	1	1	1 1	. 1	1	1 1	1	1	1	1	1	1 :	1 1	l 1	1	1 1
Id	RW	Field	Value Id	Valu	2						Desc	ripti	ion																
Α	RW	PIN		[03	L]					F	Pin r	uml	ber																
С	RW	CONNECT								(Conr	necti	ion																
			Disconnected	1						[Disco	onne	ect																
			Connected	0						(Conr	nect																	

35.10.11 BAUDRATE

Address offset: 0x524

Baud rate

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x04000000		0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW BAUDRATE		Baud-rate
	Baud1200	0x0004F000 1200 baud (actual rate: 1205)
	Baud2400	0x0009D000 2400 baud (actual rate: 2396)
	Baud4800	0x0013B000 4800 baud (actual rate: 4808)
	Baud9600	0x00275000 9600 baud (actual rate: 9598)
	Baud14400	0x003AF000 14400 baud (actual rate: 14401)
	Baud19200	0x004EA000 19200 baud (actual rate: 19208)
	Baud28800	0x0075C000 28800 baud (actual rate: 28777)
	Baud38400	0x009D0000 38400 baud (actual rate: 38369)
	Baud57600	0x00EB0000 57600 baud (actual rate: 57554)
	Baud76800	0x013A9000 76800 baud (actual rate: 76923)
	Baud115200	0x01D60000 115200 baud (actual rate: 115108)
	Baud230400	0x03B00000 230400 baud (actual rate: 231884)
	Baud250000	0x04000000 250000 baud
	Baud460800	0x07400000 460800 baud (actual rate: 457143)
	Baud921600	0x0F000000 921600 baud (actual rate: 941176)
	Baud1M	0x10000000 1Mega baud

35.10.12 RXD.PTR

Address offset: 0x534

Data pointer



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value Description
A RW PTR	Data pointer

35.10.13 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bi	t nı	umbe	er		31	30 2	29 :	28 :	27 2	26 2	25 2	24 2	23 2	22 2	21 2	20 :	19 :	18	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
																																				п
Id																													Α	Α	Α	Α	Α	Α.	Α.	4
							_	_	_	_	_	_	_		_	_	_	_	_				_					_		_				_	_	
R	ese	t OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	נ
			e: 11	V. I I.I.																																
10		KW	Field	Value Id	va	lue							Jes	crip	τιο	n																				
Λ		D\A/	MAXCNT										112	imi	ım	nu	mh	or c	sf h	v+o	c in	·ro	coi	, a k	ff	or										Ξ.
А		L/A/	IVIAACIVI									- 1	vid)	HIII	uill	пu	HID	בו (ט וע	yιe	:> II	пe	CGL	אה ו	Juli	CI.										

35.10.14 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A R AMOUNT		Number of bytes transferred in the last transaction

35.10.15 TXD.PTR

Address offset: 0x544

Data pointer

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 Α	A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. A	. A
Rese	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	PTR		Data pointer																													

35.10.16 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8	8 7 6 5 4 3 2 1
Id					AAAAAA
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	00000000	0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW MAXCNT			Maximum number of	bytes in transmit buffer	

35.10.17 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Id	RW	Field	Value Id	Value	Description										
Re	set 0x	00000000		0 0 0 0 0	0 0 0 0 0 0 0	0 0 0	0 0 0	0 0	0 0 0	0	0 0	0	0 0	0	0 0
Id											A A	Α	A A	Α	A A
Bit	numb	er		31 30 29 28 27 2	26 25 24 23 22 21 20	19 18 17	16 15 14	1 13 12 1	1 10 9	8	7 6	5	4 3	2	1 0

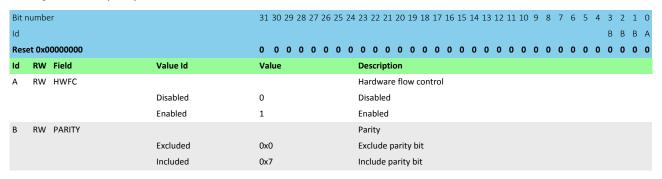
A R AMOUNT Number of bytes transferred in the last transaction



35.10.18 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control



35.11 Electrical Specification

35.11.1 UARTE electrical specification

Symbol	Description	Min.	Тур.	Max.	Units
f _{UARTE}	Baud rate for UARTE ³¹ .			1000	kbps
I _{UARTE1M}	Run current at max baud rate.		55		μΑ
I _{UARTE115k}	Run current at 115200 bps.		55		μΑ
I _{UARTE1k2}	Run current at 1200 bps.		55		μΑ
I _{UARTE,IDLE}	Idle current for UARTE (STARTed, no XXX activity)		1		μΑ
t _{UARTE,CTSH}	CTS high time	1			μs
t _{UARTE,START,LP}	Time from STARTRX/STARTTX task to transmission started, low		t _{UARTE,S}	ΓAR	μs
	power mode		+		
			t _{START_H}	FIN	
t _{UARTE,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1		μs
	constant latency mode				

Higher baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.



36 QDEC — Quadrature decoder

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Decoding of digital waveform from off-chip quadrature encoder.
- Sample accumulation eliminating hard real-time requirements to be enforced on application.
- Optional input de-bounce filters.
- · Optional LED output signal for optical encoders.

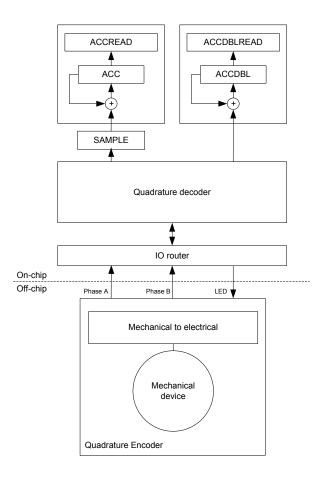


Figure 96: Quadrature decoder configuration

36.1 Sampling and decoding

The QDEC decodes the output from an incremental motion encoder by sampling the QDEC phase input pins (A and B).

The off-chip quadrature encoder is an incremental motion encoder outputting two waveforms, phase A and phase B. The two output waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by which of these two waveforms that changes level first. Invalid transitions may occur, that is when the two waveforms switch simultaneously. This may occur if the wheel rotates too fast relative to the sample rate set for the decoder.



The QDEC decodes the output from the off-chip encoder by sampling the QDEC phase input pins (A and B) at a fixed rate as specified in the SAMPLEPER register.

If the SAMPLEPER value needs to be changed, the QDEC shall be stopped using the STOP task. SAMPLEPER can be then changed upon receiving the STOPPED event, and QDEC can be restarted using the START task. Failing to do so may result in unpredictable behaviour.

It is good practice to change other registers (LEDPOL, REPORTPER, DBFEN and LEDPRE) only when the QDEC is stopped.

When started, the decoder continuously samples the two input waveforms and decodes these by comparing the current sample pair (n) with the previous sample pair (n-1).

The decoding of the sample pairs is described in the table below.

Table 79: Sampled value encoding

Previous sample - 1)	e pair(n	·	les pair(n)	SAMPLE register	ACC operation	ACCDBL operation	Description
Α	В	Α	В				
0	0	0	0	0	No change	No change	No movement
0	0	0	1	1	Increment	No change	Movement in positive direction
0	0	1	0	-1	Decrement	No change	Movement in negative direction
0	0	1	1	2	No change	Increment	Error: Double transition
0	1	0	0	-1	Decrement	No change	Movement in negative direction
0	1	0	1	0	No change	No change	No movement
0	1	1	0	2	No change	Increment	Error: Double transition
0	1	1	1	1	Increment	No change	Movement in positive direction
1	0	0	0	1	Increment	No change	Movement in positive direction
1	0	0	1	2	No change	Increment	Error: Double transition
1	0	1	0	0	No change	No change	No movement
1	0	1	1	-1	Decrement	No change	Movement in negative direction
1	1	0	0	2	No change	Increment	Error: Double transition
1	1	0	1	-1	Decrement	No change	Movement in negative direction
1	1	1	0	1	Increment	No change	Movement in positive direction
1	1	1	1	0	No change	No change	No movement

36.2 LED output

The LED output follows the sample period, and the LED is switched on a given period before sampling and switched off immediately after the inputs are sampled. The period the LED is switched on before sampling is given in the LEDPRE register.

The LED output pin polarity is specified in the LEDPOL register.

For using off-chip mechanical encoders not requiring a LED, the LED output can be disabled by writing value 'Disconnected' to the CONNECT field of the PSEL.LED register. In this case the QDEC will not acquire access to a LED output pin and the pin can be used for other purposes by the CPU.

36.3 Debounce filters

Each of the two-phase inputs have digital debounce filters.

When enabled through the DBFEN register, the filter inputs are sampled at a fixed 1 MHz frequency during the entire sample period (which is specified in the SAMPLEPER register), and the filters require all of the samples within this sample period to equal before the input signal is accepted and transferred to the output of the filter.

As a result, only input signal with a steady state longer than twice the period specified in SAMPLEPER are guaranteed to pass through the filter, and any signal with a steady state shorter than SAMPLEPER will always be suppressed by the filter. (This is assumed that the frequency during the debounce period never exceeds 500 kHz (as required by the Nyquist theorem when using a 1 MHz sample frequency).

The LED will always be ON when the debounce filters are enabled, as the inputs in this case will be sampled continuously.



Note that when when the debounce filters are enabled, displacements reported by the QDEC peripheral are delayed by one SAMPLEPER period.

36.4 Accumulators

The quadrature decoder contains two accumulator registers, ACC and ACCDBL, that accumulate respectively valid motion sample values and the number of detected invalid samples (double transitions).

The ACC register will accumulate all valid values (1/-1) written to the SAMPLE register. This can be useful for preventing hard real-time requirements from being enforced on the application. When using the ACC register the application does not need to read every single sample from the SAMPLE register, but can instead fetch the ACC register whenever it fits the application. The ACC register will always hold the relative movement of the external mechanical device since the previous clearing of the ACC register. Sample values indicating a double transition (2) will not be accumulated in the ACC register.

An ACCOF event will be generated if the ACC receives a SAMPLE value that would cause the register to overflow or underflow. Any SAMPLE value that would cause an ACC overflow or underflow will be discarded, but any samples not causing the ACC to overflow or underflow will still be accepted.

The accumulator ACCDBL accumulates the number of detected double transitions since the previous clearing of the ACCDBL register.

The ACC and ACCDBL registers can be cleared by the READCLRACC and subsequently read using the ACCREAD and ACCDBLREAD registers.

The ACC register can be separately cleared by the RDCLRACC and subsequently read using the ACCREAD registers.

The ACCDBL register can be separately cleared by the RDCLRDBL and subsequently read using the ACCDBLREAD registers.

The REPORTPER register allows automating the capture of several samples before it can send out a REPORTRDY event in case a non-null displacement has been captured and accumulated, and a DBLRDY event in case one or more double-displacements have been captured and accumulated. The REPORTPER field in this register selects after how many samples the accumulators contents are evaluated to send (or not) REPORTRDY and DBLRDY events.

Using the RDCLRACC task (manually sent upon receiving the event, or using the DBLRDY_RDCLRACC shortcut), ACCREAD can then be read.

In case at least one double transition has been captured and accumulated, a DBLRDY event is sent. Using the RDCLRDBL task (manually sent upon receiving the event, or using the DBLRDY_RDCLRDBL shortcut), ACCDBLREAD can then be read.

36.5 Output/input pins

The QDEC uses a three-pin interface to the off-chip quadrature encoder.

These pins will be acquired when the QDEC is enabled in the ENABLE register. The pins acquired by the QDEC cannot be written by the CPU, but they can still be read by the CPU.

The pin numbers to be used for the QDEC are selected using the PSEL.n registers.

36.6 Pin configuration

The Phase A, Phase B, and LED signals are mapped to physical pins according to the configuration specified in the PSEL.A, PSEL.B, and PSEL.LED registers respectively.

If the CONNECT field value 'Disconnected' is specified in any of these registers, the associated signal will not be connected to any physical pin. The PSEL.A, PSEL.B, and PSEL.LED registers and their configurations are only used as long as the QDEC is enabled, and retained only as long as the device is in



ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN CNF[n] register.

To secure correct behavior in the QDEC, the pins used by the QDEC must be configured in the GPIO peripheral as described in *Table 80: GPIO configuration before enabling peripheral* on page 345 before enabling the QDEC. This configuration must be retained in the GPIO for the selected IOs as long as the QDEC is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 80: GPIO configuration before enabling peripheral

QDEC signal	QDEC pin	Direction	Output value	Comment
Phase A	As specified in PSEL.A	Input	Not applicable	
Phase B	As specified in PSEL.B	Input	Not applicable	
LED	As specified in PSEL.LED	Input	Not applicable	

36.7 Registers

Table 81: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40012000	QDEC	QDEC	Quadrature decoder	

Table 82: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the quadrature decoder
TASKS_STOP	0x004	Task stopping the quadrature decoder
TASKS_READCLRACC	0x008	Read and clear ACC and ACCDBL
TASKS_RDCLRACC	0x00C	Read and clear ACC
TASKS_RDCLRDBL	0x010	Read and clear ACCDBL
EVENTS_SAMPLERDY	0x100	Event being generated for every new sample value written to the SAMPLE register
EVENTS_REPORTRDY	0x104	Non-null report ready
EVENTS_ACCOF	0x108	ACC or ACCDBL register overflow
EVENTS_DBLRDY	0x10C	Double displacement(s) detected
EVENTS_STOPPED	0x110	QDEC has been stopped
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable the quadrature decoder
LEDPOL	0x504	LED output pin polarity
SAMPLEPER	0x508	Sample period
SAMPLE	0x50C	Motion sample value
REPORTPER	0x510	Number of samples to be taken before REPORTRDY and DBLRDY events can be generated
ACC	0x514	Register accumulating the valid transitions
ACCREAD	0x518	Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task
PSEL.LED	0x51C	Pin select for LED signal
PSEL.A	0x520	Pin select for A signal
PSEL.B	0x524	Pin select for B signal
DBFEN	0x528	Enable input debounce filters
LEDPRE	0x540	Time period the LED is switched ON prior to sampling
ACCDBL	0x544	Register accumulating the number of detected double transitions
ACCDBLREAD	0x548	Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

36.7.1 SHORTS

Address offset: 0x200 Shortcut register



Bit	numbe	er		31 30	29 28	27 26	25 24	1 23 22 21	20 19 1	18 17 :	16 15	14 1	3 12	11 10) 9	8 7	6	5	4 3	2	1 ()
Id																	G	F	E C) C	В	
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0	0 0	0 0	0 0	0 (0 0	0 0	0	0 0	0	0	0 0	0	0 ()
Id	RW	Field	Value Id	Value				Description	on													
Α	RW	REPORTRDY_READCLRACG						Shortcut b	betwee	n REPC	ORTRE	Y eve	ent a	nd RE	ADC	LRAC	C tas	sk				
								See EVEN	TS_REP	ORTRE	oy and	TAS	KS_R	EADC	LRAC	CC						
			Disabled	0				Disable sh	nortcut													
			Enabled	1				Enable sho	ortcut													
В	RW	SAMPLERDY_STOP						Shortcut b	betwee	n SAM	PLER	OY ev	ent a	nd ST	OP t	ask						
								See <i>EVEN</i>	TS_SAN	1PLERI	DY and	d TAS	KS_S	TOP								
			Disabled	0				Disable sh	nortcut													
			Enabled	1				Enable sho	ortcut													
С	RW	REPORTRDY_RDCLRACC						Shortcut b	betwee	n REPO	ORTRE	Y eve	ent a	nd RD	CLR	ACC t	ask					
								See <i>EVEN</i>	TS_REP	ORTRE	oy and	t TAS	KS_R	DCLR/	4 <i>CC</i>							
			Disabled	0				Disable sh	nortcut													
			Enabled	1				Enable sho	ortcut													
D	RW	REPORTRDY_STOP						Shortcut b	betwee	n REPO	ORTRE	Y eve	ent a	nd ST	OP t	ask						
								See EVEN	TS_REP	ORTRE	oy and	TAS	KS_S	ТОР								
			Disabled	0				Disable sh	nortcut													
			Enabled	1				Enable sho	ortcut													
Е	RW	DBLRDY_RDCLRDBL						Shortcut b	betwee	n DBLF	RDY ev	ent a	and R	DCLR	DBL	task						
								See <i>EVEN</i>	TS_DBL	<i>RDY</i> aı	nd <i>TA</i> .	SKS_F	RDCL	RDBL								
			Disabled	0				Disable sh	nortcut													
			Enabled	1				Enable sho	ortcut													
F	RW	DBLRDY_STOP						Shortcut b	betwee	n DBLF	RDY ev	ent a	and S	TOP t	ask							
								See EVEN	TS_DBL	<i>RDY</i> aı	nd <i>TA</i> .	SKS_S	STOP									
			Disabled	0				Disable sh	nortcut													
			Enabled	1				Enable sho	ortcut													
G	RW	SAMPLERDY_READCLRAC	C					Shortcut b	betwee	n SAM	PLER	OY ev	ent a	nd RE	ADC	LRAC	C ta	sk				
								See <i>EVEN</i>	TS_SAN	1PLERI	DY and	d <i>TAS</i>	KS_R	EADC	LRA	сс						
			Disabled	0				Disable sh	nortcut													
			Enabled	1				Enable sho	ortcut													

36.7.2 INTENSET

Address offset: 0x304 Enable interrupt

Bit r	number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D C B A
Res	et 0x00000000		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field	Value Id	Value	Description
Α	RW SAMPLERDY			Write '1' to Enable interrupt for SAMPLERDY event
				See EVENTS_SAMPLERDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REPORTRDY			Write '1' to Enable interrupt for REPORTRDY event
				See EVENTS_REPORTRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ACCOF			Write '1' to Enable interrupt for ACCOF event
				See EVENTS_ACCOF
		Set	1	Enable



Bit nur	mber		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D C B A
Reset	0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id R	RW Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D R	RW DBLRDY			Write '1' to Enable interrupt for DBLRDY event
				See EVENTS_DBLRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E R	RW STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

36.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit n	umbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E D C B A
Rese	t 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	SAMPLERDY			Write '1' to Disable interrupt for SAMPLERDY event
					See EVENTS_SAMPLERDY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	REPORTRDY			Write '1' to Disable interrupt for REPORTRDY event
					See EVENTS_REPORTRDY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	ACCOF			Write '1' to Disable interrupt for ACCOF event
					See EVENTS_ACCOF
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	DBLRDY			Write '1' to Disable interrupt for DBLRDY event
					See EVENTS_DBLRDY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	STOPPED			Write '1' to Disable interrupt for STOPPED event
					See EVENTS_STOPPED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

36.7.4 ENABLE

Address offset: 0x500

Enable the quadrature decoder



Bit	numbe	er		31	L 30	29	28	8 27	7 26	5 25	24	4 23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							De	scr	iptio	on																				
Α	RW	ENABLE										En	able	e or	dis	abl	e tl	ne (qua	dra	tur	e d	eco	der											
												W	hen	ena	able	ed t	he	de	cod	er p	oins	s wi	ll be	e ac	tive	. W	her	n di	sab	led					
												the	e qu	uadr	atu	ıre	dec	od	er p	oins	ar	e no	ot a	ctiv	e ar	nd c	an	be	use	d a	S				
												GP	PIO.																						
			Disabled	0								Dis	sabl	le																					
			Enabled	1								En	able	e																					

36.7.5 LEDPOL

Address offset: 0x504 LED output pin polarity

Bit	numbe	er		31 3	0 29	28	27	26	25	24	23 2	22 2	21 2	0 19	18	17	16	15 1	L4 1	3 12	2 11	10	9	8	7 6	5 5	4	3	2	1 0
Id																														Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ie						Des	crip	tior	1																
Α	RW	LEDPOL									LED	ou	tput	pin	pola	arity	,													
			ActiveLow	0							Led	act	ive (on o	utpu	ıt pi	n lo	w												
			ActiveHigh	1							Led	act	ive (on o	utpu	ıt pi	n hi	gh												

36.7.6 SAMPLEPER

Address offset: 0x508

Sample period

Bit numbe	er		31	30 2	29 2	8 27	7 26	25	24	23 2	22 21	. 20	19	18	17 1	16 1	15 1	4 13	3 12	11	10	9 :	3 7	6	5	4	3 :	2 1	L 0
Id																											A	4 Α	АА
Reset 0x0	0000000		0	0	0 0	0 0	0	0	0	0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0 (0	0	0	0	0 (0 0	0
ld RW	Field	Value Id	Va	lue						Desc	cripti	ion																	
A RW	SAMPLEPER									Sam	ple p	erio	od. T	he	SAN	/IPL	E re	gist	er w	ill be	up	dat	ed f	or e	very	/			
										new	sam	ple																	
		128us	0							128	us																		
		256us	1							256	us																		
		512us	2							512	us																		
		1024us	3							1024	4 us																		
		2048us	4							2048	8 us																		
		4096us	5							4096	6 us																		
		8192us	6							8192	2 us																		
		16384us	7							1638	84 us	5																	
		32ms	8							3276	68 us	5																	
		65ms	9							6553	36 us	5																	
		131ms	10							1310	072 ι	ıs																	

36.7.7 SAMPLE

Address offset: 0x50C Motion sample value

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16 1	15 1	4 1	3 12	2 1:	1 10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A .	4 4	Α Α	. Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Δ	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	R	SAMPLE		[-1	2]							Las	t m	otio	on s	am	ple																



Id RW Field Va	lue Id Val						Desci																	
Reset 0x00000000	0	0 0	0	0	0	0	0 0	0	0 (0	0	0	0 (0	0	0 (0	0	0	0	0	0 0	0	0 0
Id	А	A A	Α .	4 A	Α	Α .	A A	Α	A A	A A	Α	Α	A A	A A	Α	A A	A A	Α.	Α	Α	Α ,	4 A	Α	A A
Bit number	31	30 29	28 2	7 26	25	24 2	23 22	2 21	20 1	9 18	3 17	16 1	5 1	4 13	12 3	11 1	0 9	8	7	6	5 4	4 3	2	1 0

The value is a 2's complement value, and the sign gives the direction of the motion. The value '2' indicates a double transition.

36.7.8 REPORTPER

Address offset: 0x510

Number of samples to be taken before REPORTRDY and DBLRDY events can be generated

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW REPORTPER		Specifies the number of samples to be accumulated in the ACC
		register before the REPORTRDY and DBLRDY events can be
		generated
		The report period in [us] is given as: RPUS = SP * RP Where
		RPUS is the report period in [us/report], SP is the sample period
		in [us/sample] specified in SAMPLEPER, and RP is the report
		period in [samples/report] specified in REPORTPER .
	10Smpl	0 10 samples / report
	40Smpl	1 40 samples / report
	80Smpl	2 80 samples / report
	120Smpl	3 120 samples / report
	160Smpl	4 160 samples / report
	200Smpl	5 200 samples / report
	240Smpl	6 240 samples / report
	280Smpl	7 280 samples / report
	1Smpl	8 1 sample / report

36.7.9 ACC

Address offset: 0x514

Register accumulating the valid transitions

Bit number		31	30	29 2	28 2	27 2	26 2	25 2	24	23	22 2	21 2	20 :	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4 3	2	1	0
Id		Α	Α	Α	Α	Α.	Α.	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id RW Field V	/alue Id	Val	ue							Des	crip	tio	n																			
A R ACC		[-10	024	10	23]					Reg	iste	r a	ccu	mu	lati	ng	all v	vali	d sa	mp	les	(no	t do	oub	le t	ran	siti	on)				
										rea	d fro	om	the	SA	MF	PLE	reg	giste	er													
										Doi	ıble	+	nci	+io:	ac (CΛ	NAD		- 2		ll n	0+ h		ccu	mu	lati	ad i	_				
										this	reg	iste	er. '	The	va	lue	is a	32	bit	2's	COI	mpl	em	ent	val	ue.	. If a	1				
										sam	nple	tha	at v	vou	ld d	cau	se t	his	reg	iste	r to	o ov	erf	low	or	un	derf	low				
										is re	ecei	ved	l, th	ne s	am	ple	wi	ll be	igr	ore	ed a	and	an	ove	erflo	w	eve	nt				
										(AC	ССО	F) '	will	be	gei	ner	ate	d. 1	he	AC	c re	gist	er i	is cl	ear	ed	by					
										trio	geri	nσ	the	RF	ΔD	CI F	ΔC	C 0	r th	e R	חכו	RΔ	^C 1	tacl	,							

36.7.10 ACCREAD

Address offset: 0x518

Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task



E	3it n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ ,	4 А
F	Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
ı	d	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
-	١	R	ACCREAD		[-1	ი24	10	1231					Sn:	nsl	not	of t	he .	ACC	re	øist	er														

The ACCREAD register is updated when the READCLRACC or RDCLRACC task is triggered

36.7.11 PSEL.LED

Address offset: 0x51C Pin select for LED signal

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

36.7.12 PSEL.A

Address offset: 0x520 Pin select for A signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

36.7.13 PSEL.B

Address offset: 0x524 Pin select for B signal

Bit r	umbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	t OxF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

36.7.14 DBFEN

Address offset: 0x528

Enable input debounce filters



Bit	numbe	er		31 30	29	28 2	27 2	6 2	5 24	23	22	21 2	20 1	9 18	17	16	15	14 13	3 12	11	10 9	8	7	6	5	4	3	2	1 0
Id																													Α
Res	et 0x0	0000000		0 0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0 0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value						De	scri	ptio	n																
Α	RW	DBFEN								En	able	inp	ut d	eboı	unce	e filt	ers												
			Disabled	0						De	bou	nce	inpu	ıt fil	ters	disa	ble	d											
			Enabled	1						De	bou	nce	inpu	ıt fil	ters	ena	ble	d											

36.7.15 LEDPRE

Address offset: 0x540

Time period the LED is switched ON prior to sampling

Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A
Reset 0x00000010		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value	Description
A RW LEDPRE		[1511]	Period in us the LED is switched on prior to sampling

36.7.16 ACCDBL

Address offset: 0x544

Register accumulating the number of detected double transitions

Bit Id	numb	er		31	30 2	29 :	28 2	7 2	26 25	5 24	23	22	21 2	0 1	9 1	8 17	7 16	15	14	13 1	L2 1:	1 10	9	8	7	6	5 4		3 2 A A	-	0 A
Res	et 0x	00000000		0	0	0	0 ()	0 0	0	0	0	0 0) (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ptior	1																	
A	R	ACCDBL		[0.	15]						trai Wh acc ove ille	nsit nen cum erflo gal	er actions. this in the control of t	reg on wen	ister of d at (A ons a	PLE r ha loub ACCO are	= 2 s readle / OF) dete). ache ille will will ecte	ed it gal t I be ed af	s m rans gen	axim sition erate the r	ium ns w ed if nax	valu ill si any mui	ue t top. do m v	he An uble	e or	ıs				

36.7.17 ACCDBLREAD

Address offset: 0x548

Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

Bit	numbe	er		31 30 29 28 27	7 26 25 24	23 22 2	1 20 19	18 1	7 16	15 1	4 13	12 1	11 10	9	8	7	6	5	4	3	2 1	0
Id																				Α .	4 A	A
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	0 0 0	0 0	0 0	0	0	0 0	0	0 0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Value		Descript	tion															
Α	R	ACCDBLREAD		[015]		Snapsho	t of the	ACCE	DBL re	egist	er. T	his fi	eld is	upo	date	ed v	whe	n tl	he			
						READCI	DACC o	r DDCI	DUB	l tac	l ic t	riago	rod									

36.8 Electrical Specification

36.8.1 QDEC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{QDEC}	Run current		5		μΑ
t _{SAMPLE}	Time between sampling signals from quadrature decoder	128		131072	μs
t _{LED}	Time from LED is turned on to signals are sampled	0		511	μs



37 SAADC — Successive approximation analog-todigital converter

The ADC is a differential successive approximation register (SAR) analog-to-digital converter.

Listed here are the main features of SAADC:

- 8/10/12-bit resolution, 14-bit resolution with oversampling
- · Up to eight input channels
 - One channel per single-ended input and two channels per differential input
 - Scan mode can be configured with both single-ended channels and differential channels.
- Full scale input range (0 to VDD)
- Sampling triggered via a task from software or a PPI channel for full flexibility on sample frequency source from low power 32.768kHz RTC or more accurate 1/16MHz Timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence. Sample delay between channels is t_{ack} + t_{conv} which may vary between channels according to user configuration of t_{ack}.
- · Support for direct sample transfer to RAM using EasyDMA
- · Interrupts on single sample and full buffer events
- Samples stored as 16-bit 2's complement values for differential and single-ended sampling
- · Continuous sampling without the need of an external timer
- Internal resistor string
- · Limit checking on the fly

37.1 Shared resources

The ADC can coexist with COMP, LPCOMP and other peripherals using one of AIN0-AIN7, provided these are assigned to different pins.

It is not recommended to select the same analog input pin for both modules.

37.2 Overview

The ADC supports up to eight external analog input channels, depending on package variant. It can be operated in a one-shot mode with sampling under software control, or a continuous conversion mode with a programmable sampling rate.

The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select AIN0 to AIN7 pins, or the VDD pin. Channels can be sampled individually in one-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampled in sequence. Channels can also be oversampled to improve noise performance.



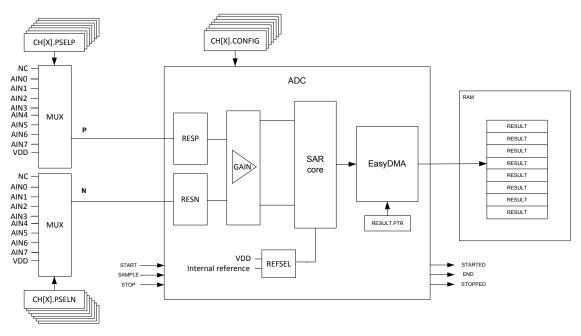


Figure 97: Simplified ADC block diagram

Internally, the ADC is always a differential analog-to-digital converter, but by default it is configured with single-ended input in the MODE field of the CH[n].CONFIG register. In single-ended mode, the negative input will be shorted to ground internally.

The assumption in single-ended mode is that the internal ground of the ADC is the same as the external ground that the measured voltage is referred to. The ADC is thus sensitive to ground bounce on the PCB in single-ended mode. If this is a concern we recommend using differential measurement.

37.3 Digital output

The output result of the ADC depends on the settings in the CH[n].CONFIG and RESOLUTION registers as follows:

```
RESULT = [V(P) - V(N)] * GAIN/REFERENCE * 2 (RESOLUTION - m)
```

where

V(P)

is the voltage at input P

V(N)

is the voltage at input N

GAIN

is the selected gain setting

REFERENCE

is the selected reference voltage

and m=0 if CONFIG.MODE=SE, or m=1 if CONFIG.MODE=Diff.

The result generated by the ADC will deviate from the expected due DC errors like offset, gain, differential non-linearity (DNL), and integral non-linearity (INL). See *Electrical specification* for details on these parameters. The result can also vary due to AC errors like non-linearities in the GAIN block, settling errors due to high source impedance and sampling jitter. For battery measurement the DC errors are most noticeable.



The ADC has a wide selection of gains controlled in the GAIN field of the CH[n].CONFIG register. If CH[n].CONFIG.REFSEL=0, the input range of the ADC core is nominally ± 0.6 V differential and the input must be scaled accordingly.

The ADC has a temperature dependent offset. If the ADC is to operate over a large temperature range, we recommend running CALIBRATEOFFSET at regular intervals, a CALIBRATEDONE event will be fired when the calibration is complete

37.4 Analog inputs and channels

Up to eight analog input channels, CH[n](n=0..7), can be configured.

See Shared resources on page 352 for shared input with comparators.

Any one of the available channels can be enabled for the ADC to operate in one-shot mode. If more than one CH[n] is configured, the ADC enters scan mode.

An analog input is selected as a positive converter input if CH[n].PSELP is set, setting CH[n].PSELP also enables the particular channel.

An analog input is selected as a negative converter input if CH[n].PSELN is set. The CH[n].PSELN register will have no effect unless differential mode is enabled, see MODE field in CH[n].CONFIG register.

If more than one of the CH[n].PSELP registers is set, the device enters scan mode. Input selections in scan mode are controlled by the CH[n].PSELP and CH[n].PSELN registers, where CH[n].PSELN is only used if the particular scan channel is specified as differential, see MODE field in CH[n].CONFIG register.

Important: Channels selected for either COMP or LPCOMP cannot be used at the same time for ADC sampling, though channels not selected for use by these blocks can be used by the ADC.

Table 83: Legal connectivity CH[n] vs. analog input

Channel input	Source	Connectivity
CH[n].PSELP	AINOAIN7	Yes(any)
CH[n].PSELP	VDD	Yes
CH[n].PSELN	AINOAIN7	Yes(any)
CH[n].PSELN	VDD	Yes

37.5 Operation modes

The ADC input configuration supports one-shot mode, continuous mode and scan mode.

Scan mode and oversampling cannot be combined.

37.5.1 One-shot mode

One-shot operation is configured by enabling only one of the available channels defined by CH[n].PSELP, CH[n].PSELN, and CH[n].CONFIG registers.

Upon a SAMPLE task, the ADC starts to sample the input voltage. The CH[n].CONFIG.TACQ controls the acquisition time.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA. For more information, see *EasyDMA* on page 356.

37.5.2 Continuous mode

Continuous sampling can be achieved by using the internal timer in the ADC, or triggering the SAMPLE task from one of the general purpose timers through the PPI.

Care shall be taken to ensure that the sample rate fulfils the following criteria, depending on how many channels are active:

fsample < 1/[tacq + tconv]



The SAMPLERATE register can be used as a local timer instead of triggering individual SAMPLE tasks. When SAMPLERATE.MODE is set to Timers, it is sufficient to trigger SAMPLE task only once in order to start the SAADC and triggering the STOP task will stop sampling. The SAMPLERATE.CC field controls the sample rate.

The SAMPLERATE timer mode cannot be combined with SCAN mode, and only one channel can be enabled in this mode.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

37.5.3 Oversampling

An accumulator in the ADC can be used to average noise on the analog input. In general, oversampling improves the signal-to-noise ratio (SNR). Oversampling, however, does not improve the integral non-linearity (INL), or differential non-linearity (DNL).

Oversampling and scan should not be combined, since oversampling and scan will average over input channels.

The accumulator is controlled in the OVERSAMPLE register. The SAMPLE task must be set 2^{OVERSAMPLE} number of times before the result is written to RAM. This can be achieved by:

- Configuring a fixed sampling rate using the local timer or a general purpose timer and PPI to trigger a SAMPLE task
- Triggering SAMPLE 2^{OVERSAMPLE} times from software
- · Enabling BURST mode

CH[n].CONFIG.BURST can be enabled to avoid setting SAMPLE task $2^{\text{OVERSAMPLE}}$ times. With BURST = 1 the ADC will sample the input $2^{\text{OVERSAMPLE}}$ times as fast as it can (actual timing: $<(t_{\text{ACQ}}+t_{\text{CONV}})\times 2^{\text{OVERSAMPLE}})$. Thus, for the user it will just appear like the conversion took a bit longer time, but other than that, it is similar to one-shot mode. Scan mode can be combined with BURST=1, if burst is enabled on all channels.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals that enough conversions have taken place for an oversampled result to get transferred into RAM. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

37.5.4 Scan mode

A channel is considered enabled if CH[n].PSELP is set. If more than one channel, CH[n], is enabled, the ADC enters scan mode.

In scan mode, one SAMPLE task will trigger one conversion per enabled channel. The time it takes to sample all channels is:

```
Total time < Sum (CH[x].t<sub>ACO</sub>+t<sub>CONV</sub>), x=0..enabled channels
```

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual values have been transferred into RAM by EasyDMA.

Figure 98: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 356 provides an example of results placement in Data RAM, with an even RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled.



	31 16	15 0
RESULT.PTR	CH[2] 1 st result	CH[1] 1 st result
RESULT.PTR + 4	CH[1] 2 nd result	CH[5] 1 st result
RESULT.PTR + 8	CH[5] 2 nd result	CH[2] 2 nd result
	(.)
RESULT.PTR + 2*(RESULT.MAXCNT – 2)	CH[5] last result	CH[2] last result

Figure 98: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled

Figure 99: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 356 provides an example of results placement in Data RAM, with an odd RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled. The last 32-bit word is populated only with one 16-bit result.

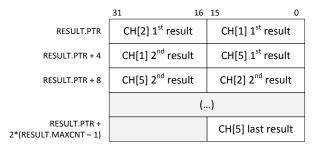


Figure 99: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled

37.6 EasyDMA

After configuring RESULT.PTR and RESULT.MAXCNT, the ADC resources are started by triggering the START task. The ADC is using EasyDMA to store results in a Result buffer in RAM.

The Result buffer is located at the address specified in the RESULT.PTR register. The RESULT.PTR register is double-buffered and it can be updated and prepared for the next START task immediately after the STARTED event is generated. The size of the Result buffer is specified in the RESULT.MAXCNT register and the ADC will generate an END event when it has filled up the Result buffer, see *Figure 100: ADC* on page 357. Results are stored in little-endian byte order in Data RAM. Every sample will be sign extended to 16 bit before stored in the Result buffer.

The ADC is stopped by triggering the STOP task. The STOP task will terminate an ongoing sampling. The ADC will generate a STOPPED event when it has stopped. If the ADC is already stopped when the STOP task is triggered, the STOPPED event will still be generated.



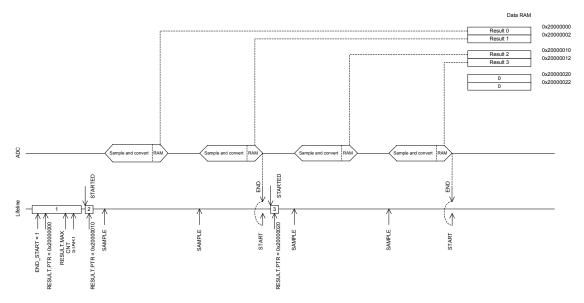


Figure 100: ADC

If the RESULT.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

The EasyDMA will have finished accessing the RAM when the END or STOPPED event has been generated.

The RESULT.AMOUNT register can be read following an END event or a STOPPED event to see how many results have been transferred to the Result buffer in RAM since the START task was triggered.

In Scan mode, the size of the Result buffer must be large enough to have room for a minimum one result from each of the enabled channels. To secure this, RESULT.MAXCNT must be specified to RESULT.MAXCNT >= "number of channels enabled". See *Scan mode* on page 355 for more information about Scan mode.

37.7 Resistor ladder

The ADC has an internal resistor string for positive and negative input.

See Figure 101: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP) on page 358. The resistors are controlled in the CH[n].CONFIG.RESP and CH[n].CONFIG.RESN registers.



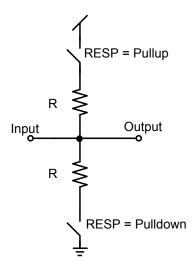


Figure 101: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)

37.8 Reference

The ADC can use two different references, controlled in the REFSEL field of the CH[n].CONFIG register.

These are:

- · Internal reference
- · VDD as reference

The internal reference results in an input range of ± 0.6 V on the ADC core. VDD as reference results in an input range of $\pm VDD/4$ on the ADC core. The gain block can be used to change the effective input range of the ADC.

```
Input range = (+- 0.6 \text{ V or } +-\text{VDD}/4)/\text{Gain}
```

For example, choosing VDD as reference, single ended input (grounded negative input), and a gain of 1/4 the input range will be:

```
Input range = (VDD/4)/(1/4) = VDD
```

With internal reference, single ended input (grounded negative input), and a gain of 1/6 the input range will be:

```
Input range = (0.6 \text{ V})/(1/6) = 3.6 \text{ V}
```

The AIN0-AIN7 inputs cannot exceed VDD, or be lower than VSS.

37.9 Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see *Figure 102: Simplified ADC sample network* on page 359. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source (R_{source}) resistance. For high source resistance the acquisition time should be increased, see *Table 84: Acquisition time* on page 359.



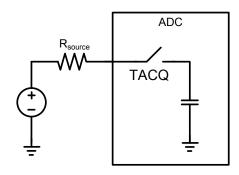


Figure 102: Simplified ADC sample network

Table 84: Acquisition time

TACQ [µs]	Maximum source resistance [kOhm]
3	10
5	40
10	100
15	200
20	400
40	800

37.10 Limits event monitoring

A channel can be event monitored by configuring limit register CH[n].LIMIT.

If the conversion result is higher than the defined high limit, or lower than the defined low limit, the appropriate event will get fired.

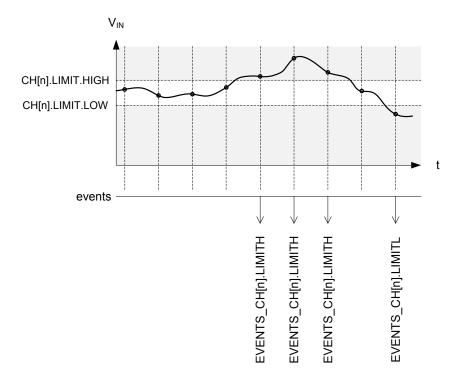


Figure 103: Example of limits monitoring on channel 'n'

Note that when setting the limits, CH[n].LIMIT.HIGH shall always be higher than or equal to CH[n].LIMIT.LOW. In other words, an event can be fired only when the input signal has been sampled



outside of the defined limits. It is not possible to fire an event when the input signal is inside a defined range by swapping high and low limits.

The comparison to limits always takes place, there is no need to enable it. If comparison is not required on a channel, the software shall simply ignore the related events. In that situation, the value of the limits registers is irrelevant, so it does not matter if CH[n].LIMIT.LOW is lower than CH[n].LIMIT.HIGH or not.

37.11 Registers

Table 85: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40007000	SAADC	SAADC	Analog to digital converter		

Table 86: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the ADC and prepare the result buffer in RAM
TASKS_SAMPLE	0x004	Take one ADC sample, if scan is enabled all channels are sampled
TASKS_STOP	0x008	Stop the ADC and terminate any on-going conversion
TASKS_CALIBRATEOFFSE	0x00C	Starts offset auto-calibration
EVENTS_STARTED	0x100	The ADC has started
EVENTS_END	0x104	The ADC has filled up the Result buffer
EVENTS_DONE	0x108	A conversion task has been completed. Depending on the mode, multiple conversions might be
		needed for a result to be transferred to RAM.
EVENTS_RESULTDONE	0x10C	A result is ready to get transferred to RAM.
EVENTS_CALIBRATEDON	0x110	Calibration is complete
EVENTS_STOPPED	0x114	The ADC has stopped
EVENTS_CH[0].LIMITH	0x118	Last results is equal or above CH[0].LIMIT.HIGH
EVENTS_CH[0].LIMITL	0x11C	Last results is equal or below CH[0].LIMIT.LOW
EVENTS_CH[1].LIMITH	0x120	Last results is equal or above CH[1].LIMIT.HIGH
EVENTS_CH[1].LIMITL	0x124	Last results is equal or below CH[1].LIMIT.LOW
EVENTS_CH[2].LIMITH	0x128	Last results is equal or above CH[2].LIMIT.HIGH
EVENTS_CH[2].LIMITL	0x12C	Last results is equal or below CH[2].LIMIT.LOW
EVENTS_CH[3].LIMITH	0x130	Last results is equal or above CH[3].LIMIT.HIGH
EVENTS_CH[3].LIMITL	0x134	Last results is equal or below CH[3].LIMIT.LOW
EVENTS_CH[4].LIMITH	0x138	Last results is equal or above CH[4].LIMIT.HIGH
EVENTS_CH[4].LIMITL	0x13C	Last results is equal or below CH[4].LIMIT.LOW
EVENTS_CH[5].LIMITH	0x140	Last results is equal or above CH[5].LIMIT.HIGH
EVENTS_CH[5].LIMITL	0x144	Last results is equal or below CH[5].LIMIT.LOW
EVENTS_CH[6].LIMITH	0x148	Last results is equal or above CH[6].LIMIT.HIGH
EVENTS_CH[6].LIMITL	0x14C	Last results is equal or below CH[6].LIMIT.LOW
EVENTS_CH[7].LIMITH	0x150	Last results is equal or above CH[7].LIMIT.HIGH
EVENTS_CH[7].LIMITL	0x154	Last results is equal or below CH[7].LIMIT.LOW
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Status
ENABLE	0x500	Enable or disable ADC
CH[0].PSELP	0x510	Input positive pin selection for CH[0]
CH[0].PSELN	0x514	Input negative pin selection for CH[0]
CH[0].CONFIG	0x518	Input configuration for CH[0]
CH[0].LIMIT	0x51C	High/low limits for event monitoring a channel
CH[1].PSELP	0x520	Input positive pin selection for CH[1]
CH[1].PSELN	0x524	Input negative pin selection for CH[1]
CH[1].CONFIG	0x528	Input configuration for CH[1]
CH[1].LIMIT	0x52C	High/low limits for event monitoring a channel
CH[2].PSELP	0x530	Input positive pin selection for CH[2]



Register	Offset	Description
CH[2].PSELN	0x534	Input negative pin selection for CH[2]
CH[2].CONFIG	0x538	Input configuration for CH[2]
CH[2].LIMIT	0x53C	High/low limits for event monitoring a channel
CH[3].PSELP	0x540	Input positive pin selection for CH[3]
CH[3].PSELN	0x544	Input negative pin selection for CH[3]
CH[3].CONFIG	0x548	Input configuration for CH[3]
CH[3].LIMIT	0x54C	High/low limits for event monitoring a channel
CH[4].PSELP	0x550	Input positive pin selection for CH[4]
CH[4].PSELN	0x554	Input negative pin selection for CH[4]
CH[4].CONFIG	0x558	Input configuration for CH[4]
CH[4].LIMIT	0x55C	High/low limits for event monitoring a channel
CH[5].PSELP	0x560	Input positive pin selection for CH[5]
CH[5].PSELN	0x564	Input negative pin selection for CH[5]
CH[5].CONFIG	0x568	Input configuration for CH[5]
CH[5].LIMIT	0x56C	High/low limits for event monitoring a channel
CH[6].PSELP	0x570	Input positive pin selection for CH[6]
CH[6].PSELN	0x574	Input negative pin selection for CH[6]
CH[6].CONFIG	0x578	Input configuration for CH[6]
CH[6].LIMIT	0x57C	High/low limits for event monitoring a channel
CH[7].PSELP	0x580	Input positive pin selection for CH[7]
CH[7].PSELN	0x584	Input negative pin selection for CH[7]
CH[7].CONFIG	0x588	Input configuration for CH[7]
CH[7].LIMIT	0x58C	High/low limits for event monitoring a channel
RESOLUTION	0x5F0	Resolution configuration
OVERSAMPLE	0x5F4	Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is
		applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.
SAMPLERATE	0x5F8	Controls normal or continuous sample rate
RESULT.PTR	0x62C	Data pointer
RESULT.MAXCNT	0x630	Maximum number of buffer words to transfer
RESULT.AMOUNT	0x634	Number of buffer words transferred since last START

37.11.1 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit r	numb	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	STARTED			Enable or disable interrupt for STARTED event
					See EVENTS_STARTED
			Disabled	0	Disable
			Disabled	0	
			Enabled	1	Enable
В	RW	END			Enable or disable interrupt for END event
					See EVENTS_END
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	DONE			Enable or disable interrupt for DONE event
					See EVENTS_DONE
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	RESULTDONE			Enable or disable interrupt for RESULTDONE event
					See EVENTS_RESULTDONE
			Disabled	0	Disable
			Enabled	1	Enable



	numbe	er		31 30	0 29	9 28	27	26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld Bos	s+ 0v0	000000		0 0					0 0	V U T S R Q P O N M L K J I H G F E D C B A 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Valu		U	U	U	0 0	Description
E		CALIBRATEDONE	value la	valu						Enable or disable interrupt for CALIBRATEDONE event
										See EVENTS_CALIBRATEDONE
			Disabled	0						Disable
			Enabled	1						Enable
F	RW	STOPPED								Enable or disable interrupt for STOPPED event
										See EVENTS_STOPPED
			Disabled	0						Disable
G	D\A/	CHOLIMITH	Enabled	1						Enable Enable or disable interrupt for CHIOLLIMITH event
G	KVV	CHOLIMITH								Enable or disable interrupt for CH[0].LIMITH event
			Disabled	0						See EVENTS_CH[0].LIMITH
			Disabled Enabled	0						Disable Enable
Н	RW	CHOLIMITL	Endoica	•						Enable or disable interrupt for CH[0].LIMITL event
										See EVENTS_CH[0].LIMITL
			Disabled	0						Disable
			Enabled	1						Enable
I	RW	CH1LIMITH								Enable or disable interrupt for CH[1].LIMITH event
										See EVENTS_CH[1].LIMITH
			Disabled	0						Disable
			Enabled	1						Enable
J	RW	CH1LIMITL								Enable or disable interrupt for CH[1].LIMITL event
										See EVENTS_CH[1].LIMITL
			Disabled	0						Disable
	DVA	CHALIMITH	Enabled	1						Enable Finable and disable interpret for CU(2) LIMITH accord
K	KVV	CH2LIMITH								Enable or disable interrupt for CH[2].LIMITH event
			6: 11 1	•						See EVENTS_CH[2].LIMITH
			Disabled Enabled	0						Disable Enable
L	RW	CH2LIMITL	Endoica	•						Enable or disable interrupt for CH[2].LIMITL event
										See EVENTS_CH[2].LIMITL
			Disabled	0						Disable
			Enabled	1						Enable
М	RW	CH3LIMITH								Enable or disable interrupt for CH[3].LIMITH event
										See EVENTS_CH[3].LIMITH
			Disabled	0						Disable
			Enabled	1						Enable
N	RW	CH3LIMITL								Enable or disable interrupt for CH[3].LIMITL event
										See EVENTS_CH[3].LIMITL
			Disabled	0						Disable
_	D\A/	CHALIMITH	Enabled	1						Enable Chable or disable interrupt for CUEAL IMITH quant
0	ΚVV	CH4LIMITH								Enable or disable interrupt for CH[4].LIMITH event
			Disabled	0						See EVENTS_CH[4].LIMITH
			Disabled Enabled	0						Disable Enable
Р	RW	CH4LIMITL		_						Enable or disable interrupt for CH[4].LIMITL event
										See EVENTS_CH[4].LIMITL
			Disabled	0						Disable
			Enabled	1						Enable
Q	RW	CH5LIMITH								Enable or disable interrupt for CH[5].LIMITH event
										See EVENTS_CH[5].LIMITH



Bitı	numbe	er		31	30 29	9 28	27	26 2	5 2	24 2	3 2	22 2:	1 20	19	18	17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id												٧	′ U	Т	S	R	Q	Р	0	Ν	М	L K	J	-1	Н	G	F	Е	D (В	Α
Res	et 0x0	0000000		0	0 0	0 (0	0 (0 (0 0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Val	ıe					D)es	cript	ion																		
			Disabled	0						D	isa	able																			
			Enabled	1						Е	nal	ble																			
R	RW	CH5LIMITL								Е	nal	ble c	r d	isab	le i	ntei	rup	t fo	or C	H[5].LIN	IITL	eve	nt							
										S	ee	EVE	NTS	C H	1[5]	.LIN	ΛΙΤΙ														
			Disabled	0						D	isa	able		_																	
			Enabled	1						Е	nal	ble																			
S	RW	CH6LIMITH								Е	nal	ble c	r d	isab	le i	ntei	rrup	t fo	or C	H[6].LIN	IITH	eve	ent							
										Ç.	00	EVE	NITS	CL	J[6]		літі	_													
			Disabled	0								able	1113		ı[U]	·LIII															
			Enabled	1								ble																			
Т	RW	CH6LIMITL	Z. I. G. Z.									ble c	or di	isab	le i	ntei	rur	t fo	or C	H[6	1.LIN	1ITL	eve	nt							
																	·				,										
												EVE	NTS	_CF	1[6]	.LIN	ΛΙΤΙ														
			Disabled	0								able																			
			Enabled	1								ble																			
U	RW	CH7LIMITH								E	nal	ble c	or di	isab	le ii	ntei	rrup	t to	or C	H[7	J.LIN	IITH	eve	ent							
										S	ee	EVE	NTS	_CF	1[7]	.LIN	ЛΙΤΙ	1													
			Disabled	0						D	isa	able																			
			Enabled	1						Е	nal	ble																			
٧	RW	CH7LIMITL								E	nal	ble c	r d	isab	le i	ntei	rup	t fo	or C	H[7].LIN	IITL	eve	nt							
										S	ee	EVE	NTS	_CF	1[7]	.LIN	ИΙΤΙ														
			Disabled	0								able																			
			Enabled	1						Е	nal	ble																			

37.11.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31	30	29	28 2	7 2	6 25	5 24	4 23	3 22	21	20	19	18	17	' 16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3 2	1	0
Id													٧	U	Т	S	R	Q	Р	О	N	M	L F	(J	-1	Н	G	F	ЕΙ) C	В	Α
Res	et 0x0	0000000		0	0	0	0 0) (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																		
Α	RW	STARTED									W	/rite	'1'	to E	na	ble	int	errı	upt	for	STA	RTE	D ev	ent								
											Se	ee <i>E</i> '	VΕN	ITS_	ST	ART	ΓED)														
			Set	1							Er	nabl	e																			
			Disabled	0							Re	ead:	Dis	abl	ed																	
			Enabled	1							Re	ead:	Ena	able	ed																	
В	RW	END									W	/rite	'1'	to E	na	ble	int	errı	upt	for	END	ev	ent									
											Se	ee <i>E</i>	VΕN	ITS_	ΕN	ID																
			Set	1							Er	nabl	e																			
			Disabled	0							Re	ead:	Dis	abl	ed																	
			Enabled	1							Re	ead:	Ena	able	ed																	
С	RW	DONE									W	/rite	'1'	to E	na	ble	int	errı	upt	for	100	NE e	ven	t								
											Se	ee <i>E</i> '	VΕN	ITS_	DC	ONE																
			Set	1							Er	nabl	e																			
			Disabled	0							Re	ead:	Dis	abl	ed																	
			Enabled	1							Re	ead:	Ena	able	ed																	
D	RW	RESULTDONE									W	/rite	'1'	to E	na	ble	int	errı	upt	for	RES	ULT	DON	IE e	vent	:						
											Se	ee <i>E</i> '	VEN	ITS_	RE	SUL	LTD	ON	Ε													
			Set	1							Er	nabl	e																			
			Disabled	0							Re	ead:	Dis	abl	ed																	
			Enabled	1							Re	ead:	Ena	able	ed																	



Bit n	umbe	r		3	1 30	29	28	27	26	25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id											V U T S R Q P O N M L K J I H G F E D C B A
		0000000					0	0	0	0 (
Id		Field	Value Id	V	alue						Description Write 11 to Enable interrupt for CALIDRATE DONE overt
E	KVV	CALIBRATEDONE									Write '1' to Enable interrupt for CALIBRATEDONE event
											See EVENTS_CALIBRATEDONE
			Set	1							Enable
			Disabled	0							Read: Disabled
_	D14/	CTORRER	Enabled	1							Read: Enabled
F	RW	STOPPED									Write '1' to Enable interrupt for STOPPED event
											See EVENTS_STOPPED
			Set	1							Enable
			Disabled	0							Read: Disabled
_	D) A /	CHOUNAUTH	Enabled	1							Read: Enabled
G	RW	CHOLIMITH									Write '1' to Enable interrupt for CH[0].LIMITH event
											See EVENTS_CH[0].LIMITH
			Set	1							Enable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
Н	RW	CHOLIMITL									Write '1' to Enable interrupt for CH[0].LIMITL event
											See EVENTS_CH[0].LIMITL
			Set	1							Enable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
I	RW	CH1LIMITH									Write '1' to Enable interrupt for CH[1].LIMITH event
											See EVENTS_CH[1].LIMITH
			Set	1							Enable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
J	RW	CH1LIMITL									Write '1' to Enable interrupt for CH[1].LIMITL event
											See EVENTS_CH[1].LIMITL
			Set	1							Enable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
K	RW	CH2LIMITH									Write '1' to Enable interrupt for CH[2].LIMITH event
											See EVENTS_CH[2].LIMITH
			Set	1							Enable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
L	RW	CH2LIMITL									Write '1' to Enable interrupt for CH[2].LIMITL event
											See EVENTS_CH[2].LIMITL
			Set	1							Enable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
М	RW	CH3LIMITH									Write '1' to Enable interrupt for CH[3].LIMITH event
											See EVENTS_CH[3].LIMITH
			Set	1							Enable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
N	RW	CH3LIMITL									Write '1' to Enable interrupt for CH[3].LIMITL event
											See EVENTS_CH[3].LIMITL
			Set	1							Enable
			Disabled	0							Read: Disabled
			Enabled	1							Read: Enabled
0	D\A/	CH4LIMITH									Write '1' to Enable interrupt for CH[4].LIMITH event



Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				V U T S R Q P O N M L K J I H G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_CH[4].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Р	RW CH4LIMITL			Write '1' to Enable interrupt for CH[4].LIMITL event
				See EVENTS_CH[4].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Q	RW CH5LIMITH			Write '1' to Enable interrupt for CH[5].LIMITH event
				See EVENTS_CH[5].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
R	RW CH5LIMITL			Write '1' to Enable interrupt for CH[5].LIMITL event
				See EVENTS_CH[5].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
S	RW CH6LIMITH			Write '1' to Enable interrupt for CH[6].LIMITH event
				See EVENTS_CH[6].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Т	RW CH6LIMITL			Write '1' to Enable interrupt for CH[6].LIMITL event
				See EVENTS_CH[6].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
U	RW CH7LIMITH			Write '1' to Enable interrupt for CH[7].LIMITH event
				See EVENTS_CH[7].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
٧	RW CH7LIMITL			Write '1' to Enable interrupt for CH[7].LIMITL event
		Sot	1	See EVENTS_CH[7].LIMITL
		Set	1	Enable Road: Disabled
		Disabled Enabled	0	Read: Disabled Read: Enabled
		Elidbieu	1	neau. Eliabieu

37.11.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit r	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id														٧	U	Т	S	R	Q	Р	О	Ν	М	L	K	J	1	Н	G	F	Ε	D	С	ВА	١.
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							Des	scri	otic	n																				
Α	RW	STARTED										Wr	ite '	1' t	o D	isal	ble	int	err	upt	for	ST	٩RT	ED	eve	nt									
													e EV		TS_	STA	\RT	ED																	
			Clear	1								Dis	able	5																					



Bitı	numb	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x(0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	END			Write '1' to Disable interrupt for END event
					See EVENTS_END
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	DONE			Write '1' to Disable interrupt for DONE event
					See EVENTS_DONE
			Clear	1	Disable
			Disabled	0	Read: Disabled
	5111	250111 = 2415	Enabled	1	Read: Enabled
D	RW	RESULTDONE			Write '1' to Disable interrupt for RESULTDONE event
					See EVENTS_RESULTDONE
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Е	RW	CALIBRATEDONE			Write '1' to Disable interrupt for CALIBRATEDONE event
					See EVENTS_CALIBRATEDONE
			Clear	1	Disable
			Disabled	0	Read: Disabled
F	D\A/	CTORRED	Enabled	1	Read: Enabled
г	KVV	STOPPED			Write '1' to Disable interrupt for STOPPED event
					See EVENTS_STOPPED
			Clear	1	Disable
			Disabled Enabled	0	Read: Disabled Read: Enabled
G	RW	CHOLIMITH	Eliabled	1	Write '1' to Disable interrupt for CH[0].LIMITH event
Ü		CHOLINITH			
					See EVENTS_CH[0].LIMITH
			Clear	1	Disable Read Disabled
			Disabled Enabled	1	Read: Disabled Read: Enabled
Н	RW	CHOLIMITL	Enabled	-	Write '1' to Disable interrupt for CH[0].LIMITL event
			Clear	1	See EVENTS_CH[0].LIMITL Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
ı	RW	CH1LIMITH			Write '1' to Disable interrupt for CH[1].LIMITH event
					See EVENTS_CH[1].LIMITH
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
J	RW	CH1LIMITL			Write '1' to Disable interrupt for CH[1].LIMITL event
					See EVENTS_CH[1].LIMITL
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	CH2LIMITH			Write '1' to Disable interrupt for CH[2].LIMITH event
					See EVENTS_CH[2].LIMITH
			Clear	1	Disable
			Disabled	0	Read: Disabled



Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Enabled	1	Read: Enabled
L	RW	CH2LIMITL			Write '1' to Disable interrupt for CH[2].LIMITL event
					See EVENTS_CH[2].LIMITL
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
М	RW	CH3LIMITH			Write '1' to Disable interrupt for CH[3].LIMITH event
					See EVENTS_CH[3].LIMITH
			Clear	1	Disable
			Disabled	0	Read: Disabled
N.	DVA	CURLINATE	Enabled	1	Read: Enabled
N	KW	CH3LIMITL			Write '1' to Disable interrupt for CH[3].LIMITL event
					See EVENTS_CH[3].LIMITL
			Clear	1	Disable
			Disabled	0	Read: Disabled
0	D\A/	CH4LIMITH	Enabled	1	Read: Enabled Write '1' to Disable interrupt for CH[4].LIMITH event
U	NVV	CH4LIIVII I H			
					See EVENTS_CH[4].LIMITH
			Clear	1	Disable
			Disabled Enabled	0	Read: Disabled Read: Enabled
Р	RW	CH4LIMITL	Lilabled	1	Write '1' to Disable interrupt for CH[4].LIMITL event
·		0.1.122			
			Clear	1	See EVENTS_CH[4].LIMITL Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Q	RW	CH5LIMITH			Write '1' to Disable interrupt for CH[5].LIMITH event
					See EVENTS_CH[5].LIMITH
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
R	RW	CH5LIMITL			Write '1' to Disable interrupt for CH[5].LIMITL event
					See EVENTS_CH[5].LIMITL
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
S	RW	CH6LIMITH			Write '1' to Disable interrupt for CH[6].LIMITH event
					See EVENTS_CH[6].LIMITH
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Т	RW	CH6LIMITL			Write '1' to Disable interrupt for CH[6].LIMITL event
					See EVENTS_CH[6].LIMITL
			Clear	1	Disable
			Disabled	0	Read: Disabled
11	D\A/	CH7IIMITU	Enabled	1	Read: Enabled Write '1' to Disable interrupt for CH[7] LIMITH event
U	κW	CH7LIMITH			Write '1' to Disable interrupt for CH[7].LIMITH event
					See EVENTS_CH[7].LIMITH
			Clear	1	Disable Read: Disabled
			Disabled Enabled	0	Read: Disabled Read: Enabled
			Litabica	±	nead. Enabled



Bit r	iumbe	er		31	1 30	29	2	8 2	7	26	25	24	23	2	2 21	1 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id															V	' U	Т	S	R	Q	Р	0	Ν	М	L	K	J	1	Н	G	F	Ε	D	С	В	Α
Res	et 0x0	0000000		0	0	0	(0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•							De	esc	ript	ion																				
٧	RW	CH7LIMITL											W	rite	· '1'	to	Dis	able	in	terr	upt	fo	r CH	[7]	.LIN	1ITL	eve	ent								
													Se	e E	VEI	NTS	_CF	1[7]	.LII	ИІТ	L															
			Clear	1									Di	sak	le																					
			Disabled	0									Re	ad	: Di	sab	led																			
			Enabled	1									Re	ad	: En	nabl	ed																			

37.11.4 STATUS

Address offset: 0x400

Status

Bit	numbe	er		3:	1 30	29	9 2	8 2	7 2	6 2	5 2	4 2	3 2	2 2:	1 20	19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0) (0 (0 0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	V	alu	е						D	esc	ript	ion																			
Α	R	STATUS										S	tatı	ıs																				
			Ready	0								Α	DC	is re	ead	y. N	lo o	n-g	oin	g co	nve	ersio	on.											
			Busy	1								Α	DC	is b	usy	. Co	nve	ersio	on i	n pı	ogı	ess												

37.11.5 ENABLE

Address offset: 0x500 Enable or disable ADC

Bit	numbe	er		31 30	29	28 2	7 26	5 25	24	23	22	21	20	19	18	17	16	15 1	L4 1	3 1	2 1:	10	9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value						Des	scri	pti	on																		
Α	RW	ENABLE								Ena	ble	e or	dis	able	e A[ЭC															
			Disabled	0						Disa	able	e A	DC																		
			Enabled	1						Ena	ble	e AE	DC																		
										Wh	en	ena	able	ed, t	he.	AD	C w	ill a	cqui	re a	cce	ss to	th	e an	alo	g in	ıpu	t			
										pin	s sp	oeci	ifie	d in	the	CH	[n].	PSE	LP a	and	CH[n].F	SEL	N re	gis	ters	š.				

37.11.6 CH[0].PSELP

Address offset: 0x510

Input positive pin selection for CH[0]

Bit nu	umbe	r		31	30 29	28	3 27	26 2	25 2	24 2	23 22	21	20 :	19 1	18 1	.7 1	6 1	L5 1	4 1	3 12	11	10	9	8	7 (5 5	4	3	2	1 0
Id																											Α	Α	Α ,	А А
Rese	t 0x0(0000000		0	0 0	0	0	0	0	0	0 0	0	0	0	0	0 ()	0 (0	0	0	0	0	0 () (0	0	0	0 (0 0
Id	RW	Field	Value Id	Val	ue						Descr	iptic	n																	
Α	RW	PSELP								A	Analo	g po	sitiv	ve ir	npu	t ch	anı	nel												
			NC	0						1	Not c	onne	cte	d																
			AnalogInput0	1						A	ONIA																			
			AnalogInput1	2						A	AIN1																			
			AnalogInput2	3						A	AIN2																			
			AnalogInput3	4						A	SNIA																			
			AnalogInput4	5						A	AIN4																			
			AnalogInput5	6						A	AIN5																			
			AnalogInput6	7						A	AIN6																			
			AnalogInput7	8						A	AIN7																			
			VDD	9						١	/DD																			



37.11.7 CH[0].PSELN

Address offset: 0x514

Input negative pin selection for CH[0]

Bit r	numbe	r		31	30 2	9 2	8 27	7 26	25	24 :	23 22	21 2	20	19 1	8 1	17 1	.6	15 1	.4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																												A	A А	Α	Α
Rese	et 0x0	0000000		0	0 () (0 0	0	0	0	0 0	0	0	0 ()	0	0	0	0 () (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue					ı	Descr	iptio	n																		
Α	RW	PSELN								,	Analo	g ne	gat	ive iı	npı	ut, e	ena	ble	s dif	fer	enti	al cl	nanı	nel							
			NC	0						ı	Not c	onne	cte	d																	
			AnalogInput0	1						,	AIN0																				
			AnalogInput1	2						,	AIN1																				
			AnalogInput2	3						,	AIN2																				
			AnalogInput3	4						,	AIN3																				
			AnalogInput4	5						,	AIN4																				
			AnalogInput5	6						,	AIN5																				
			AnalogInput6	7						,	AIN6																				
			AnalogInput7	8						,	AIN7																				
			VDD	9						١	/DD																				

37.11.8 CH[0].CONFIG

Address offset: 0x518

Input configuration for CH[0]

Bit	numbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	23	3 22 2	1 20	19	18	17	16	15	14	13	L2 1	.1 1) 9	8	7	6	5	4	3 2	1	0
Id										G			F		Е	Ε	Ε				D	C	. c	С			В	В		Α	Α
Res	et 0x0	00020000		0	0	0	0 0) (0	0	0	0 0	0	0	0	1	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0
ld	RW	Field	Value Id	Va	lue						De	escrip	tion																		
Α	RW	RESP									Pc	ositive	cha	nne	l res	sisto	or c	ont	rol												
			Bypass	0							Ву	/pass i	esis	tor	ado	ler															
			Pulldown	1							Ρu	ıll-dov	vn to	o GN	ID																
			Pullup	2							Ρu	ıll-up 1	to V	DD																	
			VDD1_2	3							Se	et inpu	t at	VDE)/2																
В	RW	RESN									Ne	egativ	e ch	ann	el re	esis	tor	cor	itro												
			Bypass	0							Ву	pass ı	esis	tor	ado	ler															
			Pulldown	1							Pu	ıll-dov	vn to	o GN	ID																
			Pullup	2							Pu	ıll-up 1	to V	DD																	
			VDD1_2	3							Se	et inpu	t at	VDE)/2																
С	RW	GAIN									Ga	ain coi	ntro	l																	
			Gain1_6	0							1/	6																			
			Gain1_5	1							1/	' 5																			
			Gain1_4	2							1/	4																			
			Gain1_3	3							1/	' 3																			
			Gain1_2	4							1/	′2																			
			Gain1	5							1																				
			Gain2	6							2																				
			Gain4	7							4																				
D	RW	REFSEL									Re	eferen	ce c	ontr	ol																
			Internal	0							In	ternal	refe	eren	ce (0.6	V)														
			VDD1_4	1							VE	DD/4 a	is re	fere	nce																
Ε	RW	TACQ									Ac	cquisit	ion	time	, th	e ti	me	the	A C	C u	ses	to s	amp	ole t	he i	npu	t				
											vo	oltage																			
			3us	0							3 (us																			
			5us	1							5 (us																			
			10us	2							10) us																			
			15us	3							15	5 us																			
			20us	4							20) us																			



Bit	numbe	er		31 30	29	28	27	26	25	24	23 2	22 2	1 20	19	18	17	16	15	14 1	13 1	L2 1	1 1	9	8	7	6	5	4	3 2	1	. 0
Id										G			F		Ε	Ε	Ε				D	C	. C	С			В	В		Α	A
Res	et 0x0	00020000		0 0	0	0	0	0	0	0	0	0 (0	0	0	1	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value	•						Des	crip	tion																		
			40us	5							40 u	IS																			
F	RW	MODE									Enal	ble o	diffe	rent	tial	mo	de														
			SE	0							Sing	le e	nde	d, P	SELI	٧w	ill b	e ig	nor	ed,	neg	ativ	e in	put	to A	ADC					
											shor	rted	to G	SND																	
			Diff	1							Diffe	eren	tial																		
G	RW	BURST									Enal	ble b	ours	t mo	ode																
			Disabled	0							Burs	st m	ode	is d	isab	led	(no	rm	al o	per	atio	n)									
			Enabled	1							Burs	st m	ode	is e	nab	led.	SA	AD	C tal	kes	2^0	OVE	RSAI	MPL	E n	umb	er	of			
											sam	ples	as f	ast	as i	t ca	n. a	nd	sen	ds t	he a	ver	age	to [ata	RA	М.				

37.11.9 CH[0].LIMIT

Address offset: 0x51C

High/low limits for event monitoring a channel

Bit	nun	nbe	r		31	. 30	29	28	27	7 26	6 2	5 2	4 2	3 2	2 2	1 2	0 1	9 1	8 1	.7 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	! :	1 0
Id					В	В	В	В	В	В	В	S E	ВЕ	3 E	3 E	3 E	3 E	3	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		А А
Res	et (0x7	FF8000		0	1	1	1	1	1	. 1	. 1	1 :	L 1	L 1	L 1	1 :	1	1 :	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	R	w	Field	Value Id	Va	lue							D	esc	rip	tior	1																			
Α	R	W	LOW		[-3	3276	58 t	0 +	32	767	7]		L	ow	lev	el li	mit																			
В	R'	w	HIGH		[-3	3276	58 t	0 +	32	767	7]		Н	ligh	lev	el l	imi	t																		

37.11.10 CH[1].PSELP

Address offset: 0x520

Input positive pin selection for CH[1]

Bit r	iumbe	r		31	30	29	28 2	27 2	26 2	5 24	1 23	22 :	21 20) 19	9 18	3 17	16	15	14	13 1	.2 11	. 10	9	8	7	6	5 4 Δ	,	2 A	1 A	_
	et 0x0	0000000		0	0	0	0 (0	0 (0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0			0	
Id	RW	Field	Value Id	Va	lue						De	escrip	ption																		
Α	RW	PSELP									An	nalog	g posi	tive	e inp	out	chai	nne	I												
			NC	0							No	ot co	nnect	ted																	
			AnalogInput0	1							ΑI	N0																			
			AnalogInput1	2							ΑI	N1																			
			AnalogInput2	3							ΑI	N2																			
			AnalogInput3	4							ΑI	N3																			
			AnalogInput4	5							ΑI	N4																			
			AnalogInput5	6							ΑI	N5																			
			AnalogInput6	7							ΑI	N6																			
			AnalogInput7	8							ΑI	N7																			
			VDD	9							VD	DD																			

37.11.11 CH[1].PSELN

Address offset: 0x524

Input negative pin selection for CH[1]

Bit	numbe	er		31 30	29	28	27 2	6 2	5 24	1 23	22	21	20	19	18	17	16	15	14 1	L3 1	.2 1	1 10	9	8	7	6	5	4	3	2 1	0
Id																												Α	A A	A A	Α
Res	et 0x0	0000000		0 0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value	•					De	escri	iptio	on																		
Α	RW	PSELN								Ar	nalo	g ne	egat	ive	inp	ut,	ena	ble	s di	ffer	enti	al ch	anr	nel							
			NC	0						No	ot co	onn	ecte	ed																	
			AnalogInput0	1						ΑI	N0																				



Bit number		31	. 30	29	28	27	26	25 2	24 2	3 2	2 21	20	19	18	17	16	15 :	14 1	.3 1	2 1	l 10	9	8	7	6	5 4	1 3	2	1	0
Id																										A	Α Α	A	Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0
Id RW Field	Value Id	Va	alue							esc	ripti	on																		
	AnalogInput1	2							A	IN1																				
	AnalogInput2	3							A	IN2																				
	AnalogInput3	4							A	NIN3																				
	AnalogInput4	5							A	IN4																				
	AnalogInput5	6							A	AIN5																				
	AnalogInput6	7							A	NIN6																				
	AnalogInput7	8							A	IN7																				
	VDD	9							١	/DD																				

37.11.12 CH[1].CONFIG

Address offset: 0x528

Input configuration for CH[1]

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d			G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0	0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0
d RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
O RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential
G RW BURST			Enable burst mode
	Disabled	0	Burst mode is disabled (normal operation)



Bit number		31 30 29 28 27 26	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Enabled	1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
			camples as fact as it can, and conds the average to Data PAM

37.11.13 CH[1].LIMIT

Address offset: 0x52C

High/low limits for event monitoring a channel

Bit r	numbe	r		31	1 30	29	28	27	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 :	10	9	8	7	6	5	4	3 2	1	1 0
Id				В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	А А	Δ	A A
Res	et 0x7	FFF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0 0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																			
Α	RW	LOW		Value [-32768 to +32767]								Lo	w le	vel	lim	it																		
В	RW	HIGH										His	gh le	evel	l lim	nit																		

37.11.14 CH[2].PSELP

Address offset: 0x530

Input positive pin selection for CH[2]

Bit r	numbe	er		31	30 2	29 2	28 27	7 26	5 25	24	23 2	2 21	20	19	18	17	16 :	15 :	14 1	.3 1	2 11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id																											,	Δ ,	A A	Α	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 (0	0	0
Id	RW	Field	Value Id	Va	lue						Des	cript	ion																		
Α	RW	PSELP									Ana	log p	osit	ive i	inpu	ut cl	han	nel													
			NC	0							Not	conr	nect	ed																	
			AnalogInput0	1							AIN)																			
			AnalogInput1	2							AIN	1																			
			AnalogInput2	3							AIN:	2																			
			AnalogInput3	4							AIN:	3																			
			AnalogInput4	5							AIN	4																			
			AnalogInput5	6							AIN:	5																			
			AnalogInput6	7							AIN	5																			
			AnalogInput7	8							AIN [°]	7																			
			VDD	9							VDD)																			

37.11.15 CH[2].PSELN

Address offset: 0x534

Input negative pin selection for CH[2]

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| | | AnalogInput0 | 1 | | | | | | | Α | IN0 | | |
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| | | AnalogInput1 | 2 | | | | | | | Α | IN1 | | |
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| | | AnalogInput2 | 3 | | | | | | | Α | IN2 | | |
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| | | AnalogInput3 | 4 | | | | | | | Α | IN3 | | |
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| | | AnalogInput4 | 5 | | | | | | | Α | IN4 | | |
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| | | AnalogInput5 | 6 | | | | | | | Α | IN5 | | |
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| | | AnalogInput6 | 7 | | | | | | | Α | IN6 | | |
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| | | AnalogInput7 | 8 | | | | | | | Α | IN7 | | |
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| | 0x0
RW | Ox0000000 RW Field RW PSELN | Ox0000000 RW Field Value Id RW PSELN NC AnalogInput0 AnalogInput1 AnalogInput2 AnalogInput3 AnalogInput4 AnalogInput5 AnalogInput6 | 0x00000000 0 RW Field Value Id Value Id RW PSELN NC 0 AnalogInput0 1 AnalogInput1 2 AnalogInput2 3 AnalogInput3 4 AnalogInput4 5 AnalogInput5 6 AnalogInput6 7 | Ox00000000 0 0 RW Field Value Id Value RW PSELN NC 0 AnalogInput0 1 4 AnalogInput1 2 2 AnalogInput2 3 3 AnalogInput3 4 4 AnalogInput4 5 5 AnalogInput5 6 6 AnalogInput6 7 7 | Ox00000000 0 0 0 0 0 0 RW Field Value Id Value Id | Ox00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | Ox00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 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O O O O O O O O O O O O O O O O <th< td=""><td>Ox00000000 O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O</td><td>Ox00000000 Value Id Value Description RW Field Value Id Analog negative input, enables NC 0 Not connected AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4 AnalogInput5 6 AIN5 AnalogInput6 7 AIN6</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables different inpu</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables different inpu</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential and provided in put, enables differen</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential changes and the connected and the connected and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, 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NC 0 Not connected Analog nput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4 AnalogInput5 6 AIN5 AnalogInput6 7 AIN6</td><td>Ox000000000 Value Id Value Id Description RW Field Value Id PSELN Analog negative input, enables differential channel NC 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td> NC</td><td> Note Note </td><td> NC</td></th<></td></th<></td></th<> | Ox000000000 O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O <th< td=""><td>Ox000000000 O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O <th< td=""><td>Ox00000000 O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O</td><td>Ox00000000 Value Id Value Description RW Field Value Id Analog negative input, enables NC 0 Not connected AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4 AnalogInput5 6 AIN5 AnalogInput6 7 AIN6</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables different inpu</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables different inpu</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential and provided in put, enables differen</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential changes and the connected and the connected and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential channels. NC 0 Not connected Analog nput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4 AnalogInput5 6 AIN5 AnalogInput6 7 AIN6</td><td>Ox000000000 Value Id Value Id Description RW Field Value Id PSELN Analog negative input, enables differential channel NC 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td> NC</td><td> Note Note </td><td> NC</td></th<></td></th<> | Ox000000000 O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O <th< td=""><td>Ox00000000 O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O</td><td>Ox00000000 Value Id Value Description RW Field Value Id Analog negative input, enables NC 0 Not connected AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4 AnalogInput5 6 AIN5 AnalogInput6 7 AIN6</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables different inpu</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables different inpu</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential and provided in put, enables differen</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential changes and the connected and the connected and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog</td><td>Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential channels. NC 0 Not connected Analog nput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4 AnalogInput5 6 AIN5 AnalogInput6 7 AIN6</td><td>Ox000000000 Value Id Value Id Description RW Field Value Id PSELN Analog negative input, enables differential channel NC 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td> NC</td><td> Note Note </td><td> NC</td></th<> | Ox00000000 O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O O | Ox00000000 Value Id Value Description RW Field Value Id Analog negative input, enables NC 0 Not connected AnalogInput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput2 3 AIN2 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4 AnalogInput5 6 AIN5 AnalogInput6 7 AIN6 | Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables different inpu | Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables different inpu | Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential and provided in put, enables differen | Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential changes and the connected and the connected and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog negative input, enables differential changes and the connected analog | Ox000000000 Value Id Value Description RW Field Value Id Analog negative input, enables differential channels. NC 0 Not connected Analog nput0 1 AIN0 AnalogInput1 2 AIN1 AnalogInput3 4 AIN3 AnalogInput4 5 AIN4 AnalogInput5 6 AIN5 AnalogInput6 7 AIN6 | Ox000000000 Value Id Value Id Description RW Field Value Id PSELN Analog negative input, enables differential channel NC 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | NC | Note Note | NC |



Bit number		31 30 29 28 27 26	$25\ 24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id			АААА
Reset 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
	VDD	9	VDD

37.11.16 CH[2].CONFIG

Address offset: 0x538

Input configuration for CH[2]

Bit	numbe	er		31 30	29	28 2	7 26	25 2	24	23 22 2	21 2	20 1	9 1	8 1	7 :	16	15	14	13	12	11	1 10	9	8	7	6	5	4	3	2	1 0
Id									G			F		E E						D				C				В			A A
	et 0x0	0020000		0 0	0	0 (0 0			0 0 0							0	0	0						0	0			0	0	
Id		Field	Value Id	Value						Descrip																					
Α	RW	RESP								Positive	e ch	ann	el ı	resis	sto	r c	ont	rol													
			Bypass	0						Bypass	res	istor	·la	dde	r																
			Pulldown	1						Pull-dov	wn	to G	NE)																	
			Pullup	2						Pull-up	to '	VDD																			
			VDD1_2	3						Set inpu	ut a	it VD	D/	2																	
В	RW	RESN								Negativ	e c	hanı	nel	res	ist	or	con	itro	ol												
			Bypass	0						Bypass	res	istor	·la	dde	r																
			Pulldown	1						Pull-dov	wn	to G	NE)																	
			Pullup	2						Pull-up	to '	VDD																			
			VDD1_2	3						Set inpu	ut a	t VD	D/	2																	
С	RW	GAIN								Gain co	ntr	ol																			
			Gain1_6	0						1/6																					
			Gain1_5	1						1/5																					
			Gain1_4	2						1/4																					
			Gain1_3	3						1/3																					
			Gain1_2	4						1/2																					
			Gain1	5						1																					
			Gain2	6						2																					
			Gain4	7						4																					
D	RW	REFSEL								Referer	nce	con	tro	I																	
			Internal	0						Interna	l re	fere	nce	e (0.	۱ 6.	V)															
			VDD1_4	1						VDD/4																					
Ε	RW	TACQ								Acquisi		n tim	ıe,	the	tir	ne	the	A	DC	use	es t	o sa	ımp	le t	he	inp	ut				
										voltage																					
			3us	0						3 us																					
			5us	1						5 us																					
			10us	2						10 us																					
			15us	3						15 us																					
			20us	4						20 us																					
_			40us	5						40 us	1																				
F	KW	MODE	C.F.	0						Enable													,			۸.	_				
			SE	0						Single e				LN	WII	II b	e ig	no	red	, n	ega	ative	e in	put	to	ΑD	C				
			D:(f							shorted			ر																		
_	DVA	DUDCT	Diff	1						Differer				l a																	
G	ĸW	BURST	Disabled	0						Enable					ام	1-		اہ		.		. \									
			Disabled	0						Burst m													C ^ '		_		.h -				
			Enabled	1						Burst m																					
										sample	s as	rasi	t as	S IT (ar	ı, a	nd	sei	ıas	tn	e a	vera	ige	ťO l	Jat	a K	AIVI.	•			

37.11.17 CH[2].LIMIT

Address offset: 0x53C

High/low limits for event monitoring a channel



Bitı	number		31	. 30	29	28	27	26	25	24	23 :	22 2	21 2	0 1	9 1	8 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id			В	В	В	В	В	В	В	В	В	В	В	ВЕ	3 E	3 B	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α Α	АА
Res	et 0x7FFF8000		0	1	1	1	1	1	1	1	1	1	1	1 1	. 1	l 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0
Id	RW Field	Value Id	Va	lue							Des	crip	tio	n																		
Id A	RW Field RW LOW	Value Id				0 +	327	'67]				crip / lev																				

37.11.18 CH[3].PSELP

Address offset: 0x540

Input positive pin selection for CH[3]

Bit r	numbe	er		31	30	29 2	28 21	7 20	6 25	24	23 2	2 21	20	19	18	17 :	16	15 :	14 1	l3 1	2 11	. 10	9	8	7	6	_		3 2 A A	_	0 A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Va	lue						Desc	ripti	on																		
Α	RW	PSELP									Anal	og po	siti	ve i	npı	ut ch	nan	nel													
			NC	0							Not o	conn	ecte	ed																	
			AnalogInput0	1							AIN0	1																			
			AnalogInput1	2							AIN1																				
			AnalogInput2	3							AIN2																				
			AnalogInput3	4							AIN3																				
			AnalogInput4	5							AIN4																				
			AnalogInput5	6							AIN5																				
			AnalogInput6	7							AIN6																				
			AnalogInput7	8							AIN7																				
			VDD	9							VDD																				

37.11.19 CH[3].PSELN

Address offset: 0x544

Input negative pin selection for CH[3]

Bit n	umbe	r		31	30	29 :	28 2	27 2	26 2	5 24	4 2	3 22	21	20	19 :	18 1	.7 1	6 1	5 1	4 1	3 12	2 11	10	9	8	7	6	5 4		3 2 A A	_	0 A
Rese	t 0x0	0000000		0	0	0	0	0	0 (0) (0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0 (0 (0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	on																		
Α	RW	PSELN									Α	nalo	g ne	gat	ive	inpu	ıt, e	nal	oles	dif	fere	ntia	l ch	ann	el							
			NC	0							N	ot co	onne	ecte	ed																	
			AnalogInput0	1							Α	IN0																				
			AnalogInput1	2							Α	IN1																				
			AnalogInput2	3							Α	IN2																				
			AnalogInput3	4							Α	IN3																				
			AnalogInput4	5							Α	IN4																				
			AnalogInput5	6							Α	IN5																				
			AnalogInput6	7							Α	IN6																				
			AnalogInput7	8							Α	IN7																				
			VDD	9							V	DD																				

37.11.20 CH[3].CONFIG

Address offset: 0x548

Input configuration for CH[3]

Bit	num	be	·		31	30 2	29 2	28 2	7 26	25	24	23 :	22 2	1 2	0 19	18	17	16	15	14 1	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id											G			F		Ε	Ε	Ε			D		С	С	С			В	В		Α	Α
Re	set 0	кO(020000		0	0	0	0 0	0	0	0	0	0 (0 (0	0	1	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RV	٧	Field	Value Id	Va	lue						Des	crip	tior	1																	
Δ	RV	V	RESP									Pos	itive	ch:	nne	ol re	sist	or c	ont	rol												



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id		G F E E E D C C C B B	A A
Reset 0x00020000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id RW Field	Value Id	Value Description	
	Bypass	0 Bypass resistor ladder	
	Pulldown	1 Pull-down to GND	
	Pullup	2 Pull-up to VDD	
	VDD1_2	3 Set input at VDD/2	
B RW RESN		Negative channel resistor control	
	Bypass	0 Bypass resistor ladder	
	Pulldown	1 Pull-down to GND	
	Pullup	2 Pull-up to VDD	
	VDD1_2	3 Set input at VDD/2	
C RW GAIN		Gain control	
	Gain1_6	0 1/6	
	Gain1_5	1 1/5	
	Gain1_4	2 1/4	
	Gain1_3	3 1/3	
	Gain1_2	4 1/2	
	Gain1	5 1	
	Gain2	6 2	
	Gain4	7 4	
D RW REFSEL		Reference control	
	Internal	0 Internal reference (0.6 V)	
	VDD1_4	1 VDD/4 as reference	
E RW TACQ		Acquisition time, the time the ADC uses to sample the input	
		voltage	
	3us	0 3 us	
	5us	1 5 us	
	10us	2 10 us	
	15us	3 15 us	
	20us	4 20 us	
	40us	5 40 us	
F RW MODE		Enable differential mode	
	SE	0 Single ended, PSELN will be ignored, negative input to ADC	
		shorted to GND	
	Diff	1 Differential	
G RW BURST		Enable burst mode	
	Disabled	O Burst mode is disabled (normal operation)	
	Enabled	1 Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of	
		samples as fast as it can, and sends the average to Data RAM.	

37.11.21 CH[3].LIMIT

Address offset: 0x54C

High/low limits for event monitoring a channel

Bit	number		31	30	29	28	27	26	25 :	24 :	23 2	22 2	21 2	0 1	9 1	8 17	7 10	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id			В	В	В	В	В	В	В	В	В	В	В	ВЕ	3 E	3 B	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	. A
Res	et 0x7FFF8000		0	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	l 1	. 1	1	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW Field	Value Id	Va	lue						- 1	Des	crip	tio	n																		
I d A	RW Field RW LOW	Value Id		lue 276		o +3	327	67]				crip / lev																				

37.11.22 CH[4].PSELP

Address offset: 0x550

Input positive pin selection for CH[4]



Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW PSELP			Analog positive input channel
	NC	0	Not connected
	AnalogInput0	1	AINO
	AnalogInput1	2	AIN1
	AnalogInput2	3	AIN2
	AnalogInput3	4	AIN3
	AnalogInput4	5	AIN4
	AnalogInput5	6	AIN5
	AnalogInput6	7	AIN6
	AnalogInput7	8	AIN7
	VDD	9	VDD

37.11.23 CH[4].PSELN

Address offset: 0x554

Input negative pin selection for CH[4]

Bit r	numbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	23 22	2 21	. 20	19	18	17	16	15	14	13	12 1	.1 1	9	8	7	6	5	3 2	! 1	0
	et 0x0	000000		0	0	0	0 0) (0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0
Id	RW	Field	Value Id	Va	lue						Desc	ripti	ion																	
Α	RW	PSELN									Analo	og n	ega	tive	inp	ut,	ena	able	es d	iffe	ent	ial c	han	nel						
			NC	0							Not o	conn	ect	ed																
			AnalogInput0	1							AIN0																			
			AnalogInput1	2							AIN1																			
			AnalogInput2	3							AIN2																			
			AnalogInput3	4							AIN3																			
			AnalogInput4	5							AIN4																			
			AnalogInput5	6							AIN5																			
			AnalogInput6	7							AIN6																			
			AnalogInput7	8							AIN7																			
			VDD	9							VDD																			

37.11.24 CH[4].CONFIG

Address offset: 0x558

Input configuration for CH[4]

Bit n	umbe	r		31	30 2	9 2	28 2	7 2	6 25	5 24	23 2	22 2	1 20	19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	6	5 -	4 3	2	1	0
Id										G			F		Ε	Ε	Ε			[)	С	С	С			В	В		Α	Α
Rese	t 0x0	0020000		0	0 0)	0 0) (0 0	0	0	0 0	0	0	0	1	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						Des	cript	tion																		
Α	RW	RESP									Posi	tive	cha	nne	l re	sist	or c	ont	rol												
			Bypass	0							Вур	ass r	esis	tor	lado	der															
			Pulldown	1							Pull	-dov	vn to	G۱	۱D																
			Pullup	2							Pull	-up t	to VI	DD																	
			VDD1_2	3							Set	inpu	t at	VDE)/2																
В	RW	RESN									Neg	ative	e cha	nn	el r	esis	tor	con	trol												
			Bypass	0							Вур	ass r	esis	tor	lado	der															
			Pulldown	1							Pull	-dov	vn to	G۱	۱D																
			Pullup	2							Pull	up t	to VI	DD																	
			VDD1_2	3							Set	inpu	t at	VDE)/2																
С	RW	GAIN									Gair	cor	ntrol																		
			Gain1_6	0							1/6																				
			Gain1_5	1							1/5																				



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Gain1_4	2 1/4
	Gain1_3	3 1/3
	Gain1_2	4 1/2
	Gain1	5 1
	Gain2	6 2
	Gain4	7 4
D RW REFSEL		Reference control
	Internal	0 Internal reference (0.6 V)
	VDD1_4	1 VDD/4 as reference
E RW TACQ		Acquisition time, the time the ADC uses to sample the input
		voltage
	3us	0 3 us
	5us	1 5 us
	10us	2 10 us
	15us	3 15 us
	20us	4 20 us
	40us	5 40 us
F RW MODE		Enable differential mode
	SE	O Single ended, PSELN will be ignored, negative input to ADC
		shorted to GND
	Diff	1 Differential
G RW BURST		Enable burst mode
	Disabled	0 Burst mode is disabled (normal operation)
	Enabled	1 Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
		samples as fast as it can, and sends the average to Data RAM.

37.11.25 CH[4].LIMIT

Address offset: 0x55C

High/low limits for event monitoring a channel

Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	B B B B B B	B B B B B B B B A A A A A A
Reset 0x7FFF8000	0 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW LOW	[-32768 to +32767]	Low level limit
B RW HIGH	[-32768 to +32767]	High level limit

37.11.26 CH[5].PSELP

Address offset: 0x560

Input positive pin selection for CH[5]

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Reset 0x00000000		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW PSELP			Analog positive input channel
	NC	0	Not connected
	AnalogInput0	1	AIN0
	AnalogInput1	2	AIN1
	AnalogInput2	3	AIN2
	AnalogInput3	4	AIN3
	AnalogInput4	5	AIN4
	AnalogInput5	6	AIN5



Bit number		31 30 29 28	27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id					$A \; A \; A \; A \; A$
Reset 0x00000000		0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	AnalogInput6	7	AIN6		
	AnalogInput7	8	AIN7		
	VDD	9	VDD		

37.11.27 CH[5].PSELN

Address offset: 0x564

Input negative pin selection for CH[5]

Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW PSELN			Analog negative input, enables differential channel
	NC	0	Not connected
	AnalogInput0	1	AIN0
	AnalogInput1	2	AIN1
	AnalogInput2	3	AIN2
	AnalogInput3	4	AIN3
	AnalogInput4	5	AIN4
	AnalogInput5	6	AIN5
	AnalogInput6	7	AIN6
	AnalogInput7	8	AIN7
	VDD	9	VDD

37.11.28 CH[5].CONFIG

Address offset: 0x568

Input configuration for CH[5]

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			G F E E E D C C C B B A A
Reset 0x00020000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
D RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)



Bit	numbe	er		31	30	29 2	28 2	7 2	6 25	5 24	23	22 2	1 20	19	18	17	16	15 :	14 1	3 12	2 11	10	9	8	7	6	5 4	1 3	2	1
Id										G			F		Ε	Ε	Ε			D)	С	С	С			ВЕ	3		Α
Res	et 0x0	00020000		0	0	0	0 0	0 (0	0	0	0 (0 0	0	0	1	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tion																	
			VDD1_4	1							VDI)/4 a	as re	fere	ence	•														
Е	RW	TACQ									Acq	uisit	tion 1	ime	e, th	ie ti	me	the	AD	C us	es to	saı	mpl	e th	e ir	put	t			
											volt	age																		
			3us	0							3 us	5																		
			5us	1							5 us	5																		
			10us	2							10 ι	ıs																		
			15us	3							15 ι	ıs																		
			20us	4							20 ι	ıs																		
			40us	5							40 ι	ıs																		
F	RW	MODE									Ena	ble (diffe	rent	tial	mo	de													
			SE	0							Sing	gle e	nded	d, PS	SELI	٧w	ill b	e ig	nore	ed, r	ega	tive	inp	ut t	o A	DC				
											sho	rted	to G	ND																
			Diff	1							Diff	erer	ntial																	
G	RW	BURST									Ena	ble l	burst	mo	ode															
			Disabled	0							Bur	st m	ode	is d	isab	led	(no	rma	al op	era	tion)								
			Enabled	1							Bur	st m	ode	is e	nab	led.	SA	ADO	C tak	es 2	٥^!	/ERS	SAN	1PLE	nu	ımb	er o	f		
											sam	ples	s as f	ast	as i	t ca	n, a	nd s	send	ls th	e av	era	ge t	o D	ata	RAN	M.			

37.11.29 CH[5].LIMIT

Address offset: 0x56C

High/low limits for event monitoring a channel

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α	ΑА
Res	et 0x7	7FFF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	LOW		[-3	3276	58 t	0 +	327	767]			Lov	v le	vel	lim	it																		
				[-3									th le																					

37.11.30 CH[6].PSELP

Address offset: 0x570

Input positive pin selection for CH[6]

Bit r	numbe	er		31	30	29 :	28 2	7 2	6 25	5 24	23 2:	2 21	20	19 1	L8 1	.7 1	6 15	5 14	13	12	11	10	9	8	7	6 !	5 4	 2 . A	_	Ο Δ
	et 0x0	0000000		0	0	0	0 () (0 0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 () (
Id	RW	Field	Value Id	Va	lue						Desc	riptic	n																	
Α	RW	PSELP									Anal	og po	siti	ve ir	npu	t ch	ann	el												_
			NC	0							Not o	conne	ecte	ed																
			AnalogInput0	1							AIN0																			
			AnalogInput1	2							AIN1																			
			AnalogInput2	3							AIN2																			
			AnalogInput3	4							AIN3																			
			AnalogInput4	5							AIN4																			
			AnalogInput5	6							AIN5																			
			AnalogInput6	7							AIN6																			
			AnalogInput7	8							AIN7																			
			VDD	9							VDD																			

37.11.31 CH[6].PSELN

Address offset: 0x574

Input negative pin selection for CH[6]



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PSELN		Analog negative input, enables differential channel
	NC	0 Not connected
	AnalogInput0	1 AINO
	AnalogInput1	2 AIN1
	AnalogInput2	3 AIN2
	AnalogInput3	4 AIN3
	AnalogInput4	5 AIN4
	AnalogInput5	6 AIN5
	AnalogInput6	7 AIN6
	AnalogInput7	8 AIN7
	VDD	9 VDD

37.11.32 CH[6].CONFIG

Address offset: 0x578

Input configuration for CH[6]

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			G F E E E D C C C B B A A
Reset 0x00020000		0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
D RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
E RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
F RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential



Bitı	numb	er		3	1 30	29	28	8 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	11 1	.0	9	8 7	7 6	5 5	4	3	2	1	0
Id											G				F		Ε	Ε	Ε				D		C I	С	С		В	В			Α	Α
Res	et Ox	00020000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alue	•						De	scri	ptic	on																			
G	RW	BURST										En	able	e bu	ırst	mo	de																	
			Disabled	0								Bu	ırstı	mod	de i	s di	sab	led	(no	orm	al o	per	atio	n)										
			Enabled	1								Bu	ırstı	mod	de i	s er	nab	led	. SA	AD	C ta	kes	2^0	OVE	RSA	١M	PLE	nur	nbe	r of				
												saı	mpl	es a	s fa	st a	as i	t ca	n, a	ınd	sen	ds t	he a	ave	rag	e to	Da	ta R	AN	1.				

37.11.33 CH[6].LIMIT

Address offset: 0x57C

High/low limits for event monitoring a channel

Bit r	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	1 2	0 19	18	3 17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1 0
Id				В	В	В	В	В	В	В	В	В	В	3 E	3 B	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Α,	4 А
Res	et 0x7	FFF8000		0	1	1	1	1	1	1	1	1	1 :	1 :	l 1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	1																		
Α	RW	LOW		[-3	3276	58 t	o +3	327	67]			Low	lev /	el li	mit																		

37.11.34 CH[7].PSELP

Address offset: 0x580

Input positive pin selection for CH[7]

Bit r	numbe	er		31	30 2	29 2	8 27	7 26	25 2	24 :	23 22	2 21	20	19	18 1	.7 1	6 1	.5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																												Α.	А А	Α	Α
Res	et 0x0	0000000		0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0 (0 (0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue					ı	Desci	riptic	n																		
Α	RW	PSELP								,	Analo	og po	siti	ve i	npu	t ch	anr	nel													
			NC	0						ı	Not c	onne	ecte	ed																	
			AnalogInput0	1						,	AINO																				
			AnalogInput1	2						,	AIN1																				
			AnalogInput2	3						,	AIN2																				
			AnalogInput3	4						,	AIN3																				
			AnalogInput4	5						,	AIN4																				
			AnalogInput5	6						,	AIN5																				
			AnalogInput6	7						,	AIN6																				
			AnalogInput7	8						,	AIN7																				
			VDD	9						١	/DD																				

37.11.35 CH[7].PSELN

Address offset: 0x584

Input negative pin selection for CH[7]

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id	ААА	. A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id RW Field Value Id	Value Description	
A RW PSELN	Analog negative input, enables differential channel	
NC	0 Not connected	
AnalogInput0	1 AINO	
AnalogInput1	2 AIN1	
AnalogInput2	3 AIN2	
AnalogInput3	4 AIN3	
AnalogInput4	5 AIN4	
AnalogInput5	6 AIN5	



Bit number		31	30 2	9 2	8 2	7 26	25	24	23	22 :	21 2	20 1	.9 1	8 1	7 1	6 15	5 14	13	12	11 1	0 9	8	7	6	5	4	3	2 1	1 0
Id																										Α	Α	A A	A A
Reset 0x00000000		0	0	0 0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0
ld RW Field	Value Id	Val	ue						De	scrip	otio	n																	
	AnalogInput6	7							ΑIN	16																			
	AnalogInput7	8							AIN	17																			
	VDD	9							VD	D																			

37.11.36 CH[7].CONFIG

Address offset: 0x588

Input configuration for CH[7]

Bit	numb	er		31 30	29	9 28	27	26 2	25 2	4 2	3 22	21	20	19	18	17	16	15	14	13	3 12	2 1:	1 10) 9	8	7	6	5	4	3	2	1	0
Id									G	à			F		Ε	Ε	Ε				D		С	С	С			В	В			Α	Α
Res	et 0x0	00020000		0 0	0	0	0	0	0 0) (0 0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Value							escri																						
Α	RW	RESP								Р	ositiv	ve c	har	nnel	res	sist	or	con	tro	ı													
			Bypass	0						В	ypas	s re	sist	tor I	ado	der																	
			Pulldown	1						Р	ull-d	owr	ı to	GN	D																		
			Pullup	2						Р	ull-u	p to	VE	DD																			
			VDD1_2	3						S	et in	put	at ۱	VDD	/2																		
В	RW	RESN								١	legat	ive	cha	anne	el re	esis	to	coı	ntr	ol													
			Bypass	0						В	ypas	s re	sist	tor I	ado	der																	
			Pulldown	1						Р	ull-d	owr	n to	GN	D																		
			Pullup	2						Р	ull-u	p to	VE	DD																			
			VDD1_2	3						S	et in	put	at ۱	VDD	/2																		
С	RW	GAIN								C	ain c	ont	rol																				
			Gain1_6	0						1	/6																						
			Gain1_5	1						1	/5																						
			Gain1_4	2						1	/4																						
			Gain1_3	3						1	/3																						
			Gain1_2	4						1	/2																						
			Gain1	5						1																							
			Gain2	6						2																							
			Gain4	7						4																							
D	RW	REFSEL								R	efere	ence	e co	ontr	ol																		
			Internal	0						li	ntern	al r	efe	ren	ce ((0.6	٧																
			VDD1_4	1						٧	DD/4	1 as	ref	fere	nce	9																	
Ε	RW	TACQ								Δ	cquis	sitio	n t	ime	, th	ne ti	m	e th	e A	DC	us	es t	o sa	m	ole 1	he	inp	ut					
										٧	oltag	e																					
			3us	0						3	us																						
			5us	1						5	us																						
			10us	2						1	0 us																						
			15us	3						1	5 us																						
			20us	4						2	0 us																						
			40us	5						4	0 us																						
F	RW	MODE								Е	nable	e dit	ffer	ent	ial	mo	de																
			SE	0						S	ingle	end	ded	l, PS	ELI	N w	ill	be i	gno	ore	d, n	ega	ativ	e in	put	to	AD	2					
										S	horte	ed to	o G	ND																			
			Diff	1							iffer																						
G	RW	BURST									nable																						
			Disabled	0							urst						•																
			Enabled	1							urst																						
										S	ampl	es a	s f	ast a	as it	t ca	n,	and	se	nd:	s th	e a	ver	age	to	Dat	a R	٩M					

37.11.37 CH[7].LIMIT

Address offset: 0x58C



High/low limits for event monitoring a channel

Bit r	num	ber			31	. 30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	L8 1	17 1	.6 1	L5 1	14 1	13 :	12	11 1	LO	9	8 7	7 (5 5	4	3	2	1	0
Id					В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В.	Α.	Α	Α	Α	Α.	Α.	A .	A A	λ /	Δ Δ		A	Α	Α	Α
Res	et O	x7F	FF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1	0	0	0	0	0	0	0 () (0	0	0	0	0	0
Id	R۱	N	Field	Value Id	Va	lue							De	scri	ptio	n																			ı
Α	R۷	N	LOW		[-3	3276	8 t	0 +3	327	'67]			Lov	v le	vel	limi	t																		_
В	R۱	Ν	HIGH		[-3	3276	8 t	0 +3	327	67]			Hig	sh le	vel	lim	it																		

37.11.38 RESOLUTION

Address offset: 0x5F0
Resolution configuration

Bitı	numbe	er		31 30 2	9 28 2	7 26	25 2	24 2	3 22	2 21	. 20	19 3	18 1	7 16	5 15	14	13 1	2 11	. 10	9	8	7	6 5	5 4	3	2	1 0
Id																										Α	A A
Res	et OxO	0000001		0 0 0	0 (0 0	0 (0 0	0	0	0	0	0 (0 0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0 1
Id	RW	Field	Value Id	Value				D	esci	ripti	ion																
Α	RW	VAL						S	et th	ne re	esol	utio	n														
			8bit	0				8	bit																		
			10bit	1				10	0 bit	t																	
			12bit	2				1	2 bit	t																	
			14bit	3				1	4 bit	t																	

37.11.39 OVERSAMPLE

Address offset: 0x5F4

Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description	
A RW OVERSAMPL	E	Oversample con	crol
	Bypass	0 Bypass oversam	oling
	Over2x	1 Oversample 2x	
	Over4x	2 Oversample 4x	
	Over8x	3 Oversample 8x	
	Over16x	4 Oversample 16x	
	Over32x	5 Oversample 32x	
	Over64x	6 Oversample 64x	
	Over128x	7 Oversample 128	·
	Over256x	8 Oversample 256	•

37.11.40 SAMPLERATE

Address offset: 0x5F8

Controls normal or continuous sample rate

Bit r	iumbe	er		31 30 29 28 2	7 26 2	25 24	23 2	22 21	. 20	19 1	18 1	7 16	15 3	14 1	3 12	11 1	.0 9	8	7	6	5	4	3 2	2 1	. 0
Id															В		4 Δ	A	Α	Α	Α	Α	A A	A A	A
Res	et 0x0	0000000		0 0 0 0	0 0	0 0	0 (0 0	0	0	0 0	0	0	0 0	0	0	0 0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Value			Des	cripti	ion																
Α	RW	CC		[802047]			Capt	ture a	and	com	pare	e valı	ue. S	amp	le ra	te is	16 N	ИHz	/CC						
В	RW	MODE					Sele	ct m	ode	for s	samp	ole ra	ate c	ontr	ol										
			Task	0			Rate	is co	ontr	olled	d fro	m SA	MPI	LE ta	sk										
			Timers	1			Rate	is co	ontr	olled	d fro	m lo	cal ti	imer	(use	CC t	о сс	ntro	ol th	ie ra	ate)				



37.11.41 RESULT.PTR

Address offset: 0x62C

Data pointer

Bit number		31	30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	3 7	7 6	5 5	5 4	3	2	1	0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	4 /	A A	\ A	Δ Δ	A	Α	Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () () (0	0	0	0	0
Id RW Field	Value Id	Va	alue							De	scri	pti	on																				
A RW PTR										Da	ta r	noin	ter																				

37.11.42 RESULT.MAXCNT

Address offset: 0x630

Maximum number of buffer words to transfer

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	7 16 15 14 13 12 11 10 9	9 8 7 6 5	4 3 2 1 0
Id				AAAAAA	A A A A A	A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	00000000	0 0 0 0	0 0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW MAXCNT			Maximum number of	buffer words to transfer		,

37.11.43 RESULT.AMOUNT

Address offset: 0x634

Number of buffer words transferred since last START

Bit	numb	er		31 3	0 29	28	27	26	25 2	24 2	23 2	2 21	. 20	19	18	17 1	16 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	1 0
Id																		A	. Δ	A	Α	Α	Α	Α	Α	Α	Α	Α.	А А	. 4	A A
Re	set 0x	00000000		0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0 0
Id	RW	/ Field	Value Id	Valu	ie						Desc	ript	ion																		
Α	R	AMOUNT								١	lum	ber	of b	ouffe	r w	ord	s tra	nsf	erre	d si	nce	last	t ST	AR	Г. Т	his					

register can be read after an END or STOPPED event.

37.12 Electrical Specification

37.12.1 SAADC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
DNL	Differential non-linearity, 10-bit resolution	-0.95	<1		LSB
INL	Integral non-linearity, 10-bit resolution		1		LSB
V _{OS}	Differential offset error (calibrated), 10-bit resolution ^a		+-2		LSB
C_{EG}	Gain error temperature coefficient		0.02		%/°C
f _{SAMPLE}	Maximum sampling rate			200	kHz
t _{ACQ,10k}	Acquisition time (configurable), source Resistance <= 10kOhm		3		μs
t _{ACQ,40k}	Acquisition time (configurable), source Resistance <= 40kOhm		5		μs
t _{ACQ,100k}	Acquisition time (configurable), source Resistance <= 100kOhm		10		μs
t _{ACQ,200k}	Acquisition time (configurable), source Resistance <= 200kOhm		15		μs
t _{ACQ,400k}	Acquisition time (configurable), source Resistance <= 400kOhm		20		μs
t _{ACQ,800k}	Acquisition time (configurable), source Resistance <= 800kOhm		40		μs
t _{CONV}	Conversion time		<2		μs
I _{ADC,CONV}	ADC current during ACQuisition and CONVersion		700		μΑ
I _{ADC,IDLE}	Idle current, when not sampling, excluding clock sources and		<5		μΑ
	regulator base currents ³²				

^a Digital output code at zero volt differential input.

When t_{ACQ} is 10us or longer, and if DC/DC is active, it will be allowed to work in refresh mode if no other resource is requiring a high quality power supply from 1V3. If t_{ACQ} is smaller than 10us and DC/DC is active,



Symbol	Description	Min.	Тур.	Max.	Units
E _{G1/6}	Error ^b for Gain = 1/6	-3		3	%
E _{G1/4}	Error ^b for Gain = 1/4	-3		3	%
E _{G1/2}	Error ^b for Gain = 1/2	-3		4	%
E _{G1}	Error ^b for Gain = 1	-3		4	%
C _{SAMPLE}	Sample and hold capacitance at maximum gain ³³		2.5		pF
R _{INPUT}	Input resistance		>1		ΜΩ
E _{NOB}	Effective number of bits, differential mode, 12-bit resolution,		9		Bit
	1/1 gain, 3 μs acquisition time, crystal HFCLK, 200 ksps				
S _{NDR}	Peak signal to noise and distortion ratio, differential mode, 12-		56		dB
	bit resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200 $$				
	ksps				
S _{FDR}	Spurious free dynamic range, differential mode, 12-bit		70		dBc
	resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200				
	ksps				
R _{LADDER}	Ladder resistance		160		kΩ

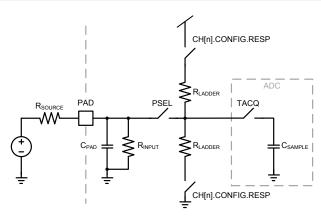


Figure 104: Model of SAADC input (one channel)

Note: SAADC average current calculation for a given application is based on the sample period, conversion and acquisition time (t_{conv} and t_{ACQ}) and conversion and idle current ($t_{ADC,CONV}$). For example, sampling at 4kHz gives a sample period of 250 μ s. The average current consumption would then be:

$$I_{AVERAGE} = \left(\frac{\left(t_{CONV} + t_{ACQ}\right)}{250}\right) \left(I_{ADC,CONV}\right) + \left(\frac{250 - \left(t_{CONV} + t_{ACQ}\right)}{250}\right) \left(I_{ADC,IDLE}\right)$$

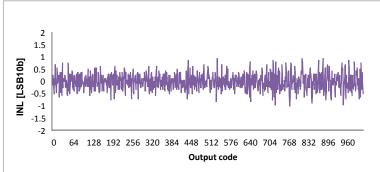


Figure 105: ADC INL vs Output Code

refresh mode will not be allowed, and it will remain in normal mode from the START task to the STOPPED event. So depending on t_{ACQ} and other resources' needs, the appropriate base current needs to be taken into account.

^b Does not include temperature drift

³³ Maximum gain corresponds to highest capacitance.



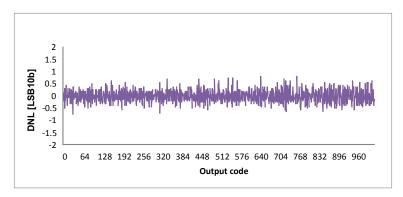


Figure 106: ADC DNL vs Output Code

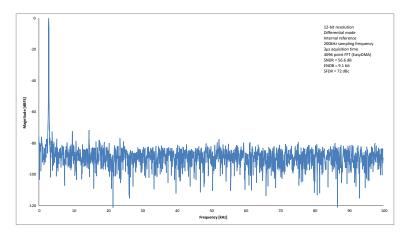


Figure 107: FFT of a 2.8 kHz sine at 200 ksps ()

37.13 Performance factors

Clock jitter, affecting sample timing accuracy, and circuit noise can affect ADC performance.

Jitter can be between START tasks or from START task to acquisition. START timer accuracy and startup times of regulators and references will contribute to variability. Sources of circuit noise may include CPU activity and the DC/DC regulator. Best ADC performance is achieved using START timing based on the TIMER module, HFXO clock source, and Constant Latency mode.



38 COMP — Comparator

The Comparator (COMP) compares the input voltage (VIN+) that is derived from an analog input pin selected via the PSEL register against a second input voltage (VIN-) that can be derived from multiple sources depending on operation mode.

Listed here are the main features for COMP:

- Input range from 0 V to VDD
- Single-ended mode
 - · Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
 - · Configurable 50 mV hysteresis
- Reference inputs:
 - VDD
 - External reference from AIN0 to AIN1 (between 0 V and VDD)
 - Internal references 1.2 V, 1.8 V and 2.4 V
- · Three operation modes: low power, normal and high-speed
- · Single-pin capacitive sensor support
- · Event generation on output changes
 - UP event on VIN- > VIN+
 - DOWN event on VIN- < VIN+
 - CROSS event on VIN+ and VIN- crossing
 - READY event on core and internal reference (if used) ready

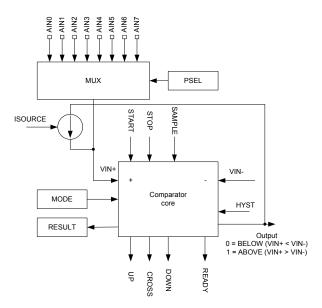


Figure 108: Comparator overview

Important: COMP cannot be used (STARTed) at the same time as LPCOMP. Only one comparator can be used at a time.

The COMP is started by triggering the START task, and stopped by triggering the STOP task. After a startup time of t_{COMP.START} ³⁴ the COMP will generate a READY event to indicate that the comparator is ready

See t_{PROPDLY,LP}, t_{PROPDLY,N}, t_{PROPDLY,HS}, I_{COMP,LP}, I_{COMP,N} and I_{COMP,HS} in *Electrical parameters* for more information about COMP speed and power characteristics related to these different modes.



to use and the output of the COMP is correct. When the COMP module is started, events will be generated every time VIN+ crosses VIN-.

VIN- can be derived directly from AIN0 or AIN1 in differential mode, or VREF in single-ended mode. VUP and VDOWN thresholds can be set to implement a hysteresis on VIN- using the Reference Ladder. VREF can be derived from VDD, AIN0, AIN1 or internal 1.2V, 1.8V and 2.4V references.

An upward crossing will generate an UP event and a downward crossing will generate a DOWN event. The CROSS event will be generated every time there is a crossing, independent of direction.

An optional hysteresis on VIN+ and VIN- can be enabled when the module is used in differential mode through the HYST register. In single ended mode the two reference ladders (VUP and VDOWN, see *Figure 111: Comparator in single-ended mode* on page 390) will be used instead of the hysteresis mechanism configured in HYST.

This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 112: Hysteresis example where VIN+ starts below VUP* on page 390 for illustration of the effect of an active hysteresis on a noisy input signal.

The COMP can be configured to operate in two main operation modes, differential mode and single-ended mode, see MODE register for more information.

The COMP can, for both main operation modes, operate in different speed and power consumption modes, see MODE register. High-speed mode will consume more power compared to low-power mode, and low-power mode will result in slower response time compared to high-speed mode.

The immediate value of the COMP can be sampled to the RESULT register by triggering the SAMPLE task.

A selectable current can be applied (ISOURCE register) on the currently selected AINx line. Enabling the block creates a feedback path around the comparator, forming a relaxation oscillator. The circuit will sink current from VIN+ when the comparator output is high, and source current into VIN+ when the comparator output is low. The frequency of the oscillator is dependent on the capacitance at the analog input pin, the reference voltages and the value of the current source. In this mode, only a capacitive sensor needs to be attached between the analog input pin and ground. With a selected current of 10 μ A, VUP-VDOWN equal to 1 V, and an external capacity of typically 10 pF, the resulting oscillation frequency is around 500 kHz.

The frequency of the oscillator can be calculated as

```
f OSC = I SOURCE / (2C · (VUP-VDOWN) )
```

38.1 Shared resources

The COMP shares analog resources with the SAADC and LPCOMP peripherals.

While it is possible to use SAADC at the same time as COMP or LPCOMP, COMP and LPCOMP are mutually exclusive: enabling one will automatically disable the other. In addition, when using SAADC and COMP or LPCOMP simultaneously, it is not possible to select the same analog input pin for both modules.

Important: The COMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has stopped. Failing to do so may result in unpredictable behaviour.

38.2 Differential mode

In differential mode, the reference input VIN- is derived directly from one of the AINx pins.

In this mode, the impedance on VIN-'s signal path is equal to the impedance on VIN+'s signal path. See $Z_{COMPVINP}$ and $Z_{COMPVINND}$ for more information. In differential mode, the PSEL, MODE and EXTREFSEL registers must be configured before the COMP is enabled via the ENABLE register. When HYST is turned on while in this mode, the Output of the comparator (and associated events) will change from ABOVE to BELOW whenever VIN+ becomes smaller than (VIN- - ($V_{DIFFHYST}$ / 2)). Similarly, it will change from BELOW to ABOVE whenever VIN+ becomes larger than (VIN- + ($V_{DIFFHYST}$ / 2)), as illustrated in *Figure 110: Hysteresis enabled in differential mode* on page 389.



Restriction: Depending on the device, not all the analog inputs may be available for each MUX.

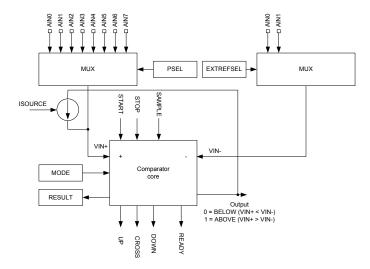


Figure 109: Comparator in differential mode

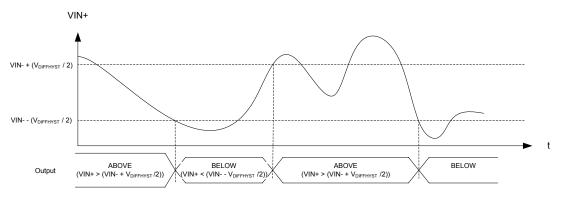


Figure 110: Hysteresis enabled in differential mode

38.3 Single-ended mode

In single-ended mode, VIN- is derived from the Reference Ladder.

The Reference Ladder uses the reference voltage VREF to derive two new voltage references, VUP and VDOWN. VUP and VDOWN are configured via THUP and THDOWN in the TH register. VREF can be sourced from any of the available references sources as illustrated in *Figure 111: Comparator in single-ended mode* on page 390. This is configured via EXTREFSEL and REFSEL.

When the comparator core detects that VIN+ > VIN-, i.e. ABOVE as per the RESULT register, VIN- will switch to VDOWN. When VIN- falls below VIN- again, VIN- will be switched back to VUP. By specifying VUP larger than VDOWN, a hysteresis as illustrated in *Figure 112: Hysteresis example where VIN+ starts below VUP* on page 390 and *Figure 113: Hysteresis example where VIN+ starts above VUP* on page 391 can be generated. In single-ended mode, the PSEL, MODE, EXTREFSEL, REFSEL and TH registers must be configured before the COMP is enabled via the ENABLE register.

Restriction: Depending on the device, not all the analog inputs may be available for each MUX.

Writing to the HYST register has no effect in single-ended mode, and the content of this register is ignored.



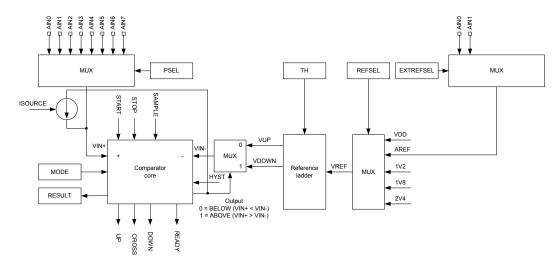


Figure 111: Comparator in single-ended mode

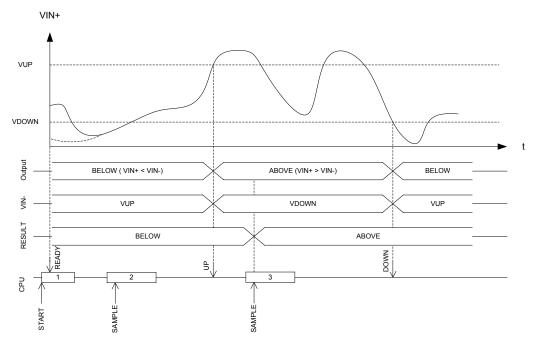


Figure 112: Hysteresis example where VIN+ starts below VUP



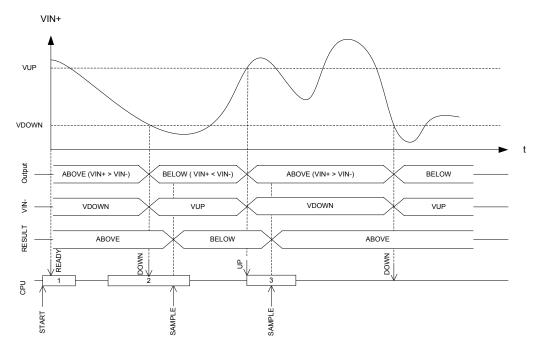


Figure 113: Hysteresis example where VIN+ starts above VUP

38.4 Pin configuration

The user can use the PSEL register to select one of the analog input pins, AINO through AINO, as input VIN +.

See *Figure 111: Comparator in single-ended mode* on page 390. Similarly the user can use the EXTREFSEL register to select one of the AINx analog input pins as reference input, in case AREF is selected in REFSEL. The selected analog pins will be acquired by the COMP when it is enabled via the ENABLE register.

Depending on the device, not all the analog inputs may be available for each MUX. See PSEL and EXTREFSEL register definition for more information about which analog pins are available on a particular device.

38.5 Registers

Table 87: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40013000	COMP	COMP	General Purpose Comparator	

Table 88: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	COMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt



Register	Offset	Description
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	COMP enable
PSEL	0x504	Pin select
REFSEL	0x508	Reference source select
EXTREFSEL	0x50C	External reference select
TH	0x530	Threshold configuration for hysteresis unit
MODE	0x534	Mode configuration
HYST	0x538	Comparator hysteresis enable
ISOURCE	0x53C	Current source select on analog input

38.5.1 SHORTS

Address offset: 0x200 Shortcut register

О.	.00	at regioter			
Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E D C B A
Res	set 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY_SAMPLE			Shortcut between READY event and SAMPLE task
					See EVENTS_READY and TASKS_SAMPLE
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
В	RW	READY_STOP			Shortcut between READY event and STOP task
					See EVENTS_READY and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
С	RW	DOWN_STOP			Shortcut between DOWN event and STOP task
					See EVENTS_DOWN and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW	UP_STOP			Shortcut between UP event and STOP task
					See EVENTS_UP and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
Ε	RW	CROSS_STOP			Shortcut between CROSS event and STOP task
					See EVENTS_CROSS and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

38.5.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	numbe	er		31	. 30	29	28	27	26 2	25 :	24 2	23 2	22 2	21 2	0 1	9 18	3 17	7 16	15	14	13	12	11 :	10 9	9 (3 7	6	5	4	3	2	1 0
Id																														D	С	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							Des	crip	tion																		
Α	RW	READY									E	Enal	ble	or d	isal	ble i	nte	rru	ot fo	or R	EAD)Y e	ven	t								
											9	See	EVE	ENTS	5_ <i>R</i>	EAL	γ															
			Disabled	0							[Disa	ble																			
			Enabled	1							E	Enal	ble																			
В	RW	DOWN									E	Enal	ble	or d	isal	ble i	nte	rru	ot fo	or D	OW	/N e	ven	t								
											9	See	EVE	ENTS	5_D	ow	'N															



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	5 4 3 2 1 0
Id			D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0
Id RW Field	Value Id	Value Description	
	Disabled	0 Disable	
	Enabled	1 Enable	
C RW UP		Enable or disable interrupt for UP event	
		See EVENTS_UP	
	Disabled	0 Disable	
	Enabled	1 Enable	
D RW CROSS		Enable or disable interrupt for CROSS event	
		See EVENTS_CROSS	
	Disabled	0 Disable	
	Enabled	1 Enable	

38.5.3 INTENSET

Address offset: 0x304

Enable interrupt

Bitı	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Enable interrupt for READY event
					See EVENTS_READY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	DOWN			Write '1' to Enable interrupt for DOWN event
					See EVENTS_DOWN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	UP			Write '1' to Enable interrupt for UP event
					See EVENTS_UP
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	CROSS			Write '1' to Enable interrupt for CROSS event
					See EVENTS_CROSS
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

38.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

it nu	umbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	5 5	5 4	3	2	1	0
t																															D	С	В	Α
ese	t 0x0(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
t	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
	RW	READY										Wı	rite	'1' t	o D	isal	ble	int	erru	ıpt	for	REA	٩DY	eve	ent									
												Se	e <i>E</i> \	/EN	TS_	REA	ADY	,																
			Clear	1								Dis	sabl	e																				
	d ese	eset 0x00	eset 0x00000000 d RW Field	d reset 0x00000000000000000000000000000000000	d reset 0x00000000 0 0 d RW Field Value Id Value	d reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0	d reset 0x00000000	d reset 0x00000000	deset 0x00000000	See EVENTS_READY	See EVENTS_READY	See EVENTS_READY See See See See See See See See See S	See EVENTS_READY See EVENTS_	See EVENTS_READY	See EVENTS_READY See EVENTS_	See EVENTS_READY See EVENTS_	See EVENTS_READY See EVENTS_	See EVENTS_READY See EVENTS_	See EVENTS_READY See EVENTS_	See EVENTS_READY See EVENTS_	See EVENTS_READY See EVENTS_	See EVENTS_READY See EVENTS_	See EVENTS_READY	See EVENTS_READY See EVENTS_	Description RW Field Value Id Value Write '1' to Disable interrupt for READY event See EVENTS_READY	D C cleset 0x000000000	D C B A READY D C B A READY							



numbe	er		31 30 29 28 27 26 25 24	\$ 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
				D C B A
et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
RW	Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
RW	DOWN			Write '1' to Disable interrupt for DOWN event
				See EVENTS_DOWN
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
RW	UP			Write '1' to Disable interrupt for UP event
				See EVENTS_UP
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
RW	CROSS			Write '1' to Disable interrupt for CROSS event
				See EVENTS_CROSS
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
	RW RW	et 0x00000000 RW Field RW DOWN RW UP	et 0x00000000 RW Field Value Id Disabled Enabled RW DOWN Clear Disabled Enabled RW UP Clear Disabled Enabled RW UP Clear Disabled Enabled Clear Disabled Enabled Clear Disabled Enabled	et 0x000000000

38.5.5 RESULT

Address offset: 0x400

Compare result

Bit	numbe	er		31 3	0 29	28	3 27	26	25	24	23	22	21 :	20 1	19 1	l8 1	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																Α
Res	et OxC	0000000		0 (0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Valu	e						De	scri	ptio	n																		
Α	R	RESULT									Res	sult	of I	ast	con	npai	e. I	Deci	isio	n po	oint	SAN	1PLE	E ta	sk.							
			Below	0							Inp	ut v	olta	age	is b	elo	w tl	ne t	hre	sho	ld (\	/IN+	< V	IN-)							
			Above	1							Inp	ut v	olta	age	is a	bov	e tl	ne t	hre	sho	ld (\	/IN+	> V	IN-)							

38.5.6 ENABLE

Address offset: 0x500

COMP enable

Bit	numbe	er		31 30	29	28	27 2	26 2	25 2	24 2	3 2	2 2	1 20	19	18	17	16	15	14	13 :	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																															А А
Res	et 0x0	0000000		0 0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	:					D	esc	ript	tion																		
Α	RW	ENABLE								Ε	nab	ole c	or di	sabl	e C	ОМ	ΙP														
			Disabled	0						D	isal	hle																			
			Disabica	U						_		٠.٠																			

38.5.7 PSEL

Address offset: 0x504

Pin select

Bit number	31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id				A A A
Reset 0x00000000	0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description		
A RW PSEL		Analog pin select		



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	ААА
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
AnalogInput0	0 AINO selected as analog input
AnalogInput1	1 AIN1 selected as analog input
AnalogInput2	2 AIN2 selected as analog input
AnalogInput3	3 AIN3 selected as analog input
AnalogInput4	4 AIN4 selected as analog input
AnalogInput5	5 AIN5 selected as analog input
AnalogInput6	6 AIN6 selected as analog input
AnalogInput7	7 AIN7 selected as analog input

38.5.8 REFSEL

Address offset: 0x508 Reference source select

Bit r	numbe	er		31	1 30	29	2	8 2	7 2	26 :	25	24	23	22	21	20	19	18	3 1	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 9	8	3 7	6	5	4	3	2	1	0
Id																																		Α	Α	Α
Res	et 0x0	000004		0	0	0	C	0)	0	0	0	0	0	0	0	0	0	C	0) () () () (0 (0 (0	C	0	0	0	0	0	1	0	0
Id	RW	Field	Value Id	Va	alue								De	scr	ipti	on																				
Α	RW	REFSEL											Re	fere	enc	e se	ele	ct																		
			Int1V2	0									VR	EF:	= in	ter	nal	1.2	2 V	ref	ere	nce	(V	DD	>=	1.7	V)									
			Int1V8	1									VR	EF:	= in	ter	nal	1.8	3 V	ref	ere	nce	(V	DD	>=	VRE	F +	0.2	2 V)							
			Int2V4	2									VR	EF:	= in	ter	nal	2.4	1 V	ref	ere	nce	(V	DD	>=	VRE	F +	0.2	2 V)							
			VDD	4									VR	EF:	= V	DD																				
			ARef	7									VR	EF:	= A	REF	(V	DD	>=	VR	EF	>=	ARE	FΝ	1IN)										

38.5.9 EXTREFSEL

Address offset: 0x50C External reference select

Bit	numl	ber			3:	1 30	29	28	3 27	26	5 25	24	23	22	21	20	19	18	17 :	16 :	15 :	14	13	12 :	11 1	.0 9	Э	8	7	6	5	4 3	2	1	0
Id																																			Α
Res	et Ox	x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (0	0	0	0 (0	0	0
Id	RV	V I	Field	Value Id	V	alue	•						De	scri	ptio	on																			
Α	RV	V I	EXTREFSEL										Ex	tern	al a	ınal	og r	efe	ren	ce s	sele	ct													
				AnalogReference0	0								Us	e Al	IN0	as e	exte	rna	l an	alo	g re	efei	en	ce											
				AnalogReference1	1								Us	e Al	IN1	as e	exte	rna	l an	alo	g re	efei	en	ce											

38.5.10 TH

Address offset: 0x530

Threshold configuration for hysteresis unit

Bit r	numb	er		31	. 30	29	28	27	26	25	24	23	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id																						В	В	В	В	В	В			Α	Α	A A	۱ ۱	A А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	crip	otic	n																			
Α	RW	THDOWN		[6	3:0]							VD	ОW	N =	(TI	HDO	ЭW	N+	1)/6	54*	VRI	F												
В	RW	THUP		[6	3:0]							VU	P = 1	(TH	UP.	+1)	/64	*V	REF															

38.5.11 MODE

Address offset: 0x534 Mode configuration



Bit n	numbe	er		31 3	0 29	28	27	26 25	5 24	23	22	21 2	0 19	18	17	16 1	5 1	4 13	12	11 1	.0 9	8	7	6	5 -	4 3	2	1 0
Id																						В						A A
Rese	et 0x0	0000000		0 0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 (0 (0	0	0	0 0	0	0	0	0	0 0	0	0 0
Id	RW	Field	Value Id	Valu	е					De	scrip	ption	ı															
Α	RW	SP								Spe	eed	and	oow	er n	node	è												
			Low	0						Lov	w po	wer	mod	de														
			Normal	1						No	rma	l mo	de															
			High	2						Hig	gh sp	oeed	mod	de														
В	RW	MAIN								Ma	ain o	pera	tion	mc	de													
			SE	0						Sin	igle e	ende	d m	ode														
			Diff	1						Dif	fere	ntial	mo	de														

38.5.12 HYST

Address offset: 0x538

Comparator hysteresis enable

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A
Reset 0x00000000		0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
A RW HYST			Comparator hysteresis
	NoHyst	0	Comparator hysteresis disabled
	Hyst50mV	1	Comparator hysteresis enabled

38.5.13 ISOURCE

Address offset: 0x53C

Current source select on analog input

Bit	numbe	er		31	L 30	29	28	27	' 26	25	5 24	1 23	3 22	2 21	20	19	18	3 17	7 16	5 15	5 14	13	3 12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	esc	ripti	ion																				
Α	RW	ISOURCE										C	omį	oara	itor	hy:	ste	resi	s																_
			Off	0								Cı	urre	ent s	sou	rce	dis	abl	ed																
			len2mA5	1								Cı	urre	ent s	sou	rce	en	able	ed (+/-	2.5	uA)												
			len5mA	2								Cı	urre	ent s	sou	rce	en	able	ed (+/-	5 u	A)													
			len10mA	3								Cı	urre	ent s	sou	rce	en	able	ed (+/-	10	uA)													

38.6 Electrical Specification

38.6.1 COMP Electrical Specification

Symbol D	Description	Min.	Тур.	Max.	Units
I _{COMP,LP} C	ore run current in low power mode		2		μΑ
I _{COMP,N} C	ore run current in normal mode		5		μΑ
I _{COMP,HS} C	ore run current in high-speed mode		10		μΑ
t _{PROPDLY,LP} P	ropagation delay, low power mode ^a		0.6		μS
t _{PROPDLY,N} P	ropagation delay, normal mode ^a		0.2		μS
t _{PROPDLY,HS} P	ropagation delay, high-speed mode ^a		0.1		μS
I _{SOURCE} C	onfigurable input current provided by the output driven				μΑ
CI	urrent source.				
I _{SOURCE,A}			2.5		μΑ
I _{SOURCE,B}			5.0		μΑ
I _{SOURCE,C}			10.0		μΑ

^a Propagation delay is with 10mV overdrive.



Symbol	Description	Min.	Тур.	Max.	Units
V _{DIFFHYST}	Optional hysteresis applied to differential input		30		mV
V _{VDD-VREF}	Required difference between VDD and a selected VREF, VDD >	0.3			V
	VREF				
I _{INT_REF}	Current used by the internal bandgap reference when selected		13		μΑ
	as source for VREF				
t _{INT_REF,START}	Startup time for the internal bandgap reference		50	80	μS
E _{INT_REF}	Internal bandgap reference error	-3		3	%
R _{LADDER}	Reference ladder resistance, ILADDER = VREF / RLADDER		550		kΩ
V _{INPUTOFFSET}	Input offset	-10		10	mV
D _{NLLADDER}	Differential non-linearity of reference ladder		<0.1		LSB
t _{COMP,START}	Startup time for the comparator core		3		μS

Total comparator run current must be calculated from the I_{COMP} , I_{INT_REF} , I_{SOURCE} and I_{LADDER} values for a given reference voltage.



39 LPCOMP — Low power comparator

LPCOMP compares an input voltage against a reference voltage.

Listed here are the main features of LPCOMP:

- 0 VDD input range
- Ultra low power
- Eight input options (AINO to AIN7)
- Reference voltage options:
 - · Two external analog reference inputs, or
 - 15-level internal reference ladder (VDD/16)
- · Optional hysteresis enable on input
- Wakeup source from OFF mode

In System ON, the LPCOMP can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the selected reference. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

Restriction: LPCOMP cannot be used (STARTed) at the same time as COMP. Only one comparator can be used at a time.

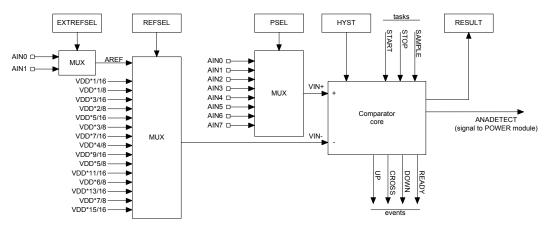


Figure 114: Low power comparator

The wakeup comparator (LPCOMP) compares an input voltage (VIN+), which comes from an analog input pin selected via the PSEL register against a reference voltage (VIN-) selected via the *REFSEL* on page 403 and *EXTREFSEL* registers.

The *PSEL*, *REFSEL*, and *EXTREFSEL* registers must be configured before the LPCOMP is enabled through the *ENABLE* register.

The *HYST* register allows enabling an optional hysteresis in the comparator core. This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 115: Effect of hysteresis on a noisy input signal* on page 399 for illustration of the effect of an active hysteresis on a noisy input signal. It is disabled by default, and shall be configured before enabling LPCOMP as well.

The LPCOMP is started by triggering the START task. After a start-up time of t_{LPCOMP,STARTUP} the LPCOMP will generate a READY event to indicate that the comparator is ready to use and the output of the LPCOMP is correct. The LPCOMP will generate events every time VIN+ crosses VIN-. More specifically, every time VIN+ rises above VIN- (upward crossing) an UP event is generated along with a CROSS event. Every time VIN+ falls below VIN- (downward crossing), a DOWN event is generated along with a CROSS event. When hysteresis is enabled, the upward crossing level becomes (VIN- + VHYST/2), and the downward crossing level becomes (VIN- - VHYST/2).



The LPCOMP is stopped by triggering the STOP task.

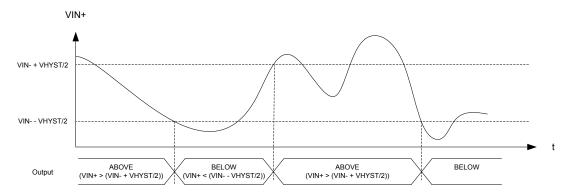


Figure 115: Effect of hysteresis on a noisy input signal

LPCOMP will be operational in both System ON and System OFF mode when it is enabled through the ENABLE register. See *POWER* — *Power supply* on page 76 for more information about power modes. Note that it is not allowed to go to System OFF when a READY event is pending to be generated.

All LPCOMP registers, including *ENABLE*, are classified as retained registers when the LPCOMP is enabled. However, when the device wakes up from System OFF, all LPCOMP registers will be reset.

The LPCOMP can wake up the system from System OFF by asserting the ANADETECT signal. The ANADETECT signal can be derived from any of the event sources that generate the UP, DOWN and CROSS events. In case of wakeup from System OFF, no events will be generated, only the ANADETECT signal. See the ANADETECT register (*ANADETECT* on page 403) for more information on how to configure the ANADETECT signal.

The immediate value of the LPCOMP can be sampled to *RESULT* on page 402 by triggering the SAMPLE task.

See *RESETREAS* on page 83 for more information on how to detect a wakeup from LPCOMP.

39.1 Shared resources

The LPCOMP shares resources with other peripherals.

The LPCOMP shares analog resources with SAADC and COMP. While it is possible to use SAADC at the same time as COMP or LPCOMP, COMP and LPCOMP are mutually exclusive: enabling one will automatically disable the other. In addition, when using SAADC and COMP or LPCOMP simultaneously, it is not possible to select the same analog input pin for both modules.

The LPCOMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has been stopped. Failing to do so may result in unpredictable behaviour.

39.2 Pin configuration

You can use the LPCOMP.PSEL register to select one of the analog input pins, AINO through AINO, as the analog input pin for the LPCOMP.

See *Figure 20: GPIO Port and the GPIO pin details* on page 108 for more information on the pins. Similarly, you can use *EXTREFSEL* on page 403 to select one of the analog reference input pins, AINO and AINI, as input for AREF in case AREF is selected in *EXTREFSEL* on page 403. The selected analog pins will be acquired by the LPCOMP when it is enabled through *ENABLE* on page 402.



39.3 Registers

Table 89: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40013000	LPCOMP	LPCOMP	Low power comparator	

Table 90: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	LPCOMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	Enable LPCOMP
PSEL	0x504	Input pin select
REFSEL	0x508	Reference select
EXTREFSEL	0x50C	External reference select
ANADETECT	0x520	Analog detect configuration
HYST	0x538	Comparator hysteresis enable

39.3.1 SHORTS

Address offset: 0x200

Shortcut register

D.11				24 20 20 20 27 26 25 24	22 22 24 20 40 47 47 47 48 42 42 44 40 0 0 7 6 5 4 2 2 4 0
	number			31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E D C B A
Res	et 0x000000	000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field		Value Id	Value	Description
Α	RW READ	DY_SAMPLE			Shortcut between READY event and SAMPLE task
					See EVENTS_READY and TASKS_SAMPLE
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
В	RW READ	DY_STOP			Shortcut between READY event and STOP task
					See EVENTS_READY and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
С	RW DOW	N_STOP			Shortcut between DOWN event and STOP task
					See EVENTS_DOWN and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
D	RW UP_S	ТОР			Shortcut between UP event and STOP task
					See EVENTS_UP and TASKS_STOP
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
E	RW CROS	SS_STOP			Shortcut between CROSS event and STOP task
					See EVENTS_CROSS and TASKS_STOP
			Disabled	0	Disable shortcut



Bit number		31 30 29 28 27 20	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			E D C B
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
	Enabled	1	Enable shortcut

39.3.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		01 00 23 20 27 20 20 2	D C B A
Reset 0x00000000		0 0 0 0 0 0 0	
ld RW Field	Value Id	Value	Description
A RW READY			Write '1' to Enable interrupt for READY event
			See EVENTS_READY
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW DOWN			Write '1' to Enable interrupt for DOWN event
			See EVENTS_DOWN
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW UP			Write '1' to Enable interrupt for UP event
			See EVENTS_UP
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW CROSS			Write '1' to Enable interrupt for CROSS event
			See EVENTS_CROSS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

39.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		31	30 2	29 2	28 2	27 :	26 2	25 2	24 2	23 2	2 2	1 2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 11	. 10	9	8	7	6	5	4 :	3 2	1	0
Id																														ı) C	В	Α
Rese	et 0x0	0000000		0	0	0	0	0	0 (0	0	0 0) (0 0	0 (0 (0 (0) () () () (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue							Desc	rip	tior	n																		
Α	RW	READY									١	Write	e '1	l' to	Di:	sab	le i	nter	rup	t fo	or F	EA	OY e	vent	t								$\overline{}$
											9	See L	EVE	NT	S_R	EA	DY																
			Clear	1							[Disal	ble																				
			Disabled	0							F	Read	l: D	isak	bled	t																	
			Enabled	1							F	Read	i: E	nab	led																		
В	RW	DOWN									١	Write	e '1	l' to	Di:	sab	le i	nter	rup	t fo	or C	OW	/N e	ven	t								
											9	See	EVE	NT	S_E	ov	VN																
			Clear	1							[Disal	ble																				
			Disabled	0							F	Read	l: D	isat	bled	t																	
			Enabled	1							F	Read	i: E	nab	led																		
С	RW	UP									١	Write	e '1	l' to	Di	sab	le i	nter	rup	t fo	or L	IP e	ven	t									
											9	See L	EVE	NT.	S_L	ΙP																	



Bit number		31	. 30 :	29 2	28 2	7 2	26 2	5 2	24 2	23 2	22 :	21 :	20	19	18 :	17 :	16	15 :	14 1	.3 :	12 1	1 1	0 9	3 (3 7	6	5	4	3 D	2 C	1 B	0 A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0) (0	0	0	0		0		
Id RW Field	Value Id	Va	lue						ı	Des	crip	otio	n																			
	Clear	1							ſ	Disa	ble	è																				
	Disabled	0							F	Rea	d: [Disa	ble	d																		
	Enabled	1							F	Rea	d: E	Ena	ble	d																		
D RW CROSS									١	Wri	te '	1' t	o D	isal	ole i	inte	rru	pt f	or (CRC)SS (eve	nt									
									9	See	EV	EN	s_	CRC	oss																	
	Clear	1							[Disa	ble	9																				
	Disabled	0							ı	Rea	d: [Disa	ble	d																		
	Enabled	1							F	Rea	d: E	Ena	ble	d																		

39.3.4 RESULT

Address offset: 0x400

Compare result

Bit	numbe	er		31 3	30 2	9 2	8 27	7 2	6 25	5 24	23	22	21	20	19	18	17 :	16	15	14	13	12	11 :	10	9 1	8 7	7 6	5	4	3	2	1 0
Id																																Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						De	scr	ipti	on																		
Α	R	RESULT									Re	sult	of	last	cor	npa	re.	De	cisi	on	poi	nt S	AM	PLE	tas	k.						
			Bellow	0							Inp	out	vol	tage	is b	oelo	w t	he	ref	ere	nce	thr	esh	old	(VI	N+ <	< VII	N-).				
			Above	1							Inp	out	vol	tage	is a	bo	ve t	he	ref	ere	nce	thr	esh	old	(VI	N+ >	> VII	N-).				

39.3.5 ENABLE

Address offset: 0x500 Enable LPCOMP

Bit	nun	nbei	•		3	1 3	0 2	9 2	8 2	7 2	26 2	25 2	24	23 :	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																				А А
Res	et (0x00	000000		0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R	w	Field	Value Id	٧	alu	e							Des	cri	otic	on																			
Α	R	W	ENABLE											Ena	ble	or	dis	abl	e L	PCC	MI)														
				Disabled	0									Disa	able	9																				
				Enabled	1									Ena	ble																					

39.3.6 PSEL

Address offset: 0x504

Input pin select

Bit number		31 30 29	28 2	27 2	26 2	5 24	23	22 2	21 20	19	18	17	16	15 1	L4 1	3 12	2 11	10	9	8 7	7 6	5 5	4	3	2	1 0
Id																									Α.	А А
Reset 0x00000000		0 0 0	0	0	0 0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0 () (0	0	0	0	0 0
ld RW Field	Value Id	Value					De	scrip	tion																	
A RW PSEL							Ana	alog	pin s	elec	t															
	AnalogInput0	0					AIN	NO se	lecte	ed a	s an	alo	g in	put												
	AnalogInput1	1					AIN	N1 se	lecte	ed a	s an	alo	g in	put												
	AnalogInput2	2					AIN	N2 se	lecte	ed a	s an	alo	g in	put												
	AnalogInput3	3					AIN	N3 se	lecte	ed a	s an	alo	g in	put												
	AnalogInput4	4					AIN	N4 se	lecte	ed a	s an	alo	g in	put												
	AnalogInput5	5					AIN	N5 se	lecte	ed a	s an	alo	g in	put												
	AnalogInput6	6					AIN	N6 se	lecte	ed a	s an	alo	g in	put												
	AnalogInput7	7					AIN	N7 se	lecte	ed a	s an	alo	g in	put												



39.3.7 REFSEL

Address offset: 0x508 Reference select

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Reset 0x00000004		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW REFSEL			Reference select
	Ref1_8Vdd	0	VDD * 1/8 selected as reference
	Ref2_8Vdd	1	VDD * 2/8 selected as reference
	Ref3_8Vdd	2	VDD * 3/8 selected as reference
	Ref4_8Vdd	3	VDD * 4/8 selected as reference
	Ref5_8Vdd	4	VDD * 5/8 selected as reference
	Ref6_8Vdd	5	VDD * 6/8 selected as reference
	Ref7_8Vdd	6	VDD * 7/8 selected as reference
	ARef	7	External analog reference selected
	Ref1_16Vdd	8	VDD * 1/16 selected as reference
	Ref3_16Vdd	9	VDD * 3/16 selected as reference
	Ref5_16Vdd	10	VDD * 5/16 selected as reference
	Ref7_16Vdd	11	VDD * 7/16 selected as reference
	Ref9_16Vdd	12	VDD * 9/16 selected as reference
	Ref11_16Vdd	13	VDD * 11/16 selected as reference
	Ref13_16Vdd	14	VDD * 13/16 selected as reference
	Ref15_16Vdd	15	VDD * 15/16 selected as reference

39.3.8 EXTREFSEL

Address offset: 0x50C External reference select

Bitı	numbe	er		3	1 30	29	28	3 27	7 26	25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id																																		А	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	٧	'alue	2						De	scri	iptio	on																				
Α	RW	EXTREFSEL										Ext	err	nal a	ınal	og i	refe	rer	ice	sele	ect														
			AnalogReference0	0								Us	e A	IN0	as e	exte	erna	ıl ar	nalc	og r	efe	ren	ce												
			AnalogReference1	1								Us	e A	IN1	as e	exte	erna	ıl ar	nalc	og r	efe	ren	ce												

39.3.9 ANADETECT

Address offset: 0x520

Analog detect configuration

Bitı	numbe	er		31	. 30	29	28 2	27 2	26 2	25 2	24 2	23 2	22 2	1 2	0 19	9 18	3 17	' 16	15	14	13	12 1	.1 10	9	8	7	6	5	4	3 2	1	0
Id																															Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0 (0	0 (0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	llue							Desc	cript	tion	1																	
Α	RW	ANADETECT									A	۱nal	log (dete	ect (con	figu	rati	on													
			Cross	0							(Gen	erat	e A	NAI	DET	ECT	on	cro	ssir	g, b	oth	upw	ard	cro	ssir	g ar	nd				
											C	wob	nwa	ard	cros	ssin	g															
			Up	1							(Gen	erat	e A	NAI	DET	ECT	on	upv	war	d cr	ossi	ng o	nly								
			Down	2							(Gen	erat	e A	NAI	DET	ECT	on	dov	vnv	varo	l cro	ssin	g or	ly							

39.3.10 HYST

Address offset: 0x538

Comparator hysteresis enable



Bit	numb	er		31 30	29	28 2	27 2	6 25	5 24	1 23	3 22	21	20 1	19 1	.8 1	7 16	15	14	13	12	11 1	9	8	7	6	5	4	3	2	1 0
Id																														Α
Res	et 0x	0000000		0 0	0	0 (0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value						De	escri	ptic	on																	
Α	RW	HYST								Co	mp	arat	or h	iyste	eres	is er	nabl	e												
			NoHyst	0						Co	mp	arat	or h	iyste	eres	is di	sab	led												
			Hyst50mV	1						Co	mp	arat	or h	iyste	eres	is di	sab	led	(typ	. 50	mV)								

39.4 Electrical Specification

39.4.1 LPCOMP Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{LPC}	Run current for low power comparator		0.5		μΑ
t _{LPCANADET}	Time from VIN crossing (>=50mV above threshold) to		5		μs
	ANADETECT signal generated.				
E _{REFLADDER}	Error in reference ladder threshold voltage	-30		30	mV
V _{HYST}	Optional hysteresis		30		mV



40 WDT — Watchdog timer

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog timer is started by triggering the START task.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by:

```
timeout [s] = ( CRV + 1 ) / 32768
```

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see chapter *CLOCK* — *Clock control* on page 98.

40.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

40.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping and when it is halted by the debugger. It is however possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

40.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset.

See *Reset* on page 80 for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, the impending watchdog reset will always be effectuated.

The watchdog must be configured before it is started. After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog can be reset from several reset sources, see *Reset behavior* on page 81.

When the device starts running again, after a reset, or waking up from OFF mode, the watchdog configuration registers will be available for configuration again.



40.4 Registers

Table 91: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40010000	WDT	WDT	Watchdog Timer	

Table 92: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the watchdog
EVENTS_TIMEOUT	0x100	Watchdog timeout
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RUNSTATUS	0x400	Run status
REQSTATUS	0x404	Request status
CRV	0x504	Counter reload value
RREN	0x508	Enable register for reload request registers
CONFIG	0x50C	Configuration register
RR[0]	0x600	Reload request 0
RR[1]	0x604	Reload request 1
RR[2]	0x608	Reload request 2
RR[3]	0x60C	Reload request 3
RR[4]	0x610	Reload request 4
RR[5]	0x614	Reload request 5
RR[6]	0x618	Reload request 6
RR[7]	0x61C	Reload request 7

40.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	iumbe	r		31	L 30	29	28	8 27	7 2	26 2	5 2	24 2	23 :	22	21	20	19	18	3 1	.7 :	16	15	14	13	3 1	2 1	1 1	0 9	9 (3 7	' (ŝ !	5	4	3	2	1	0
Id																																						Α
Res	et 0x0	0000000		0	0	0	0	0) (0 (0	0	0	0	0	0	0	0	(0	0	0	0	0	C) () () () () () () (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue								Des	cri	pti	on																						
Α	RW	TIMEOUT										١	۷ri	te	1'1	to E	na	ble	ir	ite	ru	pt	for	TII	ME	ΟU	Te	/en	t									
												9	See	ΕV	ΈN	TS_	ΤI	ME	οι	JT																		
			Set	1								E	Ena	ble	:																							
			Disabled	0								F	Rea	d:	Dis	abl	ed																					
			Enabled	1								F	Rea	d:	Ena	able	d																					

40.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		31	1 30	29	2	8 2	7 2	26 2	5 2	24 2	23	22	21	20	19	18	3 1	7 :	16	15	14	13	12	2 1	1 10) 9	8	7	E	5	4	- 3	2	1	. 0
Id																																					Α
Res	et 0x0	0000000		0	0	0	0	0) (0 (0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (
Id	RW	Field	Value Id	Va	alue							ı	Des	cri	pti	on																					
Α	RW	TIMEOUT										١	۷r	ite	'1'	to [Disa	abl	e i	nte	rru	ıpt	for	TII	ME	ΟU	Тe	ver	t								
												9	See	E١	ÆΝ	ITS_	TI	ME	Ol	JT																	
			Clear	1								[Dis	abl	е																						
			Disabled	0								ı	Rea	ıd:	Dis	abl	ed																				
			Enabled	1								F	Rea	ıd:	Ena	able	ed																				



40.4.3 RUNSTATUS

Address offset: 0x400

Run status

Bit	numbe	er		31 30	29	28	27	26	25 2	24 2	23 2	22 2	21 2	0 1	9 18	3 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	. 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Value	:					ı	Des	crip	tio	n																	
Α	R	RUNSTATUS								ı	Indi	cate	es w	het	her	or r	ot t	the	wat	chd	og is	rur	nin	g							
			NotRunning	0						١	Wat	tcho	gob	not	run	ning	3														
			Running	1						١	Wat	tcho	gob	is ru	ınni	ng															

40.4.4 REQSTATUS

Address offset: 0x404

Request status

																												_				
	numbe	er		31	1 30	29	28	27	26	25	24	23	3 22 :	21 2	0 19	18	3 17	16	15	14 1	3 12	2 11	. 10	9			6	5	4 3	3 2	1	0
Id																													E [
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	_	0	_	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	1
Id	RW	Field	Value Id	Va	alue	!						De	escrip	otio	n																	
Α	R	RR0										Re	ques	st st	atus	for	RR[0] r	egis	ter												
			DisabledOrRequested	0								RR	R[0] r	egis	ter is	s no	t er	abl	ed,	or a	re al	rea	dy r	equ	esti	ng r	elo	ad				
			${\sf EnabledAndUnrequested}$	1								RR	R[0] r	egis	ter is	s er	able	ed, a	and	are	not	yet	requ	uest	ing	relo	oad					
В	R	RR1										Re	ques	st st	atus	for	RR[1] r	egis	ter												
			DisabledOrRequested	0								RR	R[1] r	egis	ter is	s no	t er	abl	ed,	or a	re al	rea	dy r	equ	esti	ng r	elo	ad				
			${\sf EnabledAndUnrequested}$	1								RR	R[1] r	egis	ter is	s er	able	ed, i	and	are	not	yet	requ	uest	ing	relo	oad					
С	R	RR2										Re	ques	st st	atus	for	RR[2] r	egis	ter												
			DisabledOrRequested	0								RR	R[2] r	egis	ter is	s no	t er	abl	ed,	or a	re al	rea	dy r	equ	esti	ng r	elo	ad				
			EnabledAndUnrequested	1								RR	R[2] r	egis	ter is	s er	able	ed, i	and	are	not	yet	requ	uest	ting	relo	oad					
D	R	RR3										Re	ques	st st	atus	for	RR[3] r	egis	ter												
			DisabledOrRequested	0								RR	R[3] r	egis	ter is	s no	t er	abl	ed,	or a	re al	rea	dy r	equ	esti	ng r	elo	ad				
			EnabledAndUnrequested	1								RR	R[3] r	egis	ter is	s er	able	ed, i	and	are	not	yet	requ	uest	ting	relo	oad					
E	R	RR4										Re	ques	st st	atus	for	RR[4] r	egis	ter												
			DisabledOrRequested	0								RR	R[4] r	egis	ter is	s no	t er	abl	ed,	or a	re al	rea	dy r	equ	esti	ng r	elo	ad				
			EnabledAndUnrequested	1								RR	R[4] r	egis	ter is	s er	able	ed, i	and	are	not	yet	requ	uest	ing	relo	oad					
F	R	RR5										Re	ques	st st	atus	for	RR[5] r	egis	ter												
			DisabledOrRequested	0								RR	R[5] r	egis	ter is	s no	t er	abl	ed,	or a	re al	rea	dy r	equ	esti	ng r	elo	ad				
			EnabledAndUnrequested	1								RR	R[5] r	egis	ter is	s er	able	ed, i	and	are	not	yet	requ	uest	ing	relo	oad					
G	R	RR6										Re	ques	st st	atus	for	RR[6] r	egis	ter												
			DisabledOrRequested	0								RR	R[6] r	egis	ter is	s no	t er	abl	ed,	or a	re al	rea	dy r	equ	esti	ng r	elo	ad				
			EnabledAndUnrequested	1								RR	R[6] r	egis	ter is	s er	able	ed, a	and	are	not	yet	requ	uest	ing	relo	oad					
Н	R	RR7										Re	ques	st st	atus	for	RR[7] r	egis	ter												
			DisabledOrRequested	0								RR	R[7] r	egis	ter is	s no	t er	abl	ed,	or a	re al	rea	dy r	equ	esti	ng r	elo	ad				
			EnabledAndUnrequested	1								RR	R[7] r	egis	ter is	s er	able	ed, i	and	are	not	yet	requ	uest	ing	relo	oad					

40.4.5 CRV

Address offset: 0x504 Counter reload value

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CRV		[0x0000000F0xFFFFFFF Counter reload value in number of cycles of the 32.768 kHz

clock



40.4.6 RREN

Address offset: 0x508

Enable register for reload request registers

Bit r	numbe	er		31	30	29	28 2	27 2	26 2	5 2	4 23	3 22	2 21	1 20) 19	18	17	16	15	14	13 1	12 1	1 10	9	8	7	6	5	4 3	3 2	1	C
Id																										Н	G	F	Ε [
	et 0x0	0000001		0	0	0	0 (0	0 (0 (0 0	0 0	0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0				0 (
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion																		
Α	RW	RRO									Er	nab	le o	r di	sab	le F	RR[O] re	gist	er												
			Disabled	0							Di	isak	ble f	RR[()] re	egis	ter															
			Enabled	1							Er	nab	le R	RR[O] re	gist	er															
В	RW	RR1									Er	nab	le o	r di	sab	le F	RR[1] re	gist	er												
			Disabled	0							Di	isat	ble f	RR[:	1] re	egis	ter															
			Enabled	1							Er	nab	le R	RR[1] re	gist	er															
С	RW	RR2									Er	nab	le o	r di	sab	le F	RR[2] re	gist	er												
			Disabled	0							Di	isak	ole I	RR[2	2] re	egis	ter															
			Enabled	1							Er	nab	le R	RR[2] re	gist	er															
D	RW	RR3									Er	nab	le o	r di	sab	le F	RR[3] re	gist	er												
			Disabled	0							Di	isak	ble f	RR[3] re	egis	ter															
			Enabled	1							Er	nab	le R	RR[3] re	gist	er															
Ε	RW	RR4									Er	nab	le o	r di	sab	le F	RR[4] re	gist	er												
			Disabled	0							Di	isak	ble f	RR[4	4] re	egis	ter															
			Enabled	1							Er	nab	le R	RR[4] re	gist	er															
F	RW	RR5									Er	nab	le o	r di	sab	le F	RR[5] re	gist	er												
			Disabled	0							Di	isat	ble I	RR[5] re	egis	ter															
			Enabled	1							Er	nab	le R	RR[5] re	gist	er															
G	RW	RR6									Er	nab	le o	r di	sab	le F	RR[6] re	gist	er												
			Disabled	0							Di	isak	ole I	RR[5] re	egis	ter															
			Enabled	1							Er	nab	le R	RR[6] re	gist	er															
Н	RW	RR7									Er	nab	le o	r di	sab	le F	RR[7] re	gist	er												
			Disabled	0									ble I	-	-	-																
			Enabled	1							Er	nab	le R	RR[7] re	gist	er															

40.4.7 CONFIG

Address offset: 0x50C Configuration register

Bit number		31	30 2	29 2	28 2	7 2	26 2	25 2	24 2	23 2	22	21 :	20	19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4 3	3 2	1	0
Id																												(2		Α
Reset 0x00000001		0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	1
ld RW Field	Value Id	Va	lue							Des	cri	otio	n																		
A RW SLEEP									(Con	nfig	ure	the	e wa	atcl	ndo	g to	eit	her	be	pau	sed,	or	kep	ru	nnir	ng,				
									١	whi	ile t	he	CPL	J is	sle	epi	ng														
	Pause	0							F	Pau	ıse	wat	cho	gob	wł	ile	the	СР	U is	slee	pin	g									
	Run	1							ŀ	(ee	p t	he v	vat	cho	log	rur	nir	g w	hile	the	CP	U is	slee	pin	g						
C RW HALT									(Con	nfig	ure	the	e wa	atcl	ndo	g to	eit	her	be	pau	sed,	or	kep	ru	nnir	ng,				
									١	whi	ile t	he	CPL	J is	ha	tec	by	the	de	oug	ger										
	Pause	0							F	Pau	ıse	wat	cho	gob	wł	ile	the	СР	U is	halt	ed	by tl	ne d	lebu	ıgge	er					
	Run	1							ŀ	(ee	p t	he v	vat	cho	log	rur	nir	g w	hile	the	CP	U is	halt	ed	by t	he					
									C	deb	oug	ger																			

40.4.8 RR[0]

Address offset: 0x600 Reload request 0



E	Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14 :	13 :	L2 1	11 1	9	8	7	6	5	4	3	2	1	0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α
1	Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0
ı	ld	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
,	Д	W	RR										Re	load	l re	que	st r	egi	ster																
				Reload	0x	6E5	246	35					Va	lue	to r	eau	ıest	ar	elo	ad d	of tl	ne v	vat	chd	og t	me	r								

40.4.9 RR[1]

Address offset: 0x604 Reload request 1

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0)
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	4
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0)
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																				ı
Α	W	RR										Re	loa	d re	que	est i	egi	iste	r																
			Reload	0x	6E5	246	35					Va	lue	to	ea	uesi	aı	relo	ad	of t	he	wa	tch	dog	tim	ner									

40.4.10 RR[2]

Address offset: 0x608 Reload request 2

Bit r	num	nbe	r		31	. 30	29	28	3 27	7 26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	А	A	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4 А
Res	et O)x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R۱	w	Field	Value Id	Va	lue							De	escr	ipti	on																			
Α	W	/	RR										Re	loa	d re	que	est r	egi	ster																
				Reload	0х	6E5	24	535	,				Va	lue	to	req	uest	ar	elo	ad o	of t	he	wat	cho	log	tim	er								

40.4.11 RR[3]

Address offset: 0x60C Reload request 3

Bitı	num	nbe	r		31	. 30	29	2	8 2	7 2	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 :	L 0
Id					Α	Α	Α	A	۱ ۸	Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A
Res	et 0	0x0	0000000		0	0	0	C) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (
Id	R	w	Field	Value Id	Va	alue	•							De	scri	ptic	n																			
Α	W	V	RR											Rel	oad	l red	que	st r	egi	stei	r															
				Reload	0х	6E5	524	63	5					Val	ue 1	to r	equ	est	ar	elo	ad	of t	he	wa	tch	dog	tim	ner								

40.4.12 RR[4]

Address offset: 0x610 Reload request 4

Bitı	nur	mbe	r		31	L 30	29	28	8 2	7 2	6 2	5 2	24 2	23 :	22 :	21 2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 9	9 ;	3 7	΄ 6	5	4	3	2	1	0
Id					Α	Α	Α	Α	. Δ		Δ Α	۱ ۸	A .	Α	Α	Α.	Δ ,	Α ,	Α ,	Δ Α	۱ ۸	Α Α	Δ Α	۸ ۸	۱ ۸	Α Α	۱ ۸	Α,	Δ Δ	. 4	A	A	Α	Α	Α	Α
Res	et (0x0	0000000		0	0	0	0	0) (0 () (0	0	0	0	0 (0 (0 (0 () () () () () (0) () (0	0	0	0	0	0	0	0
Id	R	RW	Field	Value Id	Va	alue								Des	crip	otio	n																			
Α	٧	N	RR										F	Relo	oad	req	ues	st re	egis	ter																_
				Reload	0x	6E5	246	635	5				١	/alı	ue t	o re	que	est	a re	loa	d o	f th	e w	ato	hdo	og t	ime	er								

40.4.13 RR[5]

Address offset: 0x614 Reload request 5



Bitı	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20 1	19 1	18 1	L7 1	16 1	L5 1	L4 1	13 1	12 1	.1 1	0 9	9 8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Α.	Α.	Α.	Α	A	Α.	4 Α	\ A	\ A	A	Α	Α	Α	Α	Α	A A	
Res	et Ox(00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0 0	,
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			ı
Α	W	RR										Rel	oad	l red	que	st re	egis	ter																
			Reload	0x	6E5	246	35					Val	ue 1	to r	equ	est	a re	eloa	ad o	of th	ne v	vato	hd	og t	ime	r								

40.4.14 RR[6]

Address offset: 0x618 Reload request 6

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	W	RR										Rel	oad	l re	que	st r	egis	stei	r															
			Reload	0x	6E5	246	35					Val	ue 1	to r	equ	ıest	ar	elo	ad (of t	he v	wat	cho	log	tim	ner								

40.4.15 RR[7]

Address offset: 0x61C Reload request 7

Bitı	num	nbe	r		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20 :	19 :	18 1	.7 1	6 1	5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	Α	. A	Α	Α	Α	Α	Α	Α	Α	A	Α,	4 Α	A /	\ <i>A</i>	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4 А
Res	et 0)x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R۱	w	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	W	/	RR										Re	oad	l re	que	st r	egis	ter															
				Reload	0х	6E5	246	635	,				Va	lue 1	to r	equ	est	a re	eloa	d o	f th	e w	atcl	ndo	g tin	ner								

40.5 Electrical Specification

40.5.1 Watchdog Timer Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{WDT}	Run current for watchdog timer		0.3	2	μΑ
t _{WDT}	Time out interval	458 μs		36 h	



41 SWI — Software interrupts

A set of interrupts have been reserved for use as software interrupts.

41.1 Registers

Table 93: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40014000	SWI	SWI0	Software interrupt 0		
0x40015000	SWI	SWI1	Software interrupt 1		
0x40016000	SWI	SWI2	Software interrupt 2		
0x40017000	SWI	SWI3	Software interrupt 3		
0x40018000	SWI	SWI4	Software interrupt 4		
0x40019000	SWI	SWI5	Software interrupt 5		



42 NFCT — Near field communication tag

The NFCT peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum.

With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

- · NFC-A listen mode operation
 - · 13.56 MHz input frequency
 - Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- · Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- · Programmable frame timing controller
- · Integrated automatic collision resolution, CRC and parity functions

42.1 Overview

The NFC peripheral is an implementation of an NFC Forum compliant listening device NFC-A.

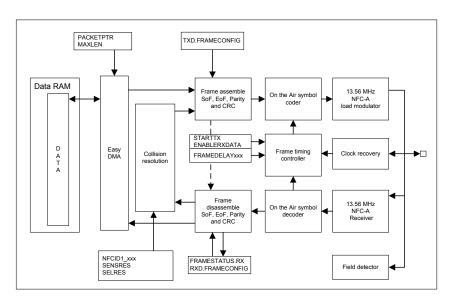


Figure 116: NFC block diagram

The NFC peripheral contains a 13.56 MHz AM receiver and a 13.56 MHz load modulator compatible with the NFC-A technology defined in the NFC Forum with 106 kbps data rate.

The received frames will be automatically disassembled and the data part of the frame transferred to RAM. When transmitting, the frame data will be transferred directly from RAM and transmitted with configurable frame type and delay timing. The system will be notified by an event whenever a complete frame is received or sent.

It also supports the collision detection and resolution ("anticollision") as defined by the NFC Forum.

Wake-on-field is supported in SENSE mode while the device is either in System OFF or System ON mode. When the antenna enters an NFC field, an event will be triggered notifying the system to activate the NFC functionality for incoming frames. In System ON, if the energy detected at the antenna increases beyond a threshold value, the module will generate a FIELDDETECTED event. The module will generate a



FIELDLOST event when the quality or strength of the field no longer support NFC communication. Please refer to *NFCT Electrical Specification* on page 431 for the Low Power Field Detect threshold values.

In system OFF, the NFC Low Power Field Detect function can wake the system up through a reset. The NFC bit in register *RESETREAS* on page 83 will be set as cause of the wake-up.

If the system is put into system OFF mode while a field is already present, the NFC Low Power Field Detect function will wake the system up right away and generate a reset.

Note that as a consequence of reset, NFC is disabled, so the reset handler will have to activate NFC again and set it up properly.

The HFXO must be running before the NFC peripheral goes into ACTIVATED state. Note that the NFC peripheral calibration is automatically done on ACTIVATE task. The HFXO can be turned off when the NFC peripheral goes into SENSE mode. The shortcut FIELDDETECTED_ACTIVATE can be used when the HFXO is already running while in SENSE mode.

Outgoing data will be collected from RAM with the EasyDMA function and assembled according to the TXD.FRAMECONFIG register. Incoming data will be disassembled according to the RXD.FRAMECONFIG register and the data section in the frame will be written to RAM via the EasyDMA function.

The NFC peripheral includes a frame timing controller that can be used to accurately control the inter-frame delay between the incoming frame and a corresponding outgoing frame. It also includes optional CRC functionality.

The NFC peripheral has a set of different states. The module can change state by triggering a task, or when specific operations are finalized. Events and tasks allow software to keep track of and change the current state.

See Figure 116: NFC block diagram on page 412 and Figure 117: NFC state diagram on page 413 for more information.

Notes:

- FIELDLOST event will not be reflected in the state machine (for instance by going back to the DISABLE state), it is up to software to decide on the actions to take when a field lost occurs.
- FIELDLOST event is not generated in SENSE mode.
- FIELDDETECTED event is generated only on the transition from FIELDLOST event to energy detected by the NFC peripheral. So, sending SENSE task while field is still present does not generate FIELDDETECTED event.
- If the FIELDDETECTED event is cleared before sending the ACTIVATE task, then the FIELDDETECTED event shows up again after sending the ACTIVATE task. The shortcut FIELDDETECTED_ACTIVATE can be used to avoid this condition.

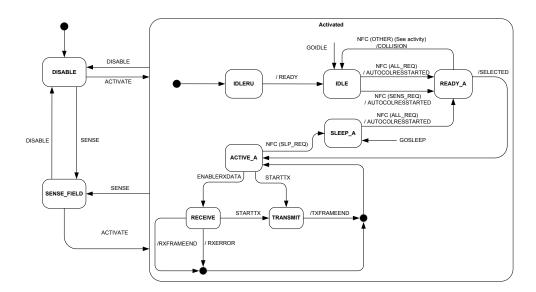


Figure 117: NFC state diagram



42.2 Pin configuration

NFC uses two pins to connect the antenna.

These pins are shared with GPIOs, and the PROTECT field in the NFCPINS register in *UICR* defines the usage of these pins and their protection level against excessive voltages. The content of the NFCPINS register is reloaded at every reset.

When NFCPINS.PROTECT=NFC, a protection circuit will be enabled on the dedicated pins, preventing the chip from being damaged in the presence of a strong NFC field. The GPIO function will be disabled on those pins as well.

When NFCPINS.PROTECT=Disabled, the device will not be protected against strong NFC field damages caught by a connected NFC antenna, and the NFCT peripheral will not operate as expected, as it will never leave the DISABLE state.

The pins dedicated to the NFC antenna function will have some limitation when the pins are configured for normal GPIO operation. The pin capacitance will be higher on those (refer to C_{PAD_NFC} in the *GPIO Electrical Specification* on page 151 below), and some increased leakage current between the two pins is to be expected if they are used in GPIO mode, and are driven to different logical values. To save power the two pins should always be set to the same logical value whenever entering one of the device power saving modes. Please refer to I_{NFC_LEAK} in *GPIO Electrical Specification* on page 151 for details.

42.3 EasyDMA

The NFC peripheral implements EasyDMA for reading and writing of data packets from and to the Data RAM without CPU involvement.

The NFC EasyDMA utilizes one pointer called PACKETPTR for receiving and transmitting packets.

The EasyDMA can either read or write between the NFC peripheral and the RAM, but not at the same time. The event RXFRAMESTART indicates that the EasyDMA has started writing to the RAM for a receive frame and the event RXFRAMEND indicates that the EasyDMA has completed writing to the RAM. Similarly, the event TXFRAMESTART indicates that the EasyDMA has started reading from the RAM for a transmit frame and the event TXFRAMEND indicates that the EasyDMA has completed reading from the RAM. If a transmit and a receive operation is issued at the same time, the transmit operation would be prioritized.

Starting a transmit operation while the EasyDMA has already started writing a receive frame to the RAM will result in unpredictable behavior. Starting an EasyDMA operation whilst there is an ongoing EasyDMA operation may result in unpredictable behavior. It is recommended to wait for the TXFRAMEEND or RXFRAMEND event for the respective ongoing transmit or receive before starting a new receive or transmit operation.

The MAXLEN register determines the maximum number of bytes that can be read from or written to the RAM. This feature can be used to secure that the NFC peripheral does not overwrite, or read beyond, the RAM assigned to a packet. Note that if the RXD.AMOUNT or TXD.AMOUNT register indicates longer data packets than set in MAXLEN, the frames sent to or received from the physical layer will be incomplete. In RX, the OVERRUN bit in the FRAMESTATUS.RX register will be set and an RXERROR event will be triggered in that situation.

Note that RXD.AMOUNT and TXD.AMOUNT define a frame length in bytes and bits excluding SoF, EoF and parity, but including CRC for RXD.AMOUNT only, make sure to take potential additional bits into account when setting MAXLEN.

Only sending task ENABLERXDATA ensures that a new value in PACKETPTR pointing to the RX buffer in Data RAM is taken into account.

If PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See Chapter *Memory* on page 20 for more information about the different memory regions.

The NFC peripherals normally do alternative receive and transmit frames. So, to prepare for the next frame, the PACKETPTR, MAXLEN, TXD.FRAMECONFIG and TXD.AMOUNT can be updated while the receive is in progress, and, similarly, the PACKETPTR, MAXLEN and RXD.FRAMECONFIG can be updated while



the transmit is in progress. They can be updated and prepared for the next NFC frame immediately after the STARTED event of the current frame has been received. Updating the TXD.FRAMECONFIG and TXD.AMOUNT during the current transmit frame or updating RXD.FRAMECONFIG during current receive frame may cause unpredictable behaviour.

In accordance with *NFC Forum, NFC Digital Protocol Technical Specification*, the least a significant bit from the least significant byte is sent on air first. The bytes are stored in increasing order, starting at the lowest address in the EasyDMA buffer in RAM.

42.4 Collision resolution

The NFC peripheral implements an automatic collision resolution function as defined by the NFC Forum.

The SENSRES and SELRES registers need to be programmed upfront in order for the collision resolution to behave correctly. Depending on the NFCIDSIZE field in SENSRES, the following registers also need to be programmed upfront:

- NFCID1 LAST if NFCID1SIZE=NFCID1Single (ID = 4 bytes);
- NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Double (ID = 7 bytes);
- NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Triple (ID = 10 bytes);

Table 94: NFCID1 byte allocation (top sent first on air) on page 415 explains the position of the ID bytes in NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST, depending on the ID size, and as compared to the definition used in the NFC Forum, NFC Digital Protocol Technical Specification.

Table 94: NFCID1 byte allocation (top sent first on air)

	ID = 4 bytes	ID = 7 bytes	ID = 10 bytes
NFCID1_Q			nfcid1 ₀
NFCID1_R			nfcid1 ₁
NFCID1_S			nfcid1 ₂
NFCID1_T		nfcid1 ₀	nfcid1 ₃
NFCID1_U		nfcid1 ₁	nfcid1 ₄
NFCID1_V		nfcid1 ₂	nfcid1 ₅
NFCID1_W	nfcid1 ₀	nfcid1 ₃	nfcid1 ₆
NFCID1_X	nfcid1 ₁	nfcid1 ₄	nfcid1 ₇
NFCID1_Y	nfcid1 ₂	nfcid1 ₅	nfcid1 ₈
NFCID1 Z	nfcid1 ₃	nfcid1 ₆	nfcid1 ₉

Automatic collision resolution is enabled by default.

The hardware implementation can handle the states from IDLE to ACTIVE_A automatically as defined in the *NFC Forum, NFC Activity Technical Specification*, and the other states are to be handled by software. The software keeps track of the state through events. The collision resolution will trigger an AUTOCOLRESSTARTED event when it has started. Reaching the ACTIVE_A state is indicated by the SELECTED event.

If collision resolution fails, a COLLISION event is triggered. Note that errors occurring during automatic collision resolution may also cause ERROR and/or RXERROR events to be generated. Also, other events may get generated. It is recommended that the software ignores any event except COLLISION, SELECTED and FIELDLOST during automatic collision resolution. Software shall also make sure that any unwanted SHORT or PPI shortcut are disabled during automatic collision resolution.

A pre-defined set of registers, NFC.TAGHEADER0..3, containing a valid NFCID1 value, is available in *FICR*, and can be used by software to populate the NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST registers. Refer to the release notes of the NFC stack for more details on the format.

The automatic collision resolution will be restarted, if the packets are received with CRC or parity errors while in ACTIVE A state.

The SLP_REQ is automatically handled by the NFC peripheral. However, this results in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) since the SLP_REQ has no response. This error must be ignored until the SELECTED event is triggered and this error should be cleared by the software when the SELECTED event is triggered.



42.5 Frame timing controller

The NFC peripheral includes a frame timing controller that continuously keeps track of the number of the 13.56 MHz RF-carrier clock periods since the end of the EoF of the last received frame.

The NFC peripheral can be programmed to send a responding frame within a time window or at an exact count of RF carrier periods. In case of FRAMEDELAYMODE = Window a STARTTX task triggered before the frame timing controller counter is equal to FRAMEDELAYMIN will force the transmission to halt until the counter is equal to FRAMEDELAYMIN. If the counter is within FRAMEDELAYMIN and FRAMEDELAYMAX when the STARTTX task is triggered, the peripheral will start the transmission straight away. In case of FRAMEDELAYMODE = ExactVal, a STARTTX task, triggered before the frame delay counter is equal to FRAMEDELAYMAX, will halt the actual transmission start until the counter is equal to FRAMEDELAYMAX.

In case of FRAMEDELAYMODE = WindowGrid, the behaviour is similar to the FRAMEDELAYMODE = Window, but the actual transmission between FRAMEDELAYMIN and FRAMEDELAYMAX starts on a bit grid as defined for NFC-A Listen frames (slot duration of 128 RF carrier periods).

The FRAMEDELAYMIN and FRAMEDELAYMAX values shall only be updated before the STARTTX task is triggered. Failing to do so may cause unpredictable behaviour. An ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) will be asserted if the frame timing controller counter reaches FRAMEDELAYMAX without any STARTTX task triggered. This may happen even when the response is not required as per *NFC Forum*, *NFC Digital Protocol Technical Specification*. Any commands handled by the automatic collision resolution that don't involve a response being generated may also result in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS).

The frame timing controller operation is illustrated in *Figure 118: Frame timing controller* (*FRAMEDELAYMODE=Window*) on page 416. The frame timing controller automatically adjusts the frame timing counter based on the last received data bit according to NFC-A technology in the *NFC Forum, NFC Digital Protocol Technical Specification*.

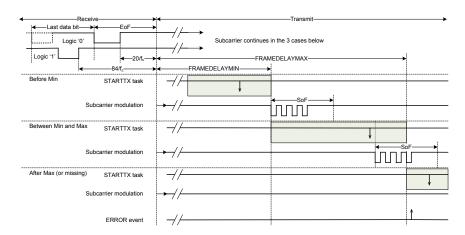


Figure 118: Frame timing controller (FRAMEDELAYMODE=Window)

42.6 Frame assembler

The NFC peripheral implements a frame assembler in hardware.

When the NFC peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For RX, see *Frame disassembler* on page 417. For TX, the software must indicate the address of the source buffer in Data RAM and its size through programming the PACKETPTR and MAXCNT registers respectively, then issuing a TXSTART task.

MAXCNT must be set so that it matches the size of the frame to be sent.

The STARTED event indicates that the PACKETPTR and MAXCNT registers have been captured by the frame assembler's EasyDMA.



When asserting the STARTTX task, the frame assembler module will start reading TXD.AMOUNT.TXDATABYTES bytes (plus one additional byte if TXD.AMOUNT.TXDATABITS > 0) from the RAM position set by the PACKETPTR.

The NFC peripheral transmits the data as read from RAM, adding framing and the CRC calculated on the fly. The NFC peripheral will take (8*TXD.AMOUNT.TXDATABYTES + TXD.AMOUNT.TXDATABITS) bits and assemble a frame according to settings in TXD.FRAMECONFIG. Both short frames, standard frames and bit oriented SDD frames as specified in the NFC Forum, NFC Digital Protocol Technical Specification can be assembled by correct setting of the TXD.FRAMECONFIG register.

The bytes will be transmitted on air in the same order as they are read from RAM with a rising bit order within each byte (least significant bit first). That is, b0 will be transmitted on air before b1, and so on. The bits read from RAM will be coded into symbols as defined in the NFC Forum, NFC Digital Protocol Technical Specification.

Important: Some NFC Forum documents, such as *NFC Forum, NFC Digital Protocol Technical Specification*, define bit numbering in a byte from b1 (LSB) to b8 (MSB), while most other technical documents from the NFC Forum, and also the Nordic Semiconductor documentation, traditionally numbers them from b0 to b7. The present document uses the b0 to b7 numbering scheme. Be aware of this when comparing with the *NFC Forum, NFC Digital Protocol Technical Specification* to others.

The frame assembler can be configured in TXD.FRAMECONFIG to add Start of Frame (SoF) symbol, calculate and add parity bits, and calculate and add CRC to the data read from RAM when assembling the frame. The total frame will then be longer than what is defined by TXD.AMOUNT.TXDATABYTES and TXDATABITS. DISCARDMODE will select if the first bits in the first byte read from RAM or the last bits in the last byte read from RAM will be discarded if TXD.AMOUNT.TXDATABITS are not equal to zero. Note that if TXD.FRAMECONFIG.PARITY = Parity and TXD.FRAMECONFIG.DISCARDMODE=DiscardStart, a parity bit will be included after the non-complete first byte. No parity will be added after a non-complete last byte.

The Frame Assemble operation is illustrated in *Figure 119: Frame assemble* on page 417 for different settings in TXD.FRAMECONFIG. All shaded bits fields are added by the frame assembler. Some of these bits are optional and appearances are configured in TXD.FRAMECONFIG. Please note that the frames illustrated do not necessarily comply with the NFC specification. The figure is only to illustrate the behavior of the NFC peripheral.

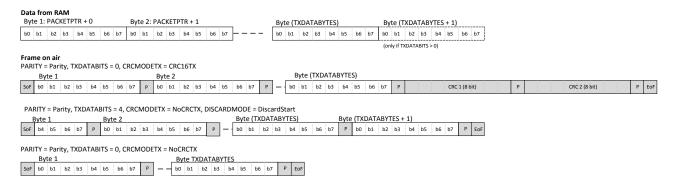


Figure 119: Frame assemble

The accurate timing for transmitting the frame on air is set using the frame timing controller settings.

42.7 Frame disassembler

The NFC peripheral implements a frame disassembler in hardware.

When the NFC peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For TX, see *Frame assembler* on page 416. For RX, the software must indicate the address of the destination buffer in Data RAM and its size through programming the PACKETPTR and MAXCNT registers respectively, then issuing a ENABLERXDATA task.



The STARTED event indicates that the PACKETPTR and MAXCNT registers have been captured by the frame disassembler's EasyDMA.

When an incoming frame starts, the RXFRAMESTART event will get issued and data will be written to the buffer in Data RAM. The frame disassembler will verify and remove on the fly any parity bits and SoF and End of Frame (EoF) symbols based on RXD.FRAMECONFIG register configuration. It will, however, verify and transfer the CRC bytes into RAM, if the CRC is was enabled through RXD.FRAMECONFIG.

When an EoF symbol is detected, the NFC peripheral will assert the RXFRAMEEND event and write the RXD.AMOUNT register to indicate numbers of received bytes and bits in the data packet. The module does not interpret the content of the data received from the remote NFC device, except for SoF, EoF, parity and CRC checking, as described above. The Frame disassemble operation is illustrated in *Figure 120: Frame disassemble illustration* on page 418.

Per NFC specification, the time between end of frame to the next start of frame can be as short as 86 μ s, so care must be taken that PACKETPTR and MAXCNT are ready and ENABLERXDATA is issued on time after the end of previous frame. The use of a PPI shortcut from TXFRAMEEND to ENABLERXDATA is recommended.

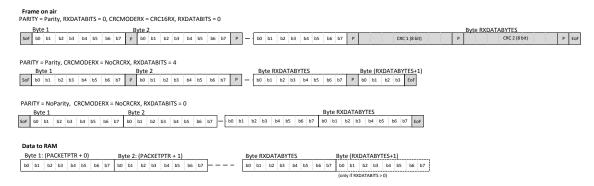


Figure 120: Frame disassemble illustration

42.8 Antenna interface

In ACTIVATED state, an amplitude regulator will adjust the voltage swing on the antenna pins to a value that is within the V_{swing} limit.

Refer to NFCT Electrical Specification on page 431.

42.9 NFCT antenna recommendations

The NFCT antenna coil must be connected differential between NFC1 and NFC2 pins of the device.

Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz.



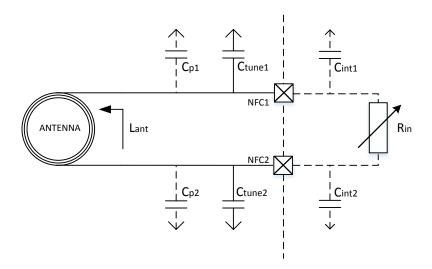


Figure 121: NFCT antenna recommendations

The required tuning capacitor value is given by the below equations:

$$C'_{tune} = \frac{1}{(2\pi \cdot 13.56 \, MHz)^2 \cdot L_{ant}} \quad where \ C'_{tune} = \frac{1}{2} \cdot \left(C_p + C_{int} + C_{tune}\right)$$

$$and \ C_{tune1} = C_{tune2} = C_{tune} \qquad C_{p1} = C_{p2} = C_p \qquad C_{int1} = C_{int2} = C_{int1}$$

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56 \, MHz)^2 \cdot L_{ant}} - C_p - C_{int1}$$

An antenna inductance of $L_{ant} = 2 \mu H$ will give tuning capacitors in the range of 130 pF on each pin. For good performance, match the total capacitance on NFC1 and NFC2.

42.10 Battery protection

If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures.

If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.

42.11 References

NFC Forum, NFC Analog Specification version 1.0, www.nfc-forum.org

NFC Forum, NFC Digital Protocol Technical Specification version 1.1, www.nfc-forum.org

NFC Forum, NFC Activity Technical Specification version 1.1, www.nfc-forum.org



42.12 Registers

Table 95: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40005000	NFCT	NFCT	Near Field Communication Tag		

Table 96: Register Overview

Register	Offset	Description
TASKS_ACTIVATE	0x000	Activate NFC peripheral for incoming and outgoing frames, change state to activated
TASKS_DISABLE	0x004	Disable NFC peripheral
TASKS_SENSE	0x008	Enable NFC sense field mode, change state to sense mode
TASKS STARTTX	0x00C	Start transmission of a outgoing frame, change state to transmit
TASKS_ENABLERXDATA		Initializes the EasyDMA for receive.
TASKS_GOIDLE	0x024	Force state machine to IDLE state
TASKS_GOSLEEP	0x028	Force state machine to SLEEP_A state
EVENTS_READY	0x100	The NFC peripheral is ready to receive and send frames
EVENTS_FIELDDETECTED		Remote NFC field detected
EVENTS_FIELDLOST	0x108	Remote NFC field lost
EVENTS_TXFRAMESTART	T 0x10C	Marks the start of the first symbol of a transmitted frame
EVENTS_TXFRAMEEND		Marks the end of the last transmitted on-air symbol of a frame
EVENTS_RXFRAMESTART		Marks the end of the first symbol of a received frame
EVENTS_RXFRAMEEND	0x118	Received data have been checked (CRC, parity) and transferred to RAM, and EasyDMA has ended
		accessing the RX buffer
EVENTS_ERROR	0x11C	NFC error reported. The ERRORSTATUS register contains details on the source of the error.
EVENTS_RXERROR	0x128	NFC RX frame error reported. The FRAMESTATUS.RX register contains details on the source of the
		error.
EVENTS_ENDRX	0x12C	RX buffer (as defined by PACKETPTR and MAXLEN) in Data RAM full.
EVENTS_ENDTX	0x130	Transmission of data in RAM has ended, and EasyDMA has ended accessing the TX buffer
EVENTS_AUTOCOLRESST	0x138	Auto collision resolution process has started
EVENTS_COLLISION	0x148	NFC Auto collision resolution error reported.
EVENTS_SELECTED	0x14C	NFC Auto collision resolution successfully completed
EVENTS_STARTED	0x150	EasyDMA is ready to receive or send frames.
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSTATUS	0x404	NFC Error Status register
FRAMESTATUS.RX	0x40C	Result of last incoming frames
CURRENTLOADCTRL	0x430	Current value driven to the NFC Load Control
FIELDPRESENT	0x43C	Indicates the presence or not of a valid field
FRAMEDELAYMIN	0x504	Minimum frame delay
FRAMEDELAYMAX	0x508	Maximum frame delay
FRAMEDELAYMODE	0x50C	Configuration register for the Frame Delay Timer
PACKETPTR	0x510	Packet pointer for TXD and RXD data storage in Data RAM
MAXLEN	0x514	Size of allocated for TXD and RXD data storage buffer in Data RAM
TXD.FRAMECONFIG	0x518	Configuration of outgoing frames
TXD.AMOUNT	0x51C	Size of outgoing frame
RXD.FRAMECONFIG	0x520	Configuration of incoming frames
RXD.AMOUNT	0x524	Size of last incoming frame
NFCID1_LAST	0x590	Last NFCID1 part (4, 7 or 10 bytes ID)
NFCID1_2ND_LAST	0x594	Second last NFCID1 part (7 or 10 bytes ID)
NFCID1_3RD_LAST	0x598	Third last NFCID1 part (10 bytes ID)
SENSRES	0x5A0	NFC-A SENS_RES auto-response settings
SELRES	0x5A4	NFC-A SEL_RES auto-response settings



42.12.1 SHORTS

Address offset: 0x200 Shortcut register

	numbe	er		31	. 30	29	28	27	26 2	25 24	4 23	22	21	20 1	19 1	L8 1	L7 1	6 1	5 1	1 13	12	11	10	9	8	7 (5 5	5 4	3	2	1	0
ld Res	at NvN	000000		0	0	٥	0	0	0	0 0		0	0	٥	^	0	n 1	, ,	٠ ،	0	0	0	0	n	0 (0 (٥	٥	В	A
Id		Field	Value Id	_	alue	Ŭ	Ŭ	Ů			_	escri	_	•	Ŭ				,	Ü	Ů	Ŭ	Ů	Ŭ			•	, ,	Ŭ	Ů	Ŭ	_
Α	RW	FIELDDETECTED_ACTIVAT	E								Sh	orto	ut b	etv	vee	n FI	ELD	DE.	ГЕС	ED	evei	nt a	nd A	٩CT	IVA	TE t	ask					
											Se	e <i>E</i> V	EN1	rs_i	FIEL	DD	ETE	СТЕ	D a	nd 7	ASK	S_ <i>A</i>	CTI	VA1	Έ							
			Disabled	0							Di	sabl	e sh	orto	cut																	
			Enabled	1							En	able	sho	orto	ut																	
В	RW	FIELDLOST_SENSE									Sh	orto	ut b	etv	vee	n FI	ELD	LOS	ST e	vent	and	l SE	NSE	tas	sk							
											Se	e EV	EN1	rs_i	FIEL	DLC	OST	and	I TA	SKS_	SEI	ISE										
			Disabled	0							Di	sabl	e sh	orto	cut																	
			Enabled	1							En	able	sho	orto	ut																	

42.12.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit ı	numbe	er er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		-		01 00 23 20 27 20 23 2	T S R N M L K H G F E D C B A
	et 0x0	0000000		0 0 0 0 0 0 0 0	
Id		Field	Value Id	Value	Description
Α	RW	READY			Enable or disable interrupt for READY event
					Car EVENTE DEADY
			Disabled	0	See EVENTS_READY Disable
			Disabled Enabled	1	Enable
В	D\A/	FIELDDETECTED	Enabled	1	Enable or disable interrupt for FIELDDETECTED event
ь	KVV	FIELDDETECTED			Enable of disable interrupt for FIELDDETECTED event
					See EVENTS_FIELDDETECTED
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	FIELDLOST			Enable or disable interrupt for FIELDLOST event
					See EVENTS_FIELDLOST
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	TXFRAMESTART			Enable or disable interrupt for TXFRAMESTART event
					See EVENTS_TXFRAMESTART
			Disabled	0	Disable
			Enabled	1	Enable
E	RW	TXFRAMEEND		_	Enable or disable interrupt for TXFRAMEEND event
				_	See EVENTS_TXFRAMEEND
			Disabled	0	Disable
_			Enabled	1	Enable
F	RW	RXFRAMESTART			Enable or disable interrupt for RXFRAMESTART event
					See EVENTS_RXFRAMESTART
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	RXFRAMEEND			Enable or disable interrupt for RXFRAMEEND event
					See EVENTS_RXFRAMEEND
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	ERROR			Enable or disable interrupt for ERROR event



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	TSR NMLK HGFEDCBA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
	See EVENTS_ERROR
Disabled	0 Disable
Enabled	1 Enable
K RW RXERROR	Enable or disable interrupt for RXERROR event
	See EVENTS_RXERROR
Disabled	0 Disable
Enabled	1 Enable
L RW ENDRX	Enable or disable interrupt for ENDRX event
	See EVENTS_ENDRX
Disabled	0 Disable
Enabled	1 Enable
M RW ENDTX	Enable or disable interrupt for ENDTX event
	See EVENTS_ENDTX
Disabled	0 Disable
Enabled	1 Enable
N RW AUTOCOLRESSTARTED	Enable or disable interrupt for AUTOCOLRESSTARTED event
	See EVENTS_AUTOCOLRESSTARTED
Disabled	0 Disable
Enabled	1 Enable
R RW COLLISION	Enable or disable interrupt for COLLISION event
	See EVENTS_COLLISION
Disabled	0 Disable
Enabled	1 Enable
S RW SELECTED	Enable or disable interrupt for SELECTED event
	CON EVENTS SELECTED
Disabled	See EVENTS_SELECTED 0 Disable
Enabled	1 Enable
T RW STARTED	Enable or disable interrupt for STARTED event
8: 11:	See EVENTS_STARTED
Disabled	0 Disable
Enabled	1 Enable

42.12.3 INTENSET

Address offset: 0x304 Enable interrupt

Bit r	numbe	r		31	30	29	28 2	27 2	26 2	25 2	24	23 2	2 21	1 20	0 19	9 1	8 17	7 1	5 15	5 1	4 1	3 1	2 11	. 10	9	8	7	6	5	4	3	2 1	L 0
Id														Т	S	F	₹			1	V	Ν	1 L	K			Н	G	F	Ε	D	C E	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 (0	0	0	(0	C	0) (0	0	0	0	0	0	0	0	0	0	0	0 0	0 (
Id	RW	Field	Value Id	Va	lue							Desc	ript	ion	,																		
Α	RW	READY										Writ	e '1'	to	Ena	able	e int	teri	upt	t fo	r Ri	AD	Y e	ent/									
												See I	EVE	NTS	5_ <i>R</i> i	EAL	DΥ																
			Set	1								Enab	le																				
			Disabled	0								Read	l: Di	sab	oled																		
			Enabled	1								Reac	l: En	nab	led																		
В	RW	FIELDDETECTED										Writ	e '1'	to	Ena	able	e int	teri	upt	t fo	r FI	ELD	DET	ECT	ED	eve	nt						
												See	VEI	NTS	S_FI	ELI	DDE	TE	TE	D													
			Set	1								Enab	le																				
			Disabled	0								Read	l: Di	sab	oled																		
			Enabled	1								Read	l: En	nab	led																		
С	RW	FIELDLOST										Writ	e '1'	to	Ena	able	e int	teri	upt	t fo	r FI	ELD	LOS	Te	vent	t							



Bit r	numbe	er		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					TSR NMLK HGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
					See EVENTS_FIELDLOST
			Set	1	Enable
			Disabled	0	Read: Disabled
-	DIA	TVEDANAECTA DT	Enabled	1	Read: Enabled
D	KW	TXFRAMESTART			Write '1' to Enable interrupt for TXFRAMESTART event
					See EVENTS_TXFRAMESTART
			Set	1	Enable
			Disabled	0	Read: Disabled
_	DIM	TVEDANASENID	Enabled	1	Read: Enabled
E	RW	TXFRAMEEND			Write '1' to Enable interrupt for TXFRAMEEND event
					See EVENTS_TXFRAMEEND
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	RXFRAMESTART			Write '1' to Enable interrupt for RXFRAMESTART event
					See EVENTS_RXFRAMESTART
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	RXFRAMEEND			Write '1' to Enable interrupt for RXFRAMEEND event
					See EVENTS_RXFRAMEEND
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	ERROR			Write '1' to Enable interrupt for ERROR event
					See EVENTS_ERROR
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	RXERROR			Write '1' to Enable interrupt for RXERROR event
					See EVENTS_RXERROR
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
L	RW	ENDRX			Write '1' to Enable interrupt for ENDRX event
					See EVENTS ENDRY
			Cot	1	See EVENTS_ENDRX Enable
			Set Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
М	RW	ENDTX	Lilabica	1	Write '1' to Enable interrupt for ENDTX event
		LINDIX			
			C-t	4	See EVENTS_ENDTX
			Set	1	Enable Pand: Disabled
			Disabled	0	Read: Disabled
N	D\A/	ALITOCOL DESSTABLED	Enabled	1	Read: Enabled Write '1' to Enable interrupt for AUTOCOLPESSTAPTED event
N	KVV	AUTOCOLRESSTARTED			Write '1' to Enable interrupt for AUTOCOLRESSTARTED event
					See EVENTS_AUTOCOLRESSTARTED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
R	RW	COLLISION			Write '1' to Enable interrupt for COLLISION event

See EVENTS_COLLISION



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			TSR NMLK HGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
S RW SELECTED			Write '1' to Enable interrupt for SELECTED event
			See EVENTS_SELECTED
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
T RW STARTED			Write '1' to Enable interrupt for STARTED event
			See EVENTS_STARTED
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

42.12.4 INTENCLR

Address offset: 0x308

Disable interrupt

Dis	sable	e interrupt			
Bit	numbe	er		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					TSR NMLK HGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Disable interrupt for READY event
					See EVENTS_READY
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	FIELDDETECTED			Write '1' to Disable interrupt for FIELDDETECTED event
					See EVENTS_FIELDDETECTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	FIELDLOST			Write '1' to Disable interrupt for FIELDLOST event
					See EVENTS_FIELDLOST
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	TXFRAMESTART			Write '1' to Disable interrupt for TXFRAMESTART event
					See EVENTS_TXFRAMESTART
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Ε	RW	TXFRAMEEND			Write '1' to Disable interrupt for TXFRAMEEND event
					See EVENTS_TXFRAMEEND
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	RXFRAMESTART			Write '1' to Disable interrupt for RXFRAMESTART event
					See EVENTS_RXFRAMESTART
			Clear	1	Disable
			Disabled	0	Read: Disabled



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		T S R N M L K H G F E D C B
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Enabled	1 Read: Enabled
G RW RXFRAMEEN	D	Write '1' to Disable interrupt for RXFRAMEEND event
		See EVENTS_RXFRAMEEND
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
H RW ERROR		Write '1' to Disable interrupt for ERROR event
		See EVENTS_ERROR
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
K RW RXERROR		Write '1' to Disable interrupt for RXERROR event
		See EVENTS_RXERROR
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
L RW ENDRX		Write '1' to Disable interrupt for ENDRX event
		See EVENTS_ENDRX
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
M RW ENDTX		Write '1' to Disable interrupt for ENDTX event
		See EVENTS_ENDTX
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
N RW AUTOCOLRE	SSTARTED	Write '1' to Disable interrupt for AUTOCOLRESSTARTED event
		See EVENTS_AUTOCOLRESSTARTED
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
R RW COLLISION		Write '1' to Disable interrupt for COLLISION event
		See EVENTS_COLLISION
	Clear	1 Disable
	Disabled	0 Read: Disabled
C DW CELECTED	Enabled	1 Read: Enabled
S RW SELECTED		Write '1' to Disable interrupt for SELECTED event
		See EVENTS_SELECTED
	Clear	1 Disable
	Disabled	0 Read: Disabled
T DIA CTARTER	Enabled	1 Read: Enabled Write 11 to Disable interrupt for STARTED quest
T RW STARTED		Write '1' to Disable interrupt for STARTED event
		See EVENTS_STARTED
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled

42.12.5 ERRORSTATUS

Address offset: 0x404 NFC Error Status register



Write a bit to '1' to clear it. Writing '0' has no effect.

Bitı	numbe	er		3	1 30	29	9 28	3 27	7 26	5 25	24	23	22	21	20	19 :	18 1	17 1	6 1	5 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																															0 0		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	V	alue	9						De	scri	ptic	n																		
Α	RW	FRAMEDELAYTIMEOUT										No	STA	٩RT	TX t	task	trig	ger	ed l	bef	ore	exp	irat	ion	of t	he t	ime	e se	t in				
												FR	AM	EDE	LAY	'MA	X																
С	RW	NFCFIELDTOOSTRONG										Fie	eld le	evel	is t	00	higł	n at	ma	x lo	ad ı	esis	star	ice									
D	RW	NFCFIELDTOOWEAK										Fie	eld le	evel	is t	:00	low	at ı	nin	loa	d re	esist	and	e									

42.12.6 FRAMESTATUS.RX

Address offset: 0x40C

Result of last incoming frames

Write a bit to '1' to clear it. Writing '0' has no effect.

Bit	numbe	er		31	1 30	29	28 2	27 2	26 2	25 2	24 2	3 22	21	20	19	18	17	16	15	14 1	.3 1	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																														C E	3	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	alue						0	escr	iptic	n																		
Α	RW	CRCERROR									N	lo va	lid E	nd	of F	rar	ne (det	ecte	ed												
			CRCCorrect	0							١	'alid	CRC	de	tect	ed																
			CRCError	1							C	RC r	ecei	/ed	l do	es r	not	ma	tch	loca	ıl ch	neck										
В	RW	PARITYSTATUS									F	arity	stat	us	of r	ece	ive	d fr	am	е												
			ParityOK	0							F	rame	e rec	eiv	ed '	with	n pa	rity	OI	(
			ParityError	1							F	rame	e rec	eiv	ed v	with	n pa	rity	er	ror												
С	RW	OVERRUN									C	verr	un d	ete	ecte	d																
			NoOverrun	0							Ν	lo ov	erru	n d	lete	cte	d															
			Overrun	1							C	verr	un e	rro	r																	

42.12.7 CURRENTLOADCTRL

Address offset: 0x430

Current value driven to the NFC Load Control

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13 :	12 :	l1 1	10 9	9 :	8 7	' 6	5 5	4	3	2	1 (ı
Id																													Д	Α	Α	Α	A A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0) (0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Val	lue	:						De	scri	otic	on																			
Α	R	CURRENTLOADCTRL										Cur	ren	t va	alue	dr	iver	n to	the	NF	-C I	.oac	l Co	ntr	ol									٦.

42.12.8 FIELDPRESENT

Address offset: 0x43C

Indicates the presence or not of a valid field

Bit	numbe	er		31	. 30	29	28	3 27	20	5 25	24	4 23	3 2	2 2	21 2	0	19	18	17	16	15	14	13	3 1	2 1	1 1	0 9	9 (3 7	' 6	5 5	, 4	1 3	2	1	0
Id																																			В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	C) () () () () () () (0 0	0	0	0
Id	RW	Field	Value Id	Va	lue							D	esc	rip	tio	n																				
Α	R	FIELDPRESENT										In	dic	ate	es t	ne	pre	sei	nce	or	nc	t o	f a	vali	d fi	eld	. A	/ail	able	or	ıly i	n				
												th	ne a	cti	vat	ed	sta	te.																		
			NoField	0								Ν	o v	alio	d fie	eld	det	tec	ted																	
			FieldPresent	1								V	alic	l fie	eld	det	ect	ed																		
В	R	LOCKDETECT										In	dic	ate	es if	th	e lo	w	lev	el l	nas	lo	ke	d to	th	e fi	eld									
			NotLocked	0								N	ot l	loc	ked	to	fie	ld																		
			Locked	1								Lo	ock	ed	to 1	iel	d																			



42.12.9 FRAMEDELAYMIN

Address offset: 0x504 Minimum frame delay

Bitı	numbe	er		31	1 3	0 29	28	3 27	26	25	24	23	22	21	20	19	18 :	17 :	16 :	15 :	14 :	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ
Res	et 0x0	0000480		0	c	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	alu	e						De	scri	ptic	n																				
Α	RW	FRAMEDELAYMIN										Mi	nim	um	fra	me	del	ay i	n n	um	ber	of	13.	56	МН	z cl	lock	S							-

42.12.10 FRAMEDELAYMAX

Address offset: 0x508 Maximum frame delay

Bit	numbe	r		31	30	29	28 2	7 2	6 2	5 2	4 23	3 22	21	20	19	18	17	16	15 1	14 1	.3 1	.2 1	1 1	9	8	7	6	5	4	3	2	1	J
Id																			Α	A	Δ.	Δ /	Α Δ	A	Α	Α	Α	Α	Α	Α	A	Α.	Α
Res	et 0x0	0001000		0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	D	1 (0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																			
Α	RW	FRAMEDELAYMAX									N	axiı	nun	n fra	ame	de	lay	in r	ıum	ber	of	13.5	6 N	1Hz	clo	cks							

42.12.11 FRAMEDELAYMODE

Address offset: 0x50C

Configuration register for the Frame Delay Timer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A
Reset 0x0000001		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW FRAMEDELAYMO	DDE	Configuration register for the Frame Delay Timer
	FreeRun	0 Transmission is independent of frame timer and will start when
		the STARTTX task is triggered. No timeout.
	Window	1 Frame is transmitted between FRAMEDELAYMIN and
		FRAMEDELAYMAX
	ExactVal	2 Frame is transmitted exactly at FRAMEDELAYMAX
	WindowGrid	3 Frame is transmitted on a bit grid between FRAMEDELAYMIN
		and FRAMEDELAYMAX

42.12.12 PACKETPTR

Address offset: 0x510

Packet pointer for TXD and RXD data storage in Data RAM

Bit r	numbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20 1	L9 1	18 1	7 1	5 15	14	13	12	11 1	.0 9	9 1	3 7	7 6	5 5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Α Δ	Α	Α	Α	Α	A	4 4	Δ,	4 4	Α Α	A A	Α	Α	Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																	
Α	RW	PTR										Pac	ket	ро	inte	r fo	r TX	D a	nd R	XD	data	a st	orag	e in	n Da	ıta F	RAN	1. TI	nis			

address is a byte aligned RAM address.

42.12.13 MAXLEN

Address offset: 0x514

Size of allocated for TXD and RXD data storage buffer in Data RAM



Bit	numb	er		31	30	29 :	28 2	27 26	5 25	24	23	22	21 :	20 1	9 1	8 17	7 16	15	14	13	12	11 1	0 9	9 (3 7	6	5	4	3	2	1 ()
Id																								A	4 A	. Δ	. A	Α	Α	Α	A A	
Res	et 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0 (ı
Id	RW	Field	Value Id	Va	lue						De	scri	otio	n																		l
Α	RW	MAXLEN		[0.	.257]					Siz	e of	allo	cate	ed f	or T	XD	and	RX	D da	ita :	stora	ige	buf	fer i	in C	ata					
											RA	М																				

42.12.14 TXD.FRAMECONFIG

Address offset: 0x518

Configuration of outgoing frames

Bit r	numbe	er		31	30 2	9 2	28 2	7 2	6 25	5 2	4 23	3 22	2 21	20	19	18	17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6	5 4	3	2	1	0
Id																												[)	С	В	Α
Res	et 0x0	0000017		0	0 ()	0 0) (0 0	(0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 1	. 0	1	1	1
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
Α	RW	PARITY									A	ddir	ng pa	arity	y or	not	t in	the	fra	me												
			NoParity	0							Pa	arity	y is r	ot a	add	ed i	in T	X fr	am	es												
			Parity	1							Pa	arity	y is a	dde	ed T	X fr	ram	es														
В	RW	DISCARDMODE									Di	isca	rdin	g uı	nuse	ed b	oits	in s	tar	t or	at e	nd	of a	Frai	ne							
			DiscardEnd	0							U	nus	ed b	its i	is di	sca	rde	d a	t er	d o	fra	me										
			DiscardStart	1							U	nus	ed b	its i	is di	sca	rde	d a	t st	art o	f fr	ame	!									
С	RW	SOF									A	ddir	ng So	oF o	r no	ot ir	n TX	fra	ame	:S												
			NoSoF	0							St	art	of F	ram	ie sy	ymb	ool	not	ad	ded												
			SoF	1							St	art	of F	ram	ie sy	ymb	ool	add	led													
D	RW	CRCMODETX									CI	RC r	nod	e fo	r ou	utgo	oing	fra	ame	S												
			NoCRCTX	0							CI	RC i	s no	t ad	lded	d to	the	fra	ame	2												
			CRC16TX	1							16	5 bi	t CR	C ac	dded	d to	the	e fr	am	e ba	sed	on	all th	ne d	ata	rea	d fro	om				
											RA	٩M	that	is ı	used	d in	the	fra	ame	:												

42.12.15 TXD.AMOUNT

Address offset: 0x51C Size of outgoing frame

Bit r	numbe	er		31	. 30	29	28	27 2	26 2	25 2	24 2	3 2	22 2	1 2	0 19	9 18	17	16	15	L4 1	.3 1	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id																						В	В	В	В	В	В	В	В	3 A	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0 (0 (0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 (0	0
Id	RW	Field	Value Id	Va	lue						D	es	crip	tior	1																	
Α	RW	TXDATABITS		[0]	7]						b T b	he in	nclu DIS is d	ided CAF isca	l in t DM rde	the IOD d at	fran E fie the	ne (eld i sta	excl n FR	udii AM at	ng p ECC the	e rea arity ONFI end	bit G.T). (se	lects	s if	unı	ısec	I			
В	RW	TXDATABYTES		[0	25	7]										•		•	s th			be i	nclu	ded	l in t	he	fra	me,				

42.12.16 RXD.FRAMECONFIG

Address offset: 0x520

Configuration of incoming frames

8	/ 6	6 5	> 4	3	2 1	. 0
			С		В	Α
0	0 (0 0) 1	0	1 () 1
				С	С	8 7 6 5 4 3 2 1 C B



Bit n	umbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	l7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6 5	4	3	2	1 0
Id																													С		В	Α
Rese	t OxO	0000015		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 ()	0 0	1	0	1	0 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																	
В	RW	SOF										Sof	ex	рес	ted	or	not	in R	X fı	ram	es											
			NoSoF	0								Sta	rt o	f Fr	am	e sy	mb	ol is	no	t ex	рес	ted	in R	X fr	am	es						
			SoF	1								Sta	rt o	f Fr	am	e sy	mb	ol is	ex	pec	ted	in R	X fr	ame	es							
С	RW	CRCMODERX										CR	C m	ode	fo	rinc	om	ing	frai	nes												
			NoCRCRX	0								CR	C is	not	ex	oect	ted	in R	X fr	am	es											
			CRC16RX	1								Las	t 16	5 bit	s in	RX	fra	me	is C	RC,	CRO	is	chec	kec	d an	d CF	CS.	ΓΑΤΙ	JS			
												upo	date	ed																		

42.12.17 RXD.AMOUNT

Address offset: 0x524

Size of last incoming frame

Bit	numbe	er		31	. 30	29	28	27	26 2	5 2	24 23	3 22	21	20	19 1	8 1	7 16	15	14 1	3 12	11	10	9	8	7 (5 5	4	3	2	1 0
Id																					В	В	В	В	3 E	3 B	В	В	Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0) (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	escri	iptio	n																
Α	R	RXDATABITS									N	umb	er o	f bi	ts in	the	last	byte	e in t	he f	ram	e, if	les	s tha	ın 8	3				
											(iı	nclu	ding	CR	C, bı	ut ex	kclud	ling	parit	y an	d Sc	F/E	oF	fram	ing).				
											Fr	ame	es wi	th (0 da	ta b	ytes	and	less	thar	n 7 c	lata	bit	s are	inv	valio	ł			
											aı	nd ai	re no	ot r	ecei	ved	prop	erly												
В	R	RXDATABYTES									N	umb	er o	f co	omp	ete	byte	s re	ceive	ed in	the	frai	ne	(incl	udi	ng (CRC	,		
											bı	ıt ex	clud	ing	gpar	ity a	and S	oF/	oF f	ram	ing)									

42.12.18 NFCID1_LAST

Address offset: 0x590

Last NFCID1 part (4, 7 or 10 bytes ID)

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21 2	20 1	L9 1	8 1	7 1	.6 1	L5 1	L4 1	.3 1	2 1	1 1	0 9	9 6	3 7	6	5	4	3	2 1	1 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	C (2 (С	В	В	ВΙ	3 E	3 E	3 E	3 E	3 A	A	Α	Α	Α	A A	A A
Res	et 0x0	0006363		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	1 :	1 (0) () 1	1 1	. 0	1	1	0	0	0 1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	otio	n																		
Α	RW	NFCID1_Z										NF	CID:	l by	te Z	' (ve	ery	ast	by	te s	ent)											
В	RW	NFCID1_Y										NF	CID:	l by	te Y	′																	
С	RW	NFCID1_X										NF	CID:	l by	te >	(
D	RW	NFCID1 W										NF	CID:	L by	te V	Ν																	

42.12.19 NFCID1_2ND_LAST

Address offset: 0x594

Second last NFCID1 part (7 or 10 bytes ID)

Bit r	numbe	er		31 3	0 29	28	3 27	7 26	25	24	23	22 :	21 2	20 1	9 1	8 17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id											С	С	С	C (C (C C	: C	В	В	В	В	В	В	В	В	Α	Α	Α	Α	A A	Α Α	A
Res	et 0x0	0000000		0 (0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Valu	e						Des	crip	otio	n																		
Α	RW	NFCID1_V									NFO	CID1	by	te V	,																	
В	RW	NFCID1_U									NFO	CID1	by	te L	J																	
С	RW	NFCID1 T									NFO	CID1	bv	te T																		

42.12.20 NFCID1_3RD_LAST

Address offset: 0x598

Third last NFCID1 part (10 bytes ID)



Bit r	numbe	er		31 30	29	28	27	26 2	25 2	24 2	23 2	22 2	1 20) 19	18	17	16	15 1	4 1	3 12	11	10	9	8 7	6	5	4	3	2	1 0
Id											С	C (C C	С	С	С	С	В	ВЕ	3 B	В	В	В	B A	A	. A	Α	Α	Α	АА
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	•					ı	Des	crip	tion																	
Α	RW	NFCID1_S								ı	NFC	ID1	byt	e S																
В	RW	NFCID1_R								1	NFC	ID1	byt	e R																
С	RW	NFCID1_Q								ı	NFC	ID1	byt	e Q																

42.12.21 SENSRES

Address offset: 0x5A0

NFC-A SENS_RES auto-response settings

Bit n	umbe	er		31	30 2	9 28	3 27	7 26	25	24 2	23 2:	2 21	. 20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5 4	1 3	2	1	0
Id																		Ε	Ε	E E	Ε [D D	D	D	С	С	В	А А	Α	Α	Α
Rese	t 0x0	0000001		0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 (0	0	0	1
Id	RW	Field	Value Id	Val	ue						Desc	ripti	ion																		
Α	RW	BITFRAMESDD								E	3it fr	ame	SD	D as	de	fine	ed b	y t	he l	b5:b	1 o	byt	e 1 i	n Sl	ENS	_RE	S				
										r	espo	onse	in t	the	NFC	Fo	run	n, N	IFC	Digit	tal I	roto	ocol	Tec	hni	cal					
										5	Spec	ifica	tion	ı																	
			SDD00000	0						5	SDD	patt	ern	000	000																
			SDD00001	1						5	SDD	patt	ern	000	01																
			SDD00010	2						5	SDD	patt	ern	000	10																
			SDD00100	4						5	SDD	patt	ern	001	.00																
			SDD01000	8						5	SDD	patt	ern	010	000																
			SDD10000	16						5	SDD	patt	ern	100	000																
В	RW	RFU5								F	Rese	rvec	for	fut	ure	use	e. Sl	hall	be	0.											
С	RW	NFCIDSIZE								١	NFCI	D1 s	ize.	Thi	s va	lue	is u	ısed	d by	the (Au	to co	ollisi	on i	resc	oluti	ion				
										e	engir	ne.																			
			NFCID1Single	0						١	NFCI	D1 s	ize:	sing	gle	(4 b	yte	s)													
			NFCID1Double	1						١	NFCI	D1 s	ize:	dou	ıble	(7	byt	es)													
			NFCID1Triple	2						١	NFCI	D1 s	ize:	trip	le (10 l	oyte	es)													
D	RW	PLATFCONFIG								1	Гад р	olatf	orm	COI	nfig	ura	tior	n as	de	fined	d by	the	b4:	b1 c	of b	yte	2				
										i	n SE	NS_	RES	res	pon	se i	n tl	he I	NFC	For	um	, NFC	Dig	gital	Pro	otoc	ol				
										1	Гесh	nica	l Sp	ecif	icat	ion															
E	RW	RFU74								F	Rese	rvec	for	fut	ure	use	e. Sl	hall	be	0.											

42.12.22 SELRES

Address offset: 0x5A4

NFC-A SEL_RES auto-response settings

Bit r	iumbe	er		33	L 30	29	28	27	26	25	24	23	22	21 2	0	19 1	L8 :	17 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																												Ε	D	D	С	С	В	A	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	alue							Des	scri	ptio	n																				
Α	RW	RFU10										Res	serv	ed f	or	futu	ire	use	. Sł	nall	be	0.													_
В	RW	CASCADE										Cas	scac	le bi	t (c	ont	rol	led	by	har	dw	are	, w	rite	ha	s no	eff	ec	t)						
			Complete	0								NF	CID	1 co	mp	lete)																		
			NotComplete	1								NF	CID	1 no	t co	omp	let	:e																	
С	RW	RFU43										Res	serv	ed f	or	futu	ire	use	. Sł	nall	be	0.													
D	RW	PROTOCOL										Pro	otoc	ol a	s de	efin	ed	by t	he	b7:	b6	of:	SEL	_RE	S r	esp	onse	e ir	the	e					
												NF	C Fo	run	ı, N	IFC	Dig	ital	Pro	oto	col	Tec	hn	ical	Spe	ecif	icati	on							
E	RW	RFU7										Res	serv	ed f	or	futu	ıre	use	. Sł	nall	be	0.													



42.13 Electrical Specification

42.13.1 NFCT Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
f_c	Frequency of operation		13.56		MHz
C _{MI}	Carrier modulation index	95			%
DR	Data Rate		106		kbps
$f_{\scriptscriptstyle S}$	Modulation sub-carrier frequency		f _c /16		MHz
V_{swing}	Peak differential Input voltage swing on NFC1 and NFC2			VDD	Vp
V _{sense}	Peak differential Field detect threshold level on NFC1-NFC2 ³⁵		1.0		Vp
I _{sense}	Current in SENSE STATE ³⁶		700		nA
R _{in_min}	Minimum input resistance when regulating voltage swing			40	Ω
R _{in_max}	Maximum input resistance when regulating voltage swing	1.0			kΩ
R _{in_loadmod}	Input resistance when load modulating	8		22	Ω
I _{max}	Maximum input current on NFC pins			80	mA

42.13.2 NFCT Timing Parameters

Symbol	Description	Min.	Тур.	Max.	Units
t _{activate}	Time from task_ACTIVATE in SENSE or DISABLE state to			500	us
	ACTIVATE_A or IDLE state ³⁷				
t _{sense}	Time from remote field is present in SENSE mode to			20	us
	FIELDDETECTED event is asserted				

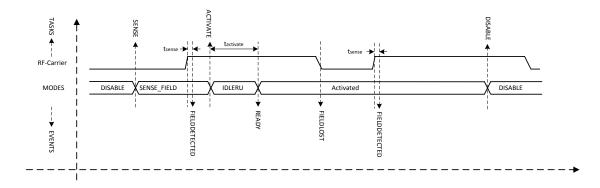


Figure 122: NFCT timing parameters (Shortcuts for FIELDDETECTED and FIELDLOST are disabled)

Input is high impedance in sense mode

This is whole device current when the device is in system off, OK RAM retained and the NFC peripheral is in sense mode.

Does not account for voltage supply and oscillator startup times



43 PDM — Pulse density modulation interface

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (Left and Right) data input. Data is transferred directly to RAM buffers using EasyDMA.

Listed here are the main features for PDM:

- · Up to two PDM microphones configured as a Left/Right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- · HW decimation filters

The PDM module illustrated in *Figure 123: PDM module* on page 432 is interfacing up to two digital microphones with the PDM interface. It implements EasyDMA, which relieves real-time requirements associated with controlling the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce PCM samples. The PDM module allows continuous audio streaming.

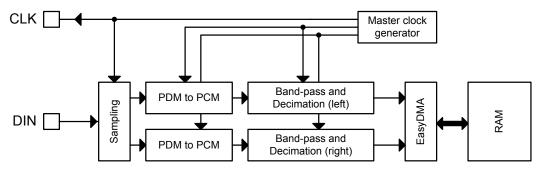


Figure 123: PDM module

43.1 Master clock generator

The FREQ field in the master clock's PDMCLKCTRL register allows adjusting the PDM clock's frequency.

The master clock generator does not add any jitter to the HFCLK source chosen. It is recommended (but not mandatory) to use the Xtal as HFCLK source.

43.2 Module operation

By default, bits from the left PDM microphone are sampled on PDM_CLK falling edge, bits for the right are sampled on the rising edge of PDM_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the PDM stream into 16-bit PCM samples, and filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping Left and Right, so that Left will be sampled on rising edge, and Right on falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM.

Depending on the mode chosen in the OPERATION field in the MODE register, memory either contains alternating left and right 16-bit samples (Stereo), or only left 16-bit samples (Mono).

To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.

The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The



STOPPED event indicates that all activity in the module are finished, and that the data is available in RAM (EasyDMA has finished transferring as well). Attempting to restart before receiving the STOPPED event may result in unpredictable behaviour.

43.3 Decimation filter

In order to convert the incoming data stream into PCM audio samples, a decimation filter is included in the PDM interface module.

The input of the filter is the two-channel PDM serial stream (with left channel on clock high, right channel on clock low), its output is 2×16 -bit PCM samples at a sample rate 64 times lower than the PDM clock rate.

The filter stage of each channel is followed by a digital volume control, to attenuate or amplify the output samples in a range of -20 dB to +20 dB around the default (reset) setting, defined by $G_{PDM,default}$. The gain is controlled by the GAINL and GAINR registers.

As an example, if the goal is to achieve 2500 RMS output samples (16 bit) with a 1 kHz 90 dBA signal into a -26 dBFS sensitivity PDM microphone, the user will have to sum the PDM module's default gain (G_{PDM,default}) and the gain introduced by the microphone and acoustic path of his implementation (an attenuation would translate into a negative gain), and adjust GAINL and GAINR by this amount. Assuming that only the PDM module influences the gain, GAINL and GAINR must be set to -G_{PDM,default} dB to achieve the requirement.

With G_{PDM,default}=3.2 dB, and as GAINL and GAINR are expressed in 0.5 dB steps, the closest value to program would be 3.0 dB, which can be calculated as:

```
GAINL = GAINR = (DefaultGain - (2 * 3))
```

Remember to check that the resulting values programmed into GAINL and GAINR fall within MinGain and MaxGain.

43.4 EasyDMA

Samples will be written directly to RAM, and EasyDMA must be configured accordingly.

The address pointer for the EasyDMA channel is set in SAMPLE.PTR register. If the destination address set in SAMPLE.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

DMA supports Stereo (Left+Right 16-bit samples) and Mono (Left only) data transfer, depending on setting in the OPERATION field in the MODE register. The samples are stored little endian.

Table 97: DMA sample storage

MODE.OPERATION	Bits per sample	Result stored per RAM word	Physical RAM allocated (32 bit words)	Result boundary indexes in RAM	Note
Stereo	32 (2x16)	L+R	ceil(SAMPLE.MAXCNT/2)	R0=[31:16]; L0=[15:0]	Default
Mono	16	2xL	ceil(SAMPLE.MAXCNT/2)	L1=[31:16]; L0=[15:0]	

The destination buffer in RAM consists of one block, the size of which is set in SAMPLE.MAXCNT register. Format is number of 16-bit samples. The physical RAM allocated is always:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 2;
```

(but the mapping of the samples depends on MODE.OPERATION.

If OPERATION=Stereo, RAM will contain a succession of Left and Right samples.

If OPERATION=Mono, RAM will contain a succession of mono samples.

For a given value of SAMPLE.MAXCNT, the buffer in RAM can contain half the stereo sampling time as compared to the mono sampling time.



The PDM acquisition can be started by the START task, after the SAMPLE.PTR and SAMPLE.MAXCNT registers have been written. When starting the module, it will take some time for the filters to start outputting valid data. Transients from the PDM microphone itself may also occur. The first few samples (typically around 50) might hence contain invalid values or transients. It is therefore advised to discard the first few samples after a PDM start.

As soon as the STARTED event is received, the firmware can write the next SAMPLE.PTR value (this register is double-buffered), to ensure continuous operation.

When the buffer in RAM is filled with samples, an END event is triggered. The firmware can start processing the data in the buffer. Meanwhile, the PDM module starts acquiring data into the new buffer pointed to by SAMPLE.PTR, and sends a new STARTED event, so that the firmware can update SAMPLE.PTR to the next buffer address.

43.5 Hardware example

Connect the microphone clock to CLK, and data to DIN.

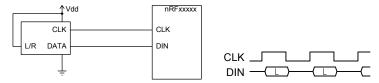


Figure 124: Example of a single PDM microphone, wired as left



Figure 125: Example of a single PDM microphone, wired as right

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data. If two microphones are used, one of them has to be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

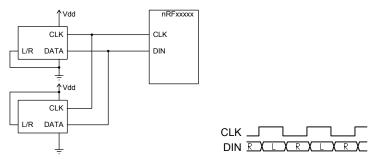


Figure 126: Example of two PDM microphones

43.6 Pin configuration

The CLK and DIN signals associated to the PDM module are mapped to physical pins according to the configuration specified in the PSEL.CLK and PSEL.DIN registers respectively. If the CONNECT field in any PSEL register is set to Disconnected, the associated PDM module signal will not be connected to the required physical pins, and will not operate properly.



The PSEL.CLK and PSEL.DIN registers and their configurations are only used as long as the PDM module is enabled, and retained only as long as the device is in System ON mode. See *POWER — Power supply* on page 76 for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To ensure correct behaviour in the PDM module, the pins used by the PDM module must be configured in the GPIO peripheral as described in *Table 98: GPIO configuration before enabling peripheral* on page 435 before enabling the PDM module. This is to ensure that the pins used by the PDM module are driven correctly if the PDM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the PDM module is supposed to be connected to an external PDM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.

Table 98: GPIO configuration before enabling peripheral

PDM signal	PDM pin	Direction	Output value	Comment
CLK	As specified in PSEL.CLK	Output	0	
DIN	As specified in PSEL.DIN	Input	Not applicable	

43.7 Registers

Table 99: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001D000	PDM	PDM	Pulse Density Modulation (Digital	
			Microphone) Interface	

Table 100: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous PDM transfer
TASKS_STOP	0x004	Stops PDM transfer
EVENTS_STARTED	0x100	PDM transfer has started
EVENTS_STOPPED	0x104	PDM transfer has finished
EVENTS_END	0x108	The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP
		task has been received) to Data RAM
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PDM module enable register
PDMCLKCTRL	0x504	PDM clock generator control
MODE	0x508	Defines the routing of the connected PDM microphones' signals
GAINL	0x518	Left output gain adjustment
GAINR	0x51C	Right output gain adjustment
PSEL.CLK	0x540	Pin number configuration for PDM CLK signal
PSEL.DIN	0x544	Pin number configuration for PDM DIN signal
SAMPLE.PTR	0x560	RAM address pointer to write samples to with EasyDMA
SAMPLE.MAXCNT	0x564	Number of samples to allocate memory for in EasyDMA mode

43.7.1 INTEN

Address offset: 0x300 Enable or disable interrupt



Bit r	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW STARTED			Enable or disable interrupt for STARTED event
				See EVENTS_STARTED
		Disabled	0	Disable
		Enabled	1	Enable
В	RW STOPPED			Enable or disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Disabled	0	Disable
		Enabled	1	Enable
С	RW END			Enable or disable interrupt for END event
				See EVENTS_END
		Disabled	0	Disable
		Enabled	1	Enable

43.7.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Res	et 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW STARTED			Write '1' to Enable interrupt for STARTED event
				See EVENTS_STARTED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

43.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	numbe	er		31	. 30	29	28	3 27	26	5 25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																	С	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																			
Α	RW	STARTED										W	rite	'1'	to [Disa	ble	int	err	upt	for	ST	٩RT	ED	eve	ent								
												Se	e <i>E</i> ۱	/EN	TS_	STA	4 <i>R</i> 7	ED																
			Clear	1								Di	sabl	e																				
			Disabled	0								Re	ad:	Dis	abl	ed																		
			Enabled	1								Re	ad:	Ena	able	d																		
В	RW	STOPPED										W	rite	'1'	to [Disa	ble	int	err	upt	for	ST	OPF	PED	ev	ent								



Bit number Id		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 C B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_STOPPED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW END			Write '1' to Disable interrupt for END event
			See EVENTS_END
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

43.7.4 ENABLE

Address offset: 0x500

PDM module enable register

Bit	num	nber			31	30	29 2	28 :	27 :	26	25 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0	00x0	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	R۱	W	Field	Value Id	Val	ue							De	scri	pti	on																			
Α	R۱	W	ENABLE										Ena	ble	or	dis	abl	e P	DM	mo	odu	le													
				Disabled	0								Dis	abl	e																				
				Enabled	1								Ena	ble	9																				

43.7.5 PDMCLKCTRL

Address offset: 0x504

PDM clock generator control

Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22	21 :	20	19 1	18 1	17 1	16 1	15 :	14 1	13 1	.2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α,	A .	Α	Α	Α.	4 /	A	Α	Α	Α	Α	Α	Α	Α	Α	A	Α
Rese	t 0x0	8400000		0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0
ld	RW	Field	Value Id	Va	lue							De	scri	ptio	n																			
Α	RW	FREQ										PD	M_(CLK	fre	que	ncy																	
			1000K	0x0	080	000	000					PD	M_(CLK	= 3	2 N	lHz	/ 32	2 =	1.0	00 1	МΗ	Z											
			Default	0x0	084	000	000					PD	M_(CLK	= 3	2 N	lHz	/ 31	1 =	1.0	32 I	МΗ	Z											
			1067K	0x0	088	000	000					PD	M_(CLK	= 3	2 N	lHz	/ 30) =	1.0	67 I	МΗ	Z											

43.7.6 MODE

Address offset: 0x508

Defines the routing of the connected PDM microphones' signals

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		В .
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW OPERATION		Mono or stereo operation
	Stereo	0 Sample and store one pair (Left + Right) of 16bit samples per
		RAM word R=[31:16]; L=[15:0]
	Mono	1 Sample and store two successive Left samples (16 bit each) per
		RAM word L1=[31:16]; L0=[15:0]
B RW EDGE		Defines on which PDM_CLK edge Left (or mono) is sampled
	LeftFalling	0 Left (or mono) is sampled on falling edge of PDM_CLK
	LeftRising	1 Left (or mono) is sampled on rising edge of PDM_CLK



43.7.7 GAINL

Address offset: 0x518

Left output gain adjustment

43.7.8 GAINR

Address offset: 0x51C

Right output gain adjustment

Bit	numbe	er		33	1 30	29	28	3 27	7 2	6 2	5 2	4 2	3 2	2 2	21 2	20 2	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																													Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000028		0	0	0	0	0	(0	0) () () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
Id	RW	Field	Value Id	V	alue							D	esc	rip	tio	n																				
Α	RW	GAINR										R	igh	t oı	utp	ut 8	gaiı	n a	dju	stm	en	t, ir	0.5	dE	ste	ps,	arc	ound	l th	ne						
												d	efa	ult	mc	du	le g	gaiı	ı (s	ee	ele	ctri	cal _l	oara	ame	ter	s)									
			MinGain	0>	x00							-2	20d	Вg	gain	ad	jus	tm	ent	(m	iniı	nuı	m)													
			DefaultGain	0>	x28							0	dB	gai	n a	dju	stn	ner	ıt ('	250	00 F	RMS	s' re	qui	ren	nen	t)									
			MaxGain	0>	x50							+	20c	dB g	gair	n ac	djus	stm	en	t (n	nax	imι	ım)													
			DefaultGain	0>	x28							d -:	efa 20d dB	ult B g gai	mo gain n a	du ad dju	le g jus stn	gaii tm ner	n (s ent nt ('	ee (m 250	eleo inii 00 F	tri mui	cal m) S' re	oara equi	ame	ter	s)									

43.7.9 PSEL.CLK

Address offset: 0x540

Pin number configuration for PDM CLK signal

Bit	numbe	er		31	30 2	9 2	8 2	7 2	6 25	5 24	23	22	21	20 :	19 1	l8 1	7 16	5 15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				С																								Α ,	A A	Α	Α
Res	et OxF	FFFFFF		1	1	1 :	1 1	. 1	l 1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1 1	1	1	1	1	1	1	l 1	1	1
Id	RW	Field	Value Id	Va	lue						De	scri	ptio	n																	
Α	RW	PIN		[0.	.31]						Pir	n nu	mbe	er																	
С	RW	CONNECT									Со	nne	ctio	n																	
			Disconnected	1							Dis	scon	nec	t:																	
			Connected	0							Со	nne	ct																		

43.7.10 PSEL.DIN

Address offset: 0x544



Pin number configuration for PDM DIN signal

Bit	numb	er		31 30	29	28 2	27 2	26 2	5 24	4 23	3 22	21	20	19 1	L8 1	7 16	15	14 1	.3 12	11	10 !	9 8	7	6	5	4	3 2	2 1	0
Id				С																						Α	A A	A	Α
Re	et OxF	FFFFFF		1 1	1	1	1	1 1	l 1	. 1	. 1	1	1	1	1 1	. 1	1	1	1 1	1	1	1 1	. 1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value						D	escri	iptic	on																
Α	RW	PIN		[031]]					Pi	in nu	ımb	er																
С	RW	CONNECT								Co	onne	ectio	n																
			Disconnected	1						Di	iscor	nnec	ct																
			Connected	0						Co	onne	ect																	

43.7.11 SAMPLE.PTR

Address offset: 0x560

RAM address pointer to write samples to with EasyDMA

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19 1	18 1	17 1	16 1	.5 1	4 1	3 1	2 1	1 1	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Α,	Δ,	Δ Α	4 Α	۱ ۸	Δ Δ	. Α	. A	Α	Α	Α	Α	Α .	Δ /	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0 () (0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	n																		
Α	RW	SAMPLEPTR										Add	dres	ss to	o w	rite	PDI	M s	amı	oles	to	ove	er D	MA									

43.7.12 SAMPLE.MAXCNT

Address offset: 0x564

Number of samples to allocate memory for in EasyDMA mode

Bit number		31 30 29 28 27 26 25 24 23 22 21 20	0 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description	1
A RW BUFFSIZE		[032767] Length of D	OMA RAM allocation in number of samples

43.8 Electrical Specification

43.8.1 PDM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PDM,stereo}	PDM module active current, stereo operation ³⁸		1.4		mA
f _{PDM,CLK}	PDM clock speed		1.032		MHz
t _{PDM,JITTER}	Jitter in PDM clock output			20	ns
T _{dPDM,CLK}	PDM clock duty cycle	40	50	60	%
t _{PDM,DATA}	Decimation filter delay			5	ms
t _{PDM,cv}	Allowed clock edge to data valid			125	ns
t _{PDM,ci}	Allowed (other) clock edge to data invalid	0			ns
t _{PDM,s}	Data setup time at f _{PDM,CLK} =1.024 MHz	65			ns
t _{PDM,h}	Data hold time at f _{PDM,CLK} =1.024 MHz	0			ns
G _{PDM} ,default	Default (reset) absolute gain of the PDM module		3.2		dB

³⁸ Average current including PDM and DMA transfers, excluding clock and power supply base currents



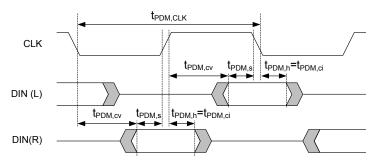


Figure 127: PDM timing diagram



44 I²S — Inter-IC sound interface

The I²S (Inter-IC Sound) module, supports the original two-channel I²S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention.

The I²S peripheral has the following main features:

- · Master and Slave mode
- Simultaneous bi-directional (TX and RX) audio streaming
- Original I²S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- · Low-jitter Master Clock generator
- · Various sample rates

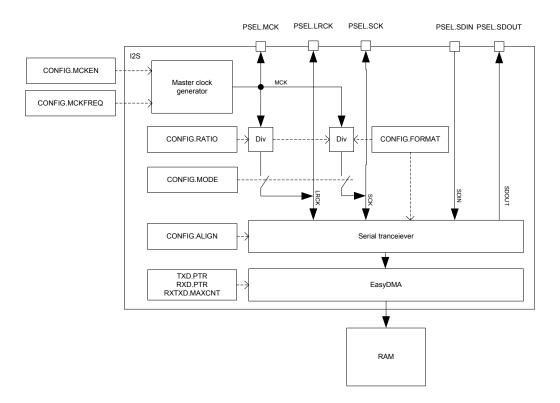


Figure 128: I²S master

44.1 Mode

The I²S protocol specification defines two modes of operation, Master and Slave.

The I²S mode decides which of the two sides (Master or Slave) shall provide the clock signals LRCK and SCK, and these signals are always supplied by the Master to the Slave.

44.2 Transmitting and receiving

The I^2S module supports both transmission (TX) and reception (RX) of serial data. In both cases the serial data is shifted synchronously to the clock signals SCK and LRCK.



TX data is written to the SDOUT pin on the falling edge of SCK, and RX data is read from the SDIN pin on the rising edge of SCK. The most significant bit (MSB) is always transmitted first.

TX and RX are available in both Master and Slave modes and can be enabled/disabled independently in the *CONFIG.TXEN* on page 451 and *CONFIG.RXEN* on page 451.

Transmission and/or reception is started by triggering the START task. When started and transmission is enabled (in *CONFIG.TXEN* on page 451), the TXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 454 number of transmitted data words (containing one or more samples). Similarly, when started and reception is enabled (in *CONFIG.RXEN* on page 451), the RXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 454 received data words.

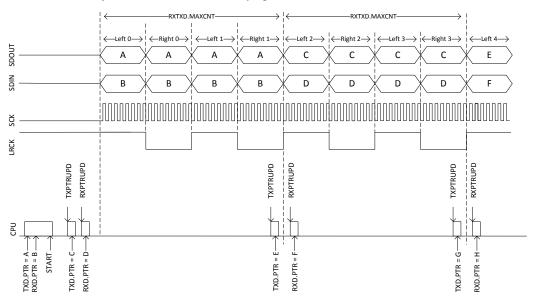


Figure 129: Transmitting and receiving. CONFIG.FORMAT = Aligned, CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo, RXTXD.MAXCNT = 1.

44.3 Left right clock (LRCK)

The Left Right Clock (LRCK), often referred to as "word clock", "sample clock" or "word select" in I²S context, is the clock defining the frames in the serial bit streams sent and received on SDOUT and SDIN, respectively.

In I2S mode, each frame contains one left and right sample pair, with the left sample being transferred during the low half period of LRCK followed by the right sample being transferred during the high period of LRCK.

In Aligned mode, each frame contains one left and right sample pair, with the left sample being transferred during the high half period of LRCK followed by the right sample being transferred during the low period of LRCK.

Consequently, the LRCK frequency is equivalent to the audio sample rate.

When operating in Master mode, the LRCK is generated from the MCK, and the frequency of LRCK is then given as:

```
LRCK = MCK / CONFIG.RATIO
```

LRCK always toggles around the falling edge of the serial clock SCK.

44.4 Serial clock (SCK)

The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.



When operating in Master mode the SCK is generated from the MCK, and the frequency of SCK is then given as:

```
SCK = 2 * LRCK * CONFIG.SWIDTH
```

The falling edge of the SCK falls on the toggling edge of LRCK.

When operating in Slave mode SCK is provided by the external I²S master.

44.5 Master clock (MCK)

The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode.

The MCK is generated by an internal MCK generator. This generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in slave mode can be useful in the case where the external Master is not able to generate its own master clock.

The MCK generator is enabled/disabled in the register *CONFIG.MCKEN* on page 452, and the generator is started or stopped by the START or STOP tasks.

In Master mode the LRCK and the SCK frequencies are closely related, as both are derived from MCK and set indirectly through *CONFIG.RATIO* on page 452 and *CONFIG.SWIDTH* on page 453.

When configuring these registers, the user is responsible for fulfilling the following requirements:

1. SCK frequency can never exceed the MCK frequency, which can be formulated as:

```
CONFIG.RATIO >= 2 * CONFIG.SWIDTH
```

2. The MCK/LRCK ratio shall be a multiple of 2 * CONFIG.SWIDTH, which can be formulated as:

```
Integer = (CONFIG.RATIO / (2 * CONFIG.SWIDTH))
```

The MCK signal can be routed to an output pin (specified in PSEL.MCK) to supply external I²S devices that require the MCK to be supplied from the outside.

When operating in Slave mode, the I²S module does not use the MCK and the MCK generator does not need to be enabled.

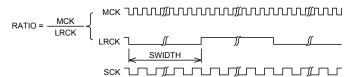


Figure 130: Relation between RATIO, MCK and LRCK.

Table 101: Configuration examples

16000	16Bit					LRCK error [%]
	TODIC	32X	32MDIV63	507936.5	15873.0	-0.8
16000	16Bit	64X	32MDIV31	1032258.1	16129.0	0.8
16000	16Bit	256X	32MDIV8	4000000.0	15625.0	-2.3
32000	16Bit	32X	32MDIV31	1032258.1	32258.1	0.8
32000	16Bit	64X	32MDIV16	2000000.0	31250.0	-2.3
32000	16Bit	256X	32MDIV4	0.000008	31250.0	-2.3
44100	16Bit	32X	32MDIV23	1391304.3	43478.3	-1.4
44100	16Bit	64X	32MDIV11	2909090.9	45454.5	3.1
44100	16Bit	256X	32MDIV3	10666666.7	41666.7	-5.5

44.6 Width, alignment and format

The CONFIG.SWIDTH register primarily defines the sample width of the data written to memory. In master mode, it then also sets the amount of bits per frame. In Slave mode it controls padding/trimming if required. Left, right, transmitted, and received samples always have the same width. The CONFIG.FORMAT register specifies the position of the data frames with respect to the LRCK edges in both Master and Slave modes.



When using I²S format, the first bit in a half-frame (containing one left or right sample) gets sampled on the second rising edge of the SCK after a LRCK edge. When using Aligned mode, the first bit in a half-frame gets sampled on the first rising edge of SCK following a LRCK edge.

For data being received on SDIN the sample value can be either right or left-aligned inside a half-frame, as specified in *CONFIG.ALIGN* on page 453. *CONFIG.ALIGN* on page 453 affects only the decoding of the incoming samples (SDIN), while the outgoing samples (SDOUT) are always left-aligned (or justified).

When using left-alignment, each half-frame starts with the MSB of the sample value (both for data being sent on SDOUT and received on SDIN).

When using right-alignment, each half-frame of data being received on SDIN ends with the LSB of the sample value, while each half-frame of data being sent on SDOUT starts with the MSB of the sample value (same as for left-alignment).

In Master mode, the size of a half-frame (in number of SCK periods) equals the sample width (in number of bits), and in this case the alignment setting does not care as each half-frame in any case will start with the MSB and end with the LSB of the sample value.

In slave mode, however, the sample width does not need to equal the frame size. This means you might have extra or fewer SCK pulses per half-frame than what the sample width specified in *CONFIG.SWIDTH* requires.

In the case where we use **left-alignment** and the number of SCK pulses per half-frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits after the LSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0.

In the case where we use **left-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

· Data sent and received on SDOUT and SDIN will be truncated with the LSBs being removed first.

In the case where we use **right-alignment** and the number of SCK pulses per frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits before the MSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0 (same behavior as for left-alignment).

In the case where we use **right-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data received on SDIN will be sign-extended to "sample width" number of bits before being written to memory.
- Data sent on SDOUT will be truncated with the LSBs being removed first (same behavior as for leftalignment).

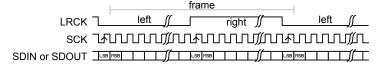


Figure 131: I²S format. CONFIG.SWIDTH equalling half-frame size.

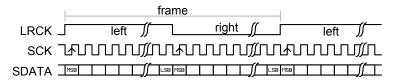


Figure 132: Aligned format. CONFIG.SWIDTH equalling half-frame size.



44.7 EasyDMA

The I²S module implements EasyDMA for accessing internal Data RAM without CPU intervention.

The source and destination pointers for the TX and RX data are configured in *TXD.PTR* on page 454 and *RXD.PTR* on page 454. The memory pointed to by these pointers will only be read or written when TX or RX are enabled in *CONFIG.TXEN* on page 451 and *CONFIG.RXEN* on page 451.

The addresses written to the pointer registers *TXD.PTR* on page 454 and *RXD.PTR* on page 454 are double-buffered in hardware, and these double buffers are updated for every *RXTXD.MAXCNT* on page 454 words (containing one or more samples) read/written from/to memory. The events TXPTRUPD and RXPTRUPD are generated whenever the TXD.PTR and RXD.PTR are transferred to these double buffers.

If *TXD.PTR* on page 454 is not pointing to the Data RAM region when transmission is enabled, or *RXD.PTR* on page 454 is not pointing to the Data RAM region when reception is enabled, an EasyDMA transfer may result in a HardFault and/or memory corruption. See *Memory* on page 20 for more information about the different memory regions.

Due to the nature of I²S, where the number of transmitted samples always equals the number of received samples (at least when both TX and RX are enabled), one common register *RXTXD.MAXCNT* on page 454 is used for specifying the sizes of these two memory buffers. The size of the buffers is specified in a number of 32-bit words. Such a 32-bit memory word can either contain four 8-bit samples, two 16-bit samples or one right-aligned 24-bit sample sign extended to 32 bit.

In stereo mode (decided by CONFIG.CHANNELS), the samples are stored as "left and right sample pairs" in memory. Figure Figure 133: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo. on page 445, Figure 135: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo. on page 446 and Figure 137: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo. on page 446 show how the samples are mapped to memory in this mode.

In mono mode (left or right channel only), samples for only one single channel are stored in memory. Figure Figure 134: Memory mapping for 8 bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left. on page 446, Figure 136: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left. on page 446 and Figure 138: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left. on page 447 show how samples are mapped to memory in this mode.

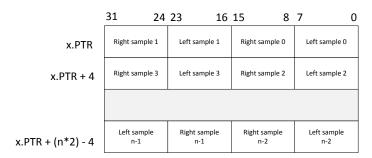


Figure 133: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo.



	31 24	23 16	15 8	7 0
x.PTR	Left sample 3	Left sample 2	Left sample 1	Left sample 0
x.PTR + 4	Left sample 7	Left sample 6	Left sample 5	Left sample 4
x.PTR + n - 4	Left sample n-1	Left sample n-2	Left sample n-3	Left sample n-4

Figure 134: Memory mapping for 8 bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left.

	31 16	15	0
x.PTR	Right sample 0	Left sample 0	
x.PTR + 4	Right sample 1	Left sample 1	
x.PTR + (n*4) - 4	Right sample n - 1	Left sample n - 1	

Figure 135: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo.

	31 16	15 0
x.PTR	Left sample 1	Left sample 0
x.PTR + 4	Left sample 3	Left sample 2
x.PTR + (n*2) - 4	Left sample n - 1	Left sample n - 2

Figure 136: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left.

	31	23 0
x.PTR	Sign ext.	Left sample 0
x.PTR + 4	Sign ext.	Right sample 0
x.PTR + (n*8) - 8	Sign ext.	Left sample n - 1
x.PTR + (n*8) - 4	Sign ext.	Right sample n - 1

Figure 137: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo.



	31	23 0
x.PTR	Sign ext.	Left sample 0
x.PTR + 4	Sign ext.	Left sample 1
x.PTR + (n*4) - 4	Sign ext.	Left sample n - 1

Figure 138: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left.

44.8 Module operation

Described here is a typical operating procedure for the I²S module.

1. Configure the I²S module using the CONFIG registers

```
// Enable reception
NRF I2S->CONFIG.RXEN = (I2S CONFIG RXEN RXEN Enabled <<
                                        I2S_CONFIG_RXEN_RXEN_Pos);
// Enable transmission
NRF I2S->CONFIG.TXEN = (I2S CONFIG TXEN TXEN Enabled <<
                                        I2S CONFIG_TXEN_TXEN_Pos);
// Enable MCK generator
NRF_I2S->CONFIG.MCKEN = (I2S_CONFIG_MCKEN_MCKEN_Enabled <<</pre>
                                        12S CONFIG MCKEN MCKEN Pos);
// MCKFREQ = 4 MHz
NRF_12S->CONFIG.MCKFREQ = 12S_CONFIG_MCKFREQ_MCKFREQ_32MDIV8 <<
                                        12S CONFIG MCKFREQ MCKFREQ Pos;
// Ratio = 256
NRF I2S->CONFIG.RATIO = I2S CONFIG RATIO RATIO 256X <<
                                       12S CONFIG RATIO RATIO Pos;
// MCKFREQ = 4 MHz and Ratio = 256 gives sample rate = 15.625 ks/s
// Sample width = 16 bit
NRF I2S->CONFIG.SWIDTH = I2S CONFIG SWIDTH SWIDTH 16Bit <<
                                        12S CONFIG SWIDTH SWIDTH Pos;
// Alignment = Left
NRF I2S->CONFIG.ALIGN = I2S CONFIG ALIGN ALIGN Left <<
                                       12S CONFIG ALIGN ALIGN Pos;
// Format = I2S
NRF I2S->CONFIG.FORMAT = I2S CONFIG FORMAT FORMAT I2S <<
                                        12S CONFIG FORMAT FORMAT Pos;
// Use stereo
NRF 12S->CONFIG.CHANNELS = 12S CONFIG CHANNELS CHANNELS Stereo <<
                                        12S CONFIG CHANNELS CHANNELS Pos;
```

2. Map IO pins using the PINSEL registers



3. Configure TX and RX data pointers using the TXD, RXD and RXTXD registers

```
NRF_I2S->TXD.PTR = my_tx_buf;
NRF_I2S->RXD.PTR = my_rx_buf;
NRF_I2S->TXD.MAXCNT = MY_BUF_SIZE;
```

4. Enable the I²S module using the ENABLE register

```
NRF_I2S->ENABLE = 1;
```

5. Start audio streaming using the START task

```
NRF_I2S->TASKS_START = 1;
```

6. Handle received and transmitted data when receiving the TXPTRUPD and RXPTRUPD events

```
if (NRF_I2S->EVENTS_TXPTRUPD != 0)
{
    NRF_I2S->TXD.PTR = my_next_tx_buf;
    NRF_I2S->EVENTS_TXPTRUPD = 0;
}

if (NRF_I2S->EVENTS_RXPTRUPD != 0)
{
    NRF_I2S->RXD.PTR = my_next_rx_buf;
    NRF_I2S->EVENTS_RXPTRUPD = 0;
}
```

44.9 Pin configuration

The MCK, SCK, LRCK, SDIN and SDOUT signals associated with the I²S module are mapped to physical pins according to the pin numbers specified in the PSEL.x registers.

These pins are acquired whenever the I²S module is enabled through the register *ENABLE* on page 451.

When a pin is acquired by the I²S module, the direction of the pin (input or output) will be configured automatically, and any pin direction setting done in the GPIO module will be overridden. The directions for the various I²S pins are shown below in *Table 102: GPIO configuration before enabling peripheral (master mode)* on page 448 and *Table 103: GPIO configuration before enabling peripheral (slave mode)* on page 449.

To secure correct signal levels on the pins when the system is in OFF mode, and when the I²S module is disabled, these pins must be configured in the GPIO peripheral directly.

Table 102: GPIO configuration before enabling peripheral (master mode)

I ² S signal	I ² S pin	Direction	Output value	Comment	
MCK	As specified in PSEL.MCK	Output	0		
LRCK	As specified in PSEL.LRCK	Output	0		



I ² S signal	I ² S pin	Direction	Output value	Comment	
SCK	As specified in PSEL.SCK	Output	0		
SDIN	As specified in PSEL.SDIN	Input	Not applicable		
SDOUT	As specified in PSEL.SDOUT	Output	0		

Table 103: GPIO configuration before enabling peripheral (slave mode)

I ² S signal	I ² S pin	Direction	Output value	Comment
MCK	As specified in PSEL.MCK	Output	0	
LRCK	As specified in PSEL.LRCK	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
SDIN	As specified in PSEL.SDIN	Input	Not applicable	
SDOUT	As specified in PSEL.SDOUT	Output	0	

44.10 Registers

Table 104: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40025000	I2S	I2S	Inter-IC Sound interface		

Table 105: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous I2S transfer. Also starts MCK generator when this is enabled.
TASKS_STOP	0x004	Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the {event:STOPPED}
		event to be generated.
EVENTS_RXPTRUPD	0x104	The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started
		and RX is enabled, this event will be generated for every RXTXD.MAXCNT words that are received on
		the SDIN pin.
EVENTS_STOPPED	0x108	I2S transfer stopped.
EVENTS_TXPTRUPD	0x114	The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started
		and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the
		SDOUT pin.
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable I2S module.
CONFIG.MODE	0x504	I2S mode.
CONFIG.RXEN	0x508	Reception (RX) enable.
CONFIG.TXEN	0x50C	Transmission (TX) enable.
CONFIG.MCKEN	0x510	Master clock generator enable.
CONFIG.MCKFREQ	0x514	Master clock generator frequency.
CONFIG.RATIO	0x518	MCK / LRCK ratio.
CONFIG.SWIDTH	0x51C	Sample width.
CONFIG.ALIGN	0x520	Alignment of sample within a frame.
CONFIG.FORMAT	0x524	Frame format.
CONFIG.CHANNELS	0x528	Enable channels.
RXD.PTR	0x538	Receive buffer RAM start address.
TXD.PTR	0x540	Transmit buffer RAM start address.
RXTXD.MAXCNT	0x550	Size of RXD and TXD buffers.
PSEL.MCK	0x560	Pin select for MCK signal.
PSEL.SCK	0x564	Pin select for SCK signal.
PSEL.LRCK	0x568	Pin select for LRCK signal.
PSEL.SDIN	0x56C	Pin select for SDIN signal.
PSEL.SDOUT	0x570	Pin select for SDOUT signal.

44.10.1 INTEN

Address offset: 0x300 Enable or disable interrupt



Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F C B
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
В	RW RXPTRUPD			Enable or disable interrupt for RXPTRUPD event
				See EVENTS_RXPTRUPD
		Disabled	0	Disable
		Enabled	1	Enable
С	RW STOPPED			Enable or disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Disabled	0	Disable
		Enabled	1	Enable
F	RW TXPTRUPD			Enable or disable interrupt for TXPTRUPD event
				See EVENTS_TXPTRUPD
		Disabled	0	Disable
		Enabled	1	Enable

44.10.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31 3	30 29	9 28	27	26 2	5 24	23 2	22 21	1 20	19	18	17	16	15 :	14 :	L3 1	2 1	1 10	9	8	7	6	5 4	4 3	2	1 0
Id																										F		С	В
Res	et 0x0	0000000		0	0 0	0 0	0	0 (0 0	0	0 0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0 (0 0	0	0 0
Id	RW	Field	Value Id	Valu	ue					Des	cript	ion																	
В	RW	RXPTRUPD								Writ	te '1'	to E	nab	le i	nte	rru	pt f	or F	XPT	RUI	PD e	ven	t						
										See	EVE	NTS_	RXF	PTR	UPL)													
			Set	1						Enal	ble																		
			Disabled	0						Read	d: Di	sabl	ed																
			Enabled	1						Read	d: En	nable	ed																
С	RW	STOPPED								Writ	te '1'	to E	nab	le i	nte	rru	pt f	or S	TOP	PE	eve	ent							
										See	EVE	NTS_	STC	PP	ED														
			Set	1						Enal	ble																		
			Disabled	0						Read	d: Di	sabl	ed																
			Enabled	1						Read	d: En	nable	ed																
F	RW	TXPTRUPD								Writ	te '1'	to E	nab	le i	nte	rru	pt f	or T	XPT	RUI	D e	vent							
										See	EVE	NTS_	TXP	TR	UPL)													
			Set	1						Enal	ble																		
			Disabled	0						Read	d: Di	sabl	ed																
			Enabled	1						Read	d: En	nable	ed																

44.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		31	. 30	29	28	3 27	26	5 25	24	1 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4 3	2	1	0
Id																														F		С	В	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	alue							De	esci	ripti	on																			
В	RW	RXPTRUPD										W	rite	'1'	to [Disa	able	in	terr	up	t fo	r R>	(PTI	RUP	Dе	ven	t							
												Se	ee E	VEN	NTS_	_RX	PTI	RUI	PD															
			Clear	1								Di	sab	le																				
			Disabled	0								Re	ead	: Dis	sabl	ed																		
			Enabled	1								Re	ead	: En	able	ed																		
С	RW	STOPPED										W	rite	'1'	to [Disa	able	in	terr	up	t fo	r ST	OPI	PED	eve	ent								



Bit n	umbe	er		31	1 30 :	29	28	27	26	25 2	24 2	3 22	2 21	20	19 1	18 1	L7 1	6 1	5 1	4 13	3 12	2 11	10	9	8 7	6	5	4	3	2	1 0
Id																											F			C I	В
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 () (0	0	0	0	0	0	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue						C	esc	ripti	on																	
											S	ee E	VEN	ITS_	STO	PPE	D														
			Clear	1							C	isat	ole																		
			Disabled	0							R	lead	: Dis	able	ed																
			Enabled	1							R	lead	: Ena	able	d																
F	RW	TXPTRUPD									٧	Vrite	e '1'	to D	isab	le i	ntei	rup	t fo	r T	(PT	RUP	D ev	ent							
											S	ee E	VEN	ITS_	TXP	TRL	JPD														
			Clear	1								isat	ole																		
			Disabled	0							R	lead	: Dis	able	ed																
			Enabled	1							R	lead	: Ena	able	d																

44.10.4 ENABLE

Address offset: 0x500 Enable I2S module.

Bit	numbe	er		31 30	29	28	27	26	25 2	24 2	23 2	22 2	1 20) 19	18	17	16	15	14 1	13 1	2 11	. 10	9	8	7	6	5	4	3	2 :	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0 0
ld	RW	Field	Value Id	Value	2						Des	crip	tion																		
Α	RW	ENABLE								E	nal	ble I	2S r	nod	ule.																
			Disabled	0						[Disa	ble																			
			Enabled	1						E	nal	ble																			

44.10.5 CONFIG.MODE

Address offset: 0x504

I2S mode.

Bit num	ber		31	30	29	28	27 :	26 :	25 :	24	23	22 :	21 2	20 1	L9 1	18 1	17 1	16 :	15	14 1	13 :	12 1	11 1	0 9	9 8	3 7	' 6	5	4	3	2	1 0
Id																																Α
Reset 0	x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () () () (0	0	0	0	0	0 0
Id R\	W Field	Value Id	Va	lue							Des	crip	otio	n																		
A RV	W MODE										I2S	mo	de.																			
		Master	0								Ma	ster	r mo	ode	. SC	Ка	nd I	LRC	CK g	ene	erat	ed	fron	n in	terr	nal	mas	ter				
											clcc	k (I	MCI	<) a	nd o	out	put	on	pir	ns d	efir	ied	by F	PSE	L.xx	x.						
		Slave	1								Slav	/e n	nod	e. S	CK	and	l LR	CK	gei	nera	ite	by	ext	ern	al n	nas	ter	and				
											rec	eive	ed o	n p	ins (def	ine	d b	y P	SEL.	xxx											

44.10.6 CONFIG.RXEN

Address offset: 0x508 Reception (RX) enable.

Bit number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW RXEN		Reception (RX) enable.
Disabled	0	Reception disabled and now data will be written to the RXD.PTR
		address.
Enabled	1	Reception enabled.

44.10.7 CONFIG.TXEN

Address offset: 0x50C



Transmission (TX) enable.

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 1	7 1	5 15	5 14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0	l
Id																																	Α	l
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0 (0 (0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 1	l
Id	RW	Field	Value Id	Va	alue							Des	crip	tio	n																			l
Α	RW	TXEN										Tra	nsm	issi	on (TX)	en	able																1
			Disabled	0								Tra	nsm	issi	on o	disa	ble	d ar	d n	ow	dat	a w	ll be	re	ad 1	ron	n th	ie						
												RXE	XT.C	D a	ddr	ess.																		
			Enabled	1								Tra	nsm	issi	on e	enal	ble	d.																

44.10.8 CONFIG.MCKEN

Address offset: 0x510

Master clock generator enable.

Bit	numbe	r		3:	1 30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 1	16 1	L5 1	L4 1	3 12	2 11	. 10	9	8	7	6	5	4	3 2	2 1	L 0
Id																																	Α
Res	et 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0	1
Id	RW	Field	Value Id	V	alue	:						De	escri	ptic	on																		
Α	RW	MCKEN										M	aste	r clo	ock	gen	era	tor	ena	able	<u>.</u>												
			Disabled	0								M	aste	r clo	ock	gen	era	tor	dis	able	ed a	nd I	PSEL	MC	CK n	ot							
												со	nne	cted	d(av	/aila	ble	as	GPI	O).													
			Enabled	1								M	aste	r clo	ock	gen	era	tor	run	nin	ıg aı	nd N	ΛСК	out	put	on	PSE	L.N	1CK				

44.10.9 CONFIG.MCKFREQ

Address offset: 0x514

Master clock generator frequency.

Bitı	numb	er		3	1 30	29	28	27	26	25	24	23 2	2 21	L 20	19	18	17	16	15	14	l3 1	2 1:	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α /	4 A	Α	Α	Α	Α	Α	Α	Α	A A	4 A	Α	Α	Α	Α	Α	Α	Α	A A	A	A
Res	et 0x2	20000000		0	0	1	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	٧	alue	•						Desc	ript	ion																		
Α	RW	MCKFREQ										Mas	ter c	lock	c ge	ner	ato	r fre	equ	enc	/.											
			32MDIV2	0:	x800	0000	000					32 N	1Hz ,	/ 2 =	16	.0 N	ИHz															
			32MDIV3	0:	x500	0000	000					32 N	1Hz ,	/ 3 =	= 10	.66	666	67	МН	Z												
			32MDIV4	0:	x400	0000	000					32 N	1Hz ,	/ 4 =	8.0	M C	Hz															
			32MDIV5	0:	x300	0000	000					32 N	1Hz ,	/ 5 =	6.4	4 M	Hz															
			32MDIV6	0:	x280	0000	000					32 N	1Hz ,	/ 6 =	5.3	333	333	3 N	1Hz													
			32MDIV8	0:	x200	0000	000					32 N	1Hz ,	/ 8 =	4.0	M C	Hz															
			32MDIV10	0:	x180	0000	000					32 N	1Hz ,	/ 10	= 3	.2 N	ИHz															
			32MDIV11	0:	x160	0000	000					32 N	1Hz ,	/ 11	= 2	.90	909	09	МН	Z												
			32MDIV15	0:	x11(0000	000					32 N	1Hz ,	/ 15	= 2	.13	333	33	МН	Z												
			32MDIV16	0:	x100	0000	000					32 N	1Hz ,	/ 16	= 2	.0 N	ИHz															
			32MDIV21	0:	x0C(0000	000					32 N	1Hz ,	/ 21	= 1	.52	380	95														
			32MDIV23	0:	x0B(0000	000					32 N	1Hz ,	/ 23	= 1	.39	130	43	МН	Z												
			32MDIV30	0:	x088	3000	000					32 N	1Hz ,	/ 30	= 1	.06	666	67	МН	Z												
			32MDIV31	0:	x084	4000	000					32 N	1Hz ,	/ 31	= 1	.03	225	81	МН	Z												
			32MDIV32	0:	x080	0000	000					32 N	1Hz ,	/ 32	= 1	.0 N	ИHz															
			32MDIV42	0:	x060	0000	000					32 N	1Hz ,	/ 42	= 0	.76	190	48	МН	Z												
			32MDIV63	0:	x04:	1000	000					32 N	1Hz ,	/ 63	= 0	.50	793	65	МН	Z												
			32MDIV125	0:	x020)CO	000					32 N	1Hz ,	/ 12	5 =	0.2	56 I	ИH	Z													

44.10.10 CONFIG.RATIO

Address offset: 0x518 MCK / LRCK ratio.



Bit number	3	30 29 28 2	27 26 25 24	23 22 21	20 1	.9 18	17 10	6 15	14 13	12 1	1 10	9	8 7	6	5 4		2 1 A A	. 0
Reset 0x00000006	0	0000	0 0 0 0	0 0 0	0 (0 0	0 0	0	0 0	0 0	0	0	0 0	0	0 0	0	1 1	. 0
Id RW Field Va	alue Id V	/alue		Description	on													
A RW RATIO				MCK / LR	CK ra	itio.												
32	2X 0)		LRCK = M	CK/	32												
48	3X 1	_		LRCK = M	CK /	48												
64	1X 2	!		LRCK = M	CK/	64												
96	5X 3	}		LRCK = M	CK/	96												
12	28X 4	ļ		LRCK = M	CK/	128												
19	92X 5	;		LRCK = M	CK/	192												
25	56X 6	i		LRCK = M	CK/	256												
38	34X 7	,		LRCK = M	CK/	384												
51	12X 8	3		LRCK = M	CK/	512												

44.10.11 CONFIG.SWIDTH

Address offset: 0x51C

Sample width.

Bit n	umbe	r		31	L 30	29	28	27	26	5 25	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 .	4 3	2	1	0
Id																																	Α	Α
Rese	t 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	1
Id	RW	Field	Value Id	Va	alue							D	escr	ipti	on																			
Α	RW	SWIDTH										Sa	mp	le w	/idt	h.																		
			8Bit	0								8	bit.																					
			16Bit	1								16	bit																					
			24Bit	2								24	bit																					

44.10.12 CONFIG.ALIGN

Address offset: 0x520

Alignment of sample within a frame.

Е	it n	umb	er		31 30	29	28	3 27	26	25	24	23	22	21 2	20 1	L9 1	8 1	7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	1	0
10	ł																																Α
F	ese	t OxC	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0	0 (0	0	0
b	t	RW	Field	Value Id	Valu	е						De	scrip	otio	n																		
P		RW	ALIGN									Ali	gnm	ent	of	sam	ple	wit	hin	a fr	ame	e.											
				Left	0							Lef	t-ali	gne	d.																		
				Right	1							Rig	ht-a	ligr	ied.																		

44.10.13 CONFIG.FORMAT

Address offset: 0x524

Frame format.

Bit	num	ber			31 3	0 29	9 28	8 27	7 26	5 25	24	23	22	21	20	19	18	17	16	15 :	14 :	13 1	L2 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id																																	Α
Res	et O	x00	000000		0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RV	N	Field	Value Id	Valu	e						De	scri	ipti	on																		
Α	RV	Ν	FORMAT									Fra	ame	e fo	rma	it.																	
				125	0							Or	igin	al I	2S f	orm	nat.																
				Aligned	1							Alt	tern	ate	(le	ft- c	or ri	ght	-alię	gne	d) f	orm	ıat.										

44.10.14 CONFIG.CHANNELS

Address offset: 0x528 Enable channels.



Bit	nur	mbe	r		3	1 30	29	28	8 27	7 20	6 25	5 2	4 2	3 2	2 21	L 20	19	18	17	16	15	14	13	12	11 1	.0	9 .	8	7	6	5	4	3 2	2 1	L 0
Id																																		Δ	A A
Re	set	0x0	0000000		0	0	0	0	0	0	0	0) (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()	0	0	0	0 (0	0
Id	F	RW	Field	Value Id	٧	alue	9						C	esc	ript	ion																			
Α	F	RW	CHANNELS										Е	nab	le c	han	nel	S.																	
				Stereo	0								S	tere	o.																				
				Left	1								L	eft (only	٠.																			
				Right	2								R	Right	on	ly.																			

44.10.15 RXD.PTR

Address offset: 0x538

Receive buffer RAM start address.

Bit	numb	er		31	. 30	29	9 28	8 2	7 2	26 2	25 :	24	23 :	22 :	21 :	20 :	19	18 1	.7 1	6 1	5 1	4 1	3 12	2 11	. 10	9	8	7	6	5	4	3	2	1 (
Id				Α	Α	Α	. 4	Α Α	Δ.	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ,	A A	۱ ۸	A A	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A.	A A
Res	et 0x	00000000		0	0	0	0) (0	0	0	0	0	0	0	0	0	0 (0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue								Des	crip	otio	n																		
Α	RW	PTR											Rec	eiv	e bı	ıffe	r D	ata	RAI	∕l st	art	ado	dres	s. W	/her	n re	ceiv	/ing	, w	ord	s			
													con	tair	ning	sa	mp	les v	vill	be v	vrit	ten	to 1	his	add	Ires	s. T	his	ado	ires	SS			
												i	s a	wο	rd a	aliøi	ned	Dat	ta R	ΔΙΛ	ad	dre	cc											

44.10.16 TXD.PTR

Address offset: 0x540

Transmit buffer RAM start address.

Bitı	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21 2	20 1	9 18	3 17	16	15	14	13 1	2 1:	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	A A	A	Α	Α	Α	Α	A	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptio	n																	
Α	RW	PTR										Tra	nsn	nit b	uffe	r Da	ıta F	RAN	1 sta	art a	ddr	ess.	Wh	en ti	ran	smi	ttin	ıg,				
												wo	rds	con	taini	ing s	am	ples	wi	ll be	feto	ched	l fro	m tł	nis a	addı	res	s. T	his			
												ado	dres	s is	a wo	ord a	aligr	ned	Dat	a R	AM a	addr	ess.									

44.10.17 RXTXD.MAXCNT

Address offset: 0x550

Size of RXD and TXD buffers.

Reset 0x000000000	00000	0 0
	0 0 0 0 0	0 0
Id A A A A A A		
		A A
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7	6 5 4 3 2	1 0

44.10.18 PSEL.MCK

Address offset: 0x560 Pin select for MCK signal.

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ААААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect



44.10.19 PSEL.SCK

Address offset: 0x564 Pin select for SCK signal.

Bit r	numbe	er		31	30	29	28 2	27 2	26 2	25 2	24 2	3 2	2 2:	1 20	0 19	9 1	3 17	16	15	14	13 1	2 1	1 10	9	8	7	6	5 4	4 3	3 2	1	0
Id				С																								,	A A	A A	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1 :	1 1	L 1	L 1	. 1	. 1	1	. 1	1	1	1	1	1 1	l 1	1	1	1	1	1	1 :	l 1	1	1
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion	1																	
Α	RW	PIN		[0.	.31]						Р	in r	num	ber																		
С	RW	CONNECT									С	onr	nect	ion																		
			Disconnected	1							D	isco	onn	ect																		
			Connected	0							С	onr	nect																			

44.10.20 PSEL.LRCK

Address offset: 0x568

Pin select for LRCK signal.

31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
С	АААА
1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Value	Description
[031]	Pin number
	Connection
1	Disconnect
0	Connect
	C 1 1 1 1 1 1 1 1 1 1 Value [031]

44.10.21 PSEL.SDIN

Address offset: 0x56C

Pin select for SDIN signal.

Bit	numbe	er		31 30 29 28 27 26 25 2	$24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id				С	A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

44.10.22 PSEL.SDOUT

Address offset: 0x570

Pin select for SDOUT signal.

Bit	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect



44.11 Electrical Specification

44.11.1 I2S timing specification

Symbol	Description	Min.	Тур.	Max.	Units
t_{S_SDIN}	SDIN setup time before SCK rising	20			ns
t _{H_SDIN}	SDIN hold time after SCK rising	15			ns
t _{S_SDOUT}	SDOUT setup time after SCK falling	40			ns
t _{H_SDOUT}	SDOUT hold time before SCK falling	6			ns
t _{SCK_LRCK}	SCLK falling to LRCK edge	-5	0	5	ns
f_{MCK}	MCK frequency			4000	kHz
f_{LRCK}	LRCK frequency			48	kHz
f_{SCK}	SCK frequency			2000	kHz
DC _{CK}	Clock duty cycle (MCK, LRCK, SCK)	45		55	%

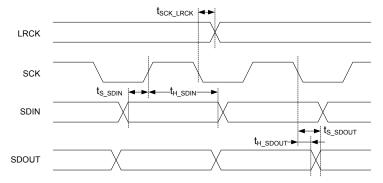


Figure 139: I2S timing diagram



45 MWU — Memory watch unit

The Memory watch unit (MWU) can be used to generate events when a memory region is accessed by the CPU. The MWU can be configured to trigger events for access to Data RAM and Peripheral memory segments. The MWU allows an application developer to generate memory access events during development for debugging or during production execution for failure detection and recovery.

Listed here are the main features for MWU:

- · Six memory regions, four user-configurable and two fixed regions in peripheral address space
- Flexible configuration of regions with START and END addresses
- Generate events on CPU read and/or write to a defined region of Data RAM or peripheral memory address space
- Programmable maskable or non-maskable (NMI) interrupt on events
- Peripheral interfaces can be watched for read and write access using subregions of the two fixed memory regions

Table 106: Memory regions

Memory region	START address	END address
REGION[03]	Configurable	Configurable
PREGION[0]	0x4000000	0x4001FFFF
PREGION[1]	0x40020000	0x4003FFFF

Each MWU region is defined by a start address and an end address, configured by the START and END registers respectively. These addresses are byte aligned and inclusive. The END register value has to be greater or equal to the START register value. Each region is associated with a pair of events that indicate that either a write access or a read access from the CPU has been detected inside the region.

For regions containing subregions (see below), a set of status registers PERREGION[0..1].SUBSTATWA and PERREGION[0..1].SUBSTATRA indicate which subregion(s) caused the EVENT_PREGION[0..1].WA and EVENT_PREGION[0..1].RA respectively.

The MWU is only able to detect memory accesses in the Data RAM and Peripheral memory segments from the CPU, see *Memory* on page 20 for more information about the different memory segments. EasyDMA accesses are not monitored by the MWU. The MWU requires two HCLK cycles to detect and generate the event.

The peripheral regions, PREGION[0...1], are divided into 32 equally sized subregions, SR[0...31]. All subregions are excluded in the main region by default, and any can be included by specifying them in the SUBS register. When a subregion is excluded from the main region, the memory watch mechanism will not trigger any events when that subregion is accessed.

Subregions in PREGION[0..1] cannot be individually configured for read or write access watch. Watch configuration is only possible for a region as a whole. The PRGNiRA and PRGNiWA (i=0..1) fields in the REGIONEN register control watching read and write access.

REGION[0..3] can be individually enabled for read and/or write access watching through their respective RGNiRA and RGNiWA (i=0..3) fields in the REGIONEN register.

REGIONENSET and REGIONENCLR allow respectively enabling and disabling one or multiple REGIONs or PREGIONs watching in a single write access.

45.1 Registers

Table 107: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40020000	MWU	MWU	Memory Watch Unit	



Table 108: Register Overview

Register	Offset	Description
EVENTS_REGION[0].W	A 0x100	Write access to region 0 detected
EVENTS_REGION[0].RA	0x104	Read access to region 0 detected
EVENTS_REGION[1].W	A 0x108	Write access to region 1 detected
EVENTS_REGION[1].RA	0x10C	Read access to region 1 detected
EVENTS_REGION[2].W	A 0x110	Write access to region 2 detected
EVENTS_REGION[2].RA	0x114	Read access to region 2 detected
EVENTS_REGION[3].W	A 0x118	Write access to region 3 detected
EVENTS_REGION[3].RA	0x11C	Read access to region 3 detected
EVENTS_PREGION[0].V	VA 0x160	Write access to peripheral region 0 detected
EVENTS_PREGION[0].R	A 0x164	Read access to peripheral region 0 detected
EVENTS_PREGION[1].V	VA 0x168	Write access to peripheral region 1 detected
EVENTS_PREGION[1].R	A 0x16C	Read access to peripheral region 1 detected
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
NMIEN	0x320	Enable or disable non-maskable interrupt
NMIENSET	0x324	Enable non-maskable interrupt
NMIENCLR	0x328	Disable non-maskable interrupt
PERREGION[0].SUBSTA	71 0x400	Source of event/interrupt in region 0, write access detected while corresponding subregion was
		enabled for watching
PERREGION[0].SUBSTA	TI 0x404	Source of event/interrupt in region 0, read access detected while corresponding subregion was
		enabled for watching
PERREGION[1].SUBSTA	71 0x408	Source of event/interrupt in region 1, write access detected while corresponding subregion was
		enabled for watching
PERREGION[1].SUBSTA	77 0x40C	Source of event/interrupt in region 1, read access detected while corresponding subregion was
		enabled for watching
REGIONEN	0x510	Enable/disable regions watch
REGIONENSET	0x514	Enable regions watch
REGIONENCLR	0x518	Disable regions watch
REGION[0].START	0x600	Start address for region 0
REGION[0].END	0x604	End address of region 0
REGION[1].START	0x610	Start address for region 1
REGION[1].END	0x614	End address of region 1
REGION[2].START	0x620	Start address for region 2
REGION[2].END	0x624	End address of region 2
REGION[3].START	0x630	Start address for region 3
REGION[3].END	0x634	End address of region 3
PREGION[0].START	0x6C0	Reserved for future use
PREGION[0].END	0x6C4	Reserved for future use
PREGION[0].SUBS	0x6C8	Subregions of region 0
PREGION[1].START	0x6D0	Reserved for future use
PREGION[1].END	0x6D4	Reserved for future use
PREGION[1].SUBS	0x6D8	Subregions of region 1

45.1.1 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	numbe	er		31	1 30	29	9 28	8 27	26	5 25	24	1 23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id								L	K	J	-1																Н	G	F	Ε	D	С	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	•						De	scr	ipti	on																		
Α	RW	REGION0WA										En	abl	e oı	dis	sabl	e ii	nter	rup	t fo	r R	EGI]NC	0].V	/A e	ven	t						
												Se	e <i>E</i>	VΕN	ITS_	_RE	GIC	ON[(0].V	VA													
			Disabled	0								Di	sab	le																			



Bit n	umbe	er		31 30	29 28	27 2	6 2	5 24	23 22 21	1 20 19	18 17	16	15 1	4 13	12 :	11 10) 9	8	7	6 5	4	3	2 1	0
Id						LI															Е			
Rese	t 0x0	0000000		0 0	0 0	0 (0 (0	0 0 0	0 0	0 0	0	0	0 0	0	0 0	0	0	0	0 0	0	0	0 0	0
Id	RW	Field	Value Id	Value					Descript	ion														
			Enabled	1					Enable															
В	RW	REGIONORA							Enable o	r disabl	e inte	rrup	t for	REGI	ON[0].RA	eve	ent						
									See <i>EVEI</i>	NTS RE	GION[0].R.	A											
			Disabled	0					Disable	_														
			Enabled	1					Enable															
С	RW	REGION1WA							Enable o	r disabl	e inte	rrup	t for	REGI	ON[1].W	A ev	ent						
									See <i>EVEI</i>	NTS RE	GIONÍ	11. W	/A											
			Disabled	0					Disable	_		1												
			Enabled	1					Enable															
D	RW	REGION1RA							Enable o	r disabl	e inte	rrup	t for	REGI	ON[1].RA	eve	ent						
									See <i>EVEI</i>	NTS RF	GIONI	11 R	Δ											
			Disabled	0					Disable	*13_11E	O/O/V _[
			Enabled	1					Enable															
E	RW	REGION2WA							Enable o	r disabl	e inte	rrup	t for	REGI	ON[2].W	A ev	ent						
									See <i>EVEI</i>	NTS RF	GIONI	21 M	/Δ											
			Disabled	0					Disable	*13_11E	O/O/V _L													
			Enabled	1					Enable															
F	RW	REGION2RA							Enable o	r disabl	e inte	rrup	t for	REGI	ON[2].RA	eve	ent						
									See <i>EVEI</i>	NTS RF	GIONI	21 R	Δ											
			Disabled	0					Disable	*13_11E	0,0,4													
			Enabled	1					Enable															
G	RW	REGION3WA							Enable o	r disabl	e inte	rrup	t for	REGI	ON[3].W	A ev	ent						
									See <i>EVEI</i>	NTS RF	GIONÍ	31 M	/Δ											
			Disabled	0					Disable	*13_11E	0,0,1	٥,.٠١												
			Enabled	1					Enable															
Н	RW	REGION3RA							Enable o	r disabl	e inte	rrup	t for	REGI	ON[3].RA	eve	ent						
									See <i>EVEI</i>	NTS RF	GIONÍ	31 R	4											
			Disabled	0					Disable		0.0	J	•											
			Enabled	1					Enable															
ı	RW	PREGIONOWA							Enable o	r disabl	e inte	rrup	t for	PREC	SION	[0].V	VA e	vent	t					
									See <i>EVEI</i>	NTS PR	FGION	IFO1.	WA											
			Disabled	0					Disable			1-1-												
			Enabled	1					Enable															
J	RW	PREGIONORA							Enable o	r disabl	e inte	rrup	t for	PREC	SION	[0].R	A ev	<i>y</i> ent						
									See <i>EVEI</i>	NTS PR	FGION	IFO1.	RA											
			Disabled	0					Disable			1-1-												
			Enabled	1					Enable															
K	RW	PREGION1WA							Enable o	r disabl	e inte	rrup	t for	PREC	SION	[1].V	VA e	ven	t					
									See <i>EVEI</i>	NTS PR	EGION	l[1]	WA											
			Disabled	0					Disable			2 91												
			Enabled	1					Enable															
L	RW	PREGION1RA							Enable o	r disabl	e inte	rrup	t for	PREC	SION	[1].R	A ev	<i>e</i> nt						
									See <i>EVEI</i>	NTS PR	EGION	I[11	RA											
			Disabled	0					Disable			, .												
			Enabled	1					Enable															

45.1.2 INTENSET

Address offset: 0x304 Enable interrupt



Bit r	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K	J I H G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW REGIONOWA			Write '1' to Enable interrupt for REGION[0].WA event
				See EVENTS_REGION[0].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REGIONORA			Write '1' to Enable interrupt for REGION[0].RA event
				See EVENTS_REGION[0].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW REGION1WA			Write '1' to Enable interrupt for REGION[1].WA event
				See EVENTS_REGION[1].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW REGION1RA			Write '1' to Enable interrupt for REGION[1].RA event
				See EVENTS_REGION[1].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW REGION2WA			Write '1' to Enable interrupt for REGION[2].WA event
				See EVENTS_REGION[2].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW REGION2RA			Write '1' to Enable interrupt for REGION[2].RA event
				See EVENTS_REGION[2].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW REGION3WA		_	Write '1' to Enable interrupt for REGION[3].WA event
		Cot	1	See EVENTS_REGION[3].WA Enable
		Set Disabled	1 0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW REGION3RA	Enablea	-	Write '1' to Enable interrupt for REGION[3].RA event
		Sot	1	See EVENTS_REGION[3].RA
		Set Disabled	1 0	Enable Read: Disabled
		Enabled	1	Read: Disabled
	RW PREGIONOWA	Litablea	•	Write '1' to Enable interrupt for PREGION[0].WA event
•				,
		Cat	1	See EVENTS_PREGION[0].WA
		Set	1	Enable Read: Disabled
		Disabled Enabled	0 1	Read: Disabled Read: Enabled
	RW PREGIONORA	Liiableu	1	Write '1' to Enable interrupt for PREGION[0].RA event
	TREGIONORA			
				See EVENTS_PREGION[0].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
V	DW DDECIGALANA	Enabled	1	Read: Enabled
K	RW PREGION1WA			Write '1' to Enable interrupt for PREGION[1].WA event



Bit r	numbe	er		31	. 30	29 :	28 2	7 2	26 2	5 2	24 2	23 2	2 2	21 20	0 1	9 1	3 17	7 16	5 15	5 14	1 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id								L	Κ.	J	L																Н	G	F	Ε	D C	В	Α
Res	et OxO	0000000		0	0	0	0 (0	0 ()	0	0 (0 (0 0) (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Desc	crip	tion	1																		
											9	See I	EVE	ENTS	S_ <i>P</i>	REC	101	V[1]	.w	Α													
			Set	1							E	Enab	ole																				
			Disabled	0							F	Reac	d: D	isab	oled	t																	
			Enabled	1							F	Reac	d: E	nab	led																		
L	RW	PREGION1RA									١	Writ	e '1	1' to	En	able	int	terr	upt	for	PR	EGI	ON[1].R	Αe	ven	t						
											9	See I	EVE	ENTS	S_ <i>P</i>	REC	101	V[1]	.RA	١													
			Set	1							E	Enab	ole																				
			Disabled	0							F	Read	d: D	isab	olec	t																	
			Enabled	1							F	Read	d: E	nab	led																		

45.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number			26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d			K J I H G F E D C B A
Reset 0x00000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
d RW Field	Value Id	Value	Description
A RW REGIONOWA			Write '1' to Disable interrupt for REGION[0].WA event
			See EVENTS_REGION[0].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGIONORA			Write '1' to Disable interrupt for REGION[0].RA event
			See EVENTS_REGION[0].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGION1WA			Write '1' to Disable interrupt for REGION[1].WA event
			See EVENTS_REGION[1].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW REGION1RA	Lilabica	-	Write '1' to Disable interrupt for REGION[1].RA event
			See EVENTS_REGION[1].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
DIAL DECIONIZIALA	Enabled	1	Read: Enabled
RW REGION2WA			Write '1' to Disable interrupt for REGION[2].WA event
			See EVENTS_REGION[2].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGION2RA			Write '1' to Disable interrupt for REGION[2].RA event
			See EVENTS_REGION[2].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
RW REGION3WA			Write '1' to Disable interrupt for REGION[3].WA event
			See EVENTS_REGION[3].WA
	Clear	1	Disable



Bitı	number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K J I	HGFEDCBA
Res	set 0x00000000		0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field Va	alue Id	Value	Description
	Di	isabled	0	Read: Disabled
	En	nabled	1	Read: Enabled
Н	RW REGION3RA			Write '1' to Disable interrupt for REGION[3].RA event
				See EVENTS_REGION[3].RA
	Cle	lear	1	Disable
	Di	isabled	0	Read: Disabled
	En	nabled	1	Read: Enabled
I	RW PREGIONOWA			Write '1' to Disable interrupt for PREGION[0].WA event
				See EVENTS_PREGION[0].WA
	Cle	ear	1	Disable
	Di	isabled	0	Read: Disabled
	En	nabled	1	Read: Enabled
J	RW PREGIONORA			Write '1' to Disable interrupt for PREGION[0].RA event
				See EVENTS_PREGION[0].RA
	Cle	ear	1	Disable
	Di	isabled	0	Read: Disabled
	En	nabled	1	Read: Enabled
K	RW PREGION1WA			Write '1' to Disable interrupt for PREGION[1].WA event
				See EVENTS_PREGION[1].WA
	Cle	ear	1	Disable
	Di	isabled	0	Read: Disabled
	En	nabled	1	Read: Enabled
L	RW PREGION1RA			Write '1' to Disable interrupt for PREGION[1].RA event
				See EVENTS_PREGION[1].RA
	Cle	ear		Disable
	Di	isabled	0	Read: Disabled
	En	nabled	1	Read: Enabled

45.1.4 NMIEN

Address offset: 0x320

Enable or disable non-maskable interrupt

Bitı	numbe	er		31 30	29	28 2	7 2	6 25	24	23 2	22 21	20	19 1	L8 1	7 16	5 15	14	13 1	.2 1	1 10	9	8	7 6	5 5	5 4	3	2	1 0
Id						l	L k	J	1														Н	G F	E	D	С	ВА
Res	et 0x0	0000000		0 0	0	0 (0	0	0	0 (0 0	0	0	0 (0 0	0	0	0	0 0	0	0	0	0 0) (0	0	0	0 0
Id	RW	Field	Value Id	Value	е					Desc	cripti	ion																
Α	RW	REGION0WA								Enab	ble o	r dis	able	no	n-ma	aska	ble	inte	rup	t for	REC	1016	١[0].	WΑ	١			
										ever	nt																	
										See	EVEN	VTS_	REG	ION	I[0].	WA												
			Disabled	0						Disa	able																	
			Enabled	1						Enab	ble																	
В	RW	REGIONORA								Enab	ble o	r dis	able	no	n-ma	aska	ble	inte	rup	t for	REC	1016	١[0].	RA				
										ever	nt																	
										See	EVEN	VTS_	REG	ION	I[0].I	RA												
			Disabled	0						Disa	able																	
			Enabled	1						Enab	ble																	
С	RW	REGION1WA								Enab	ble o	r dis	able	no	n-ma	aska	ble	inte	rup	t for	REC	1016	N[1].	WA				
										ever	nt																	
										See	EVEN	VTS_	REG	ION	I[1].	WA												
			Disabled	0						Disa	able																	
			Enabled	1						Enab	ble																	



Bit	numbe	er		31 30	29 28	27	26 25	24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id							K J		H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
D	RW	REGION1RA							Enable or disable non-maskable interrupt for REGION[1].RA event See EVENTS_REGION[1].RA
			Disabled	0					Disable
			Enabled	1					Enable
Е	RW	REGION2WA							Enable or disable non-maskable interrupt for REGION[2].WA event
			Disabled	0					See EVENTS_REGION[2].WA
			Disabled Enabled	0					Disable
F	D\A/	REGION2RA	Enabled	1					Enable Enable or disable non markable interrupt for RECION[3] RA
r	NVV	REGIONZRA							Enable or disable non-maskable interrupt for REGION[2].RA event
			5. 11.1						See EVENTS_REGION[2].RA
			Disabled Enabled	0					Disable
G	D\A/	REGION3WA	Enabled	1					Enable Enable or disable non-maskable interrupt for REGION[3].WA
d	NVV	REGIONSWA							event
									See EVENTS_REGION[3].WA
			Disabled	0					Disable
		2501011024	Enabled	1					Enable
Н	KW	REGION3RA							Enable or disable non-maskable interrupt for REGION[3].RA event
									See EVENTS_REGION[3].RA
			Disabled	0					Disable
			Enabled	1					Enable
ı	RW	PREGIONOWA							Enable or disable non-maskable interrupt for PREGION[0].WA event
									See EVENTS_PREGION[0].WA
			Disabled	0					Disable
			Enabled	1					Enable
J	RW	PREGIONORA							Enable or disable non-maskable interrupt for PREGION[0].RA event
									See EVENTS_PREGION[0].RA
			Disabled	0					Disable
			Enabled	1					Enable
K	RW	PREGION1WA							Enable or disable non-maskable interrupt for PREGION[1].WA event
									See EVENTS_PREGION[1].WA
			Disabled	0					Disable
			Enabled	1					Enable
L	RW	PREGION1RA							Enable or disable non-maskable interrupt for PREGION[1].RA event
									See EVENTS_PREGION[1].RA
			Disabled	0					Disable
			Enabled	1					Enable

45.1.5 NMIENSET

Address offset: 0x324

Enable non-maskable interrupt



New Marco	Bitı	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
No. Fed Value	Id			LKJI	H G F E D C B A
Write "1" to Enable non-maskable interrupt for REGION[0], WA event	Res			0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Set	Id		Value Id	Value	
See EVENTS_REGION(S), WA	Α	RW REGIONOWA			
Set					event
Disabled Enabled Final					
Enabled 1					
Write '1' to Enable non-maskable interrupt for REGION(0).RA					
Set	В	RW REGIONORA	Lilabieu	1	
Set		neo.o			
Set					Con EVENTS DECIONIOLDA
Disabled Carabled			Sat	1	
Enabled 1					
Write '1' to Enable non-maskable interrupt for REGION[3].WA event					
Set	С	RW REGION1WA		_	
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled D RW REGIONIRA Finable Set 1 Enable Disabled 0 Read: Disabled Set 1 Enable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[1],RA event See EVENTS, REGION[1],RA Enable E RW REGION2WA Finable 1 Read: Enabled Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Finable 0 Read: Disabled Enabled 1 Read: Enabled Finable 0 Read: Disabled Enabled 1 Read: Enabled See EVENTS, REGION[2],WA EVENT See EVENTS, REGION[2],RA EVENT See EVENTS, REGION[3],RA EVENT See EVENTS, REGION[3],RA EVENT See EVENTS, REGION[3],WA EVENT See EVENTS, REGION[3],RA EVENT SEE EVENTS REGION[3],RA EVENT SE					
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled D RW REGIONIRA Finable Set 1 Enable Disabled 0 Read: Disabled Set 1 Enable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[1],RA event See EVENTS, REGION[1],RA Enable E RW REGION2WA Finable 1 Read: Enabled Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Finable 0 Read: Disabled Enabled 1 Read: Enabled Finable 0 Read: Disabled Enabled 1 Read: Enabled See EVENTS, REGION[2],WA EVENT See EVENTS, REGION[2],RA EVENT See EVENTS, REGION[3],RA EVENT See EVENTS, REGION[3],RA EVENT See EVENTS, REGION[3],WA EVENT See EVENTS, REGION[3],RA EVENT SEE EVENTS REGION[3],RA EVENT SE					Son EVENTS RECION[1] WA
Disabled 0 Read: Disabled Read: Chabled Read: Disabled Read: Di			Sat	1	
Enabled 1					
Write '1' to Enable non-maskable interrupt for REGION[1].RA event See EVENTS_REGION[1].RA Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Enabled 1 Read: Enabled Enabled 0 Read: Enabled Enabled 0 Read: Enabled Enabled 1 Read: Enabled See EVENTS_REGION[2].WA event See EVENTS_REGION[2].WA Enable Enabled 1 Read: Enabled Enabled 1 Read: Enabled Enabled 1 Read: Enabled FRW REGION2RA Set 1 Enable See EVENTS_REGION[2].RA event See EVENTS_REGION[2].RA Event See EVENTS_REGION[3].RA Event See EVENTS_REGION[3].RA Event See EVENTS_REGION[3].RA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].RA Even					
Set 1 Chable FRW REGIONZWA FRW REGIONZWA Set 1 Chable Enable FRW REGIONZWA Set 1 Chable Frable	D	RW REGION1RA			Write '1' to Enable non-maskable interrupt for REGION[1].RA
Set					
Set					See FVFNTS REGION[1] RA
Disabled Disabled Disabled Read: Disabled Read: Enabled Read: Enabled Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[2].WA event			Set	1	
RW REGION2WA REGION2WA Write '1' to Enable non-maskable interrupt for REGION[2].WA event See EVENTS_REGION[2],WA Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[2].RA event See EVENTS_REGION[2],RA ENA ENA ENA ENA ENA ENA ENA ENA ENA E					
event See EVENTS_REGION[2]_WA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled FRW REGION2RA Set 1 Enable See EVENTS_REGION[2]_RA event See EVENTS_REGION[2]_RA event See EVENTS_REGION[2]_RA Set 1 Enabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[2]_RA event See EVENTS_REGION[2]_RA Set 1 Enabled Write '1' to Enable non-maskable interrupt for REGION[3]_WA event See EVENTS_REGION[3]_WA Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3]_RA event Write '1' to Enable non-maskable interrupt for REGION[3]_RA event See EVENTS_REGION[3]_RA Enabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3]_RA event Write '1' to Enable non-maskable interrupt for REGION[3]_RA event See EVENTS_REGION[3]_RA Enable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for PREGION[0]_WA event Write '1' to Enable non-maskable interrupt for PREGION[0]_WA event			Enabled	1	Read: Enabled
See EVENTS_REGION[2].WA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[2].RA event See EVENTS_REGION[2].RA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA event See EVENTS_REGION[3].WA Enable Set 1 Read: Enabled Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA event Write '1' to Enable non-maskable interrupt for REGION[3].WA Enabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA event Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Enabled Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[0].WA event Write '1' to Enable non-maskable interrupt for PREGION[0].WA event Write '1' to Enable non-maskable interrupt for PREGION[0].WA event	E	RW REGION2WA			Write '1' to Enable non-maskable interrupt for REGION[2].WA
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled FRW REGION2RA FRW REGION2RA Set 1 Enable Disabled 0 Read: Enabled See EVENTS_REGION[2].RA event See EVENTS_REGION[2].RA Enable Enable 1 Read: Enabled Frame REGION3WA Frame REGION3WA Frame REGION3WA Set 1 Enable See EVENTS_REGION[3].WA event See EVENTS_REGION[3].WA event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event Frame PREGION[3].RA Event See EVENTS_REGION[3].RA Event Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Event Frame '1' to Enable non-maskable interrupt for REGION[3].RA Event See EVENTS_REGION[3].RA Event Frame '1' to Enable non-maskable interrupt for PREGION[0].WA Event Frame PREGIONOWA Enabled 1 Read: Enabled Frame PREGION[0].WA Event Write '1' to Enable non-maskable interrupt for PREGION[0].WA Event Frame Precion(0].WA Event					event
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled FRW REGION2RA FRW REGION2RA Set 1 Enable Disabled 0 Read: Enabled See EVENTS_REGION[2].RA event See EVENTS_REGION[2].RA Enable Enable 1 Read: Enabled Frame REGION3WA Frame REGION3WA Frame REGION3WA Set 1 Enable See EVENTS_REGION[3].WA event See EVENTS_REGION[3].WA event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event See EVENTS_REGION[3].WA Event Frame PREGION[3].RA Event See EVENTS_REGION[3].RA Event Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Event Frame '1' to Enable non-maskable interrupt for REGION[3].RA Event See EVENTS_REGION[3].RA Event Frame '1' to Enable non-maskable interrupt for PREGION[0].WA Event Frame PREGIONOWA Enabled 1 Read: Enabled Frame PREGION[0].WA Event Write '1' to Enable non-maskable interrupt for PREGION[0].WA Event Frame Precion(0].WA Event					See EVENTS REGION[2].WA
Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[2].RA event See EVENTS_REGION[2].RA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA event See EVENTS_REGION[3].WA Set 1 Enable See EVENTS_REGION[3].WA See EVENTS_REGION[3].WA See EVENTS_REGION[3].WA Enable Disabled 0 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Event Write '1' to Enabled Enabled Enabled The Read: Enabled Write '1' to Enable non-maskable interrupt for PREGION[0].WA Event RW PREGIONOWA Event Write '1' to Enable non-maskable interrupt for PREGION[0].WA Event			Set	1	
Write '1' to Enable non-maskable interrupt for REGION[2].RA event See EVENTS_REGION[2].RA Enable Disabled Disabled Enabled Disabled Dis			Disabled	0	Read: Disabled
event See EVENTS_REGION[2],RA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA event See EVENTS_REGION[3], WA Enabled 0 Read: Disabled Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3], WA Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3], RA Enable RW PREGIONOWA RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0], WA event			Enabled	1	Read: Enabled
See EVENTS_REGION[2].RA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Read: Enabled Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA event See EVENTS_REGION[3].WA Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA ENTERION SRA Write '1' to Enable non-maskable interrupt for REGION[3].RA event RW PREGIONOWA Write '1' to Enabled Read: Enabled Write '1' to Enable non-maskable interrupt for PREGION[0].WA event	F	RW REGION2RA			Write '1' to Enable non-maskable interrupt for REGION[2].RA
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA event See EVENTS_REGION[3].WA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA event See EVENTS_REGION[3].WA Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA event See EVENTS_REGION[3].RA event RW PREGIONOWA Write '1' to Enable non-maskable interrupt for REGION[3].RA event Write '1' to Enabled Read: Enabled RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event					event
Disabled Disabled 1 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA event See EVENTS_REGION[3].WA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Enable Set 1 Enable Disabled 0 Read: Disabled Enable Read: Disabled Read: Disabled Enable Read: Disabled Enabled Read: Enabled Read: Enabled Read: Enabled Read: Disabled Enabled Read: Disabled Enabled Read: Disabled Enabled Read: Enabled Read: Enabled Read: Enabled Read: Enabled Read: Enabled Read: Disabled Enabled Read: Disabled Enabled Read: E					See EVENTS_REGION[2].RA
Enabled Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA event See EVENTS_REGION[3].WA Set Disabled Disabled Enabled Enabled Write '1' to Enable non-maskable interrupt for REGION[3].WA Enable Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Enable Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Enable Read: Disabled Enable Read: Disabled Enable Write '1' to Enable non-maskable interrupt for PREGION[0].WA event RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event			Set	1	Enable
Write '1' to Enable non-maskable interrupt for REGION[3].WA event See EVENTS_REGION[3].WA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Event See EVENTS_REGION[3].RA Event See EVENTS_REGION[3].RA Event See EVENTS_REGION[3].RA Event See EVENTS_REGION[3].RA Event Write '1' to Enable Read: Disabled Enabled Write '1' to Enable non-maskable interrupt for PREGION[0].WA event			Disabled	0	Read: Disabled
event See EVENTS_REGION[3].WA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Event See EVENTS_REGION[3].RA Event See EVENTS_REGION[3].RA Event Write '1' to Enable Write '1' to Enable Write '1' to Enabled Write '1' to Enabled Write '1' to Enabled Write '1' to Enabled Write '1' to Enable non-maskable interrupt for PREGION[0].WA event			Enabled	1	Read: Enabled
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled H RW REGION3RA Set 1 Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Enable See EVENTS_REGION[3].RA Enable Read: Enabled Finable Read: Disabled Read: Disabled Read: Disabled Enabled RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event	G	RW REGION3WA			Write '1' to Enable non-maskable interrupt for REGION[3].WA
Set 1 Read: Disabled 0 Read: Disabled 1 Read: Enabled 1 Read:					event
Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event					See EVENTS_REGION[3].WA
Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Enable Disabled Disabled Enabled 1 Read: Enabled Write '1' to Enable non-maskable interrupt for PREGION[0].WA event Write '1' to Enable non-maskable interrupt for PREGION[0].WA event			Set	1	Enable
Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Enable Disabled Disabled Enabled RW PREGIONOWA Write '1' to Enable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA Enable Read: Disabled Write '1' to Enabled Write '1' to Enable non-maskable interrupt for PREGION[0].WA event			Disabled	0	Read: Disabled
event See EVENTS_REGION[3].RA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event			Enabled	1	Read: Enabled
See EVENTS_REGION[3].RA Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event	Н	RW REGION3RA			
Set 1 Enable Disabled 0 Read: Disabled Enabled 1 Read: Enabled RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event					event
Disabled 0 Read: Disabled Enabled 1 Read: Enabled RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event					See EVENTS_REGION[3].RA
Enabled 1 Read: Enabled RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event			Set	1	Enable
RW PREGIONOWA Write '1' to Enable non-maskable interrupt for PREGION[0].WA event					
event			Enabled	1	
	I	RW PREGIONOWA			
See EVENTS_PREGION[0].WA					event
					See EVENTS_PREGION[0].WA



Bit number	•		31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L	K J I	H G F E D C B A
Reset 0x00	000000		0 0 0 0 0	0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
ld RW	Field	Value Id	Value		Description
		Set	1		Enable
		Disabled	0		Read: Disabled
		Enabled	1		Read: Enabled
J RW	PREGIONORA				Write '1' to Enable non-maskable interrupt for PREGION[0].RA
					event
					See EVENTS_PREGION[0].RA
		Set	1		Enable
		Disabled	0		Read: Disabled
		Enabled	1		Read: Enabled
K RW	PREGION1WA				Write '1' to Enable non-maskable interrupt for PREGION[1].WA
					event
					See EVENTS_PREGION[1].WA
		Set	1		Enable
		Disabled	0		Read: Disabled
		Enabled	1		Read: Enabled
L RW	PREGION1RA				Write '1' to Enable non-maskable interrupt for PREGION[1].RA
					event
					See EVENTS PREGION[1].RA
		Set	1		Enable
		Disabled	0		Read: Disabled
		Enabled	1		Read: Enabled

45.1.6 NMIENCLR

Address offset: 0x328

Disable non-maskable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW REGIONOWA		Write '1' to Disable non-maskable interrupt for REGION[0].WA event
	Clear Disabled Enabled	See EVENTS_REGION[0].WA
B RW REGIONORA	2.165.03	Write '1' to Disable non-maskable interrupt for REGION[0].RA event See EVENTS_REGION[0].RA
	Clear Disabled Enabled	1 Disable 0 Read: Disabled 1 Read: Enabled
C RW REGION1WA		Write '1' to Disable non-maskable interrupt for REGION[1].WA event See EVENTS_REGION[1].WA
	Clear Disabled Enabled	1 Disable 0 Read: Disabled 1 Read: Enabled
D RW REGION1RA		Write '1' to Disable non-maskable interrupt for REGION[1].RA event See EVENTS_REGION[1].RA



	numbe	r				23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld Ros	at NvN	000000			. K J I	H G F E D C B A
ld		Field	Value Id	Value		Description
			Clear	1		Disable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
E	RW	REGION2WA				Write '1' to Disable non-maskable interrupt for REGION[2].WA
						event
						See EVENTS_REGION[2].WA
			Clear	1		Disable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
F	RW	REGION2RA				Write '1' to Disable non-maskable interrupt for REGION[2].RA
						event
						See EVENTS_REGION[2].RA
			Clear	1		Disable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
G	RW	REGION3WA				Write '1' to Disable non-maskable interrupt for REGION[3].WA
						event
						Con EVENTS DECION[2] WA
			Clear	1		See EVENTS_REGION[3].WA Disable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
Н	RW	REGION3RA	Enabled	•		Write '1' to Disable non-maskable interrupt for REGION[3].RA
						event
						See EVENTS_REGION[3].RA
			Clear	1		Disable disabl
			Disabled Enabled	0		Read: Disabled Read: Enabled
	D\A/	PREGIONOWA	Enabled	1		Write '1' to Disable non-maskable interrupt for PREGION[0].WA
	11.00	TREGIONOWA				event
						See EVENTS_PREGION[0].WA
			Clear	1		Disable
			Disabled	0		Read: Disabled
	D\A/	DDECIONODA	Enabled	1		Read: Enabled
J	KVV	PREGIONORA				Write '1' to Disable non-maskable interrupt for PREGION[0].RA event
						event
						See EVENTS_PREGION[0].RA
			Clear	1		Disable
			Disabled	0		Read: Disabled
.,			Enabled	1		Read: Enabled
K	RW	PREGION1WA				Write '1' to Disable non-maskable interrupt for PREGION[1].WA
						event
						See EVENTS_PREGION[1].WA
			Clear	1		Disable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
L	RW	PREGION1RA				Write '1' to Disable non-maskable interrupt for PREGION[1].RA
						event
						See EVENTS_PREGION[1].RA
			Clear	1		Disable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled



45.1.7 PERREGION[0].SUBSTATWA

Address offset: 0x400

Source of event/interrupt in region 0, write access detected while corresponding subregion was enabled for watching

Bit n	number		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				ZYXWVUTSRQPONMLKJIHGFEDCB.
Rese	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW SRO			Subregion 0 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
В	RW SR1			Subregion 1 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
С	RW SR2			Subregion 2 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
D	RW SR3			Subregion 3 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
E	RW SR4			Subregion 4 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
F	RW SR5			Subregion 5 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
G	RW SR6			Subregion 6 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
Н	RW SR7			Subregion 7 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
ı	RW SR8			Subregion 8 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
J	RW SR9			Subregion 9 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
K	RW SR10			Subregion 10 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
L	RW SR11			Subregion 11 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
М	RW SR12			Subregion 12 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
N	RW SR13			Subregion 13 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
0	RW SR14			Subregion 14 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
Р	RW SR15			Subregion 15 in region 0 (write '1' to clear)
		NoAccess	0	No write access occurred in this subregion
		Access	1	Write access(es) occurred in this subregion
Q	RW SR16			Subregion 16 in region 0 (write '1' to clear)



Bitı	numbe	er		31 30	29 2	8 27	7 26	25 24	23 :	22 21	. 20	19 1	8 17	16 1	.5 14	1 13	12 1	1 10	9	8 7	6	5	4	3 2	1	0
Id				f e	d c	b	а	Z Y	Х	w v	U	Т 9	S R	Q	РС	N	М	_ K	J	ιн	G	F	E	D C	В	Α
Res	et 0x0	0000000		0 0	0 0	0	0	0 0	0	0 0	0	0 (0 0	0	0 0	0	0 (0 0	0	0 0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value					Des	script	ion															
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
R	RW	SR17							Sub	oregio	n 17	' in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
S	RW	SR18							Sub	regio	n 18	in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
Т	RW	SR19							Sub	oregio	n 19	in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n thi	is sul	oregi	on								
U	RW	SR20							Sub	regio	n 20) in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
٧	RW	SR21							Sub	oregio	n 21	. in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
W	RW	SR22							Sub	oregio	n 22	! in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
Χ	RW	SR23							Sub	oregio	n 23	in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n thi	is sul	oregi	on								
Υ	RW	SR24							Sub	oregio	n 24	in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
Z	RW	SR25							Sub	oregio	n 25	in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
а	RW	SR26							Sub	oregio	n 26	in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
b	RW	SR27							Sub	oregio	n 27	' in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n thi	is sul	oregi	on								
C	RW	SR28							Sub	oregio	n 28	in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
d	RW	SR29							Sub	oregio	n 29	in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
e	RW	SR30							Sub	oregio	n 30) in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	n								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								
f	RW	SR31							Sub	oregio	n 31	in re	egion	0 (w	rite	'1' to	clea	ar)								
			NoAccess	0					No	write	acce	ess o	ccurr	ed ir	this	s sub	regio	on								
			Access	1					Wri	ite ac	cess((es) o	occur	red i	n th	is sul	oregi	on								

45.1.8 PERREGION[0].SUBSTATRA

Address offset: 0x404

Source of event/interrupt in region 0, read access detected while corresponding subregion was enabled for watching



Bit r	numbe	er		31 30	29 28	27 26	5 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
Α	RW	SRO						Subregion 0 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
В	RW	SR1						Subregion 1 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
С	RW	SR2						Subregion 2 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
D	RW	SR3						Subregion 3 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Е	RW	SR4						Subregion 4 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
F	RW	SR5						Subregion 5 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
G	RW	SR6						Subregion 6 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Н	RW	SR7						Subregion 7 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
ı	RW	SR8						Subregion 8 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
J	RW	SR9						Subregion 9 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
K	RW	SR10						Subregion 10 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
L	RW	SR11						Subregion 11 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
М	RW	SR12						Subregion 12 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
N	RW	SR13						Subregion 13 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
0	RW	SR14						Subregion 14 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Р	RW	SR15						Subregion 15 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Q	RW	SR16						Subregion 16 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
R	RW	SR17						Subregion 17 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
S	RW	SR18						Subregion 18 in region 0 (write '1' to clear)



Name	Bit n	umbe	er		31 30	29	28 2	7 26	25 24	1 23	3 22 21 20 1	19 1	8 17 :	16 1	.5 1	4 13	12	11	10	9 8	3 7	6	5	4	3 2	1	0
	Id				f e	d	c l	b a	ΖY	Х	W V U	T S	R	Q	P C	N	М	L	K	JI	Н	G	F	ΕI	D C	В	Α
No. n	Rese	t 0x0	0000000		0 0	0	0 (0 0	0 0	0	0 0 0	0 0	0	0	0 0	0	0	0	0	0 (0	0	0	0	0 0	0	0
No.	Id	RW	Field	Value Id																							
T RW SR19				NoAccess	0					N	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	breg	gion									
No. RW SR20 Subregion 20 in region 0 (write "1" to clear)	Т	RW	SR19							Sı	ubregion 19	in re	gion	0 (w	rite	'1' t	o cl	ear)									
No.				NoAccess	0					N	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No RW SR21 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No RW SR22 NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No Read access(es) occurred in this subregion No Read access(es) occurred in this subregion No Read access occurred in this subregion No Read				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	breg	gion									
Access 1 Read access(es) occurred in this subregion (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subreg	U	RW	SR20							Sı	bregion 20	in re	gion	0 (w	rite	'1' t	o cl	ear)									
Subregion 21 in region 0 (write '1' to clear) NoAccess 1				NoAccess	0					N	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess 0 No read access occurred in this subregion Access 1 Read access[es] occurred in this subregion Subregion 22 in region 0 (write "1" to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access[es] occurred in this subregion Access 1 Read access[Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	bre	gion									
Access 1 Read access(es) occurred in this subregion W RW SR22 Subregion 22 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion X RW SR23 Subregion 23 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access	٧	RW	SR21							Sı	ubregion 21	in re	gion	0 (w	rite	'1' t	o cl	ear)									
Subsection Sub				NoAccess	0					N	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion X RW SR23 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	breg	gion									
Access 1 Read access(es) occurred in this subregion X RW SR23 Subregion 23 in region 0 (write '1' to clear') NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion X RW SR24 Subregion 24 in region 0 (write '1' to clear') NoAccess 0 No read access occurred in this subregion X RW SR25 Subregion 24 in region 0 (write '1' to clear') NoAccess 1 Read access(es) occurred in this subregion X RW SR25 Subregion 25 in region 0 (write '1' to clear') NoAccess 0 No read access occurred in this subregion X RW SR26 Subregion 25 in region 0 (write '1' to clear') NoAccess 1 Read access(es) occurred in this subregion X RW SR26 Subregion 25 in region 0 (write '1' to clear') NoAccess 1 Read access(es) occurred in this subregion X RW SR27 Subregion 26 in region 0 (write '1' to clear') NoAccess 1 Read access(es) occurred in this subregion X RW SR27 Subregion 27 in region 0 (write '1' to clear') NoAccess 1 Read access(es) occurred in this subregion X RW SR28 Subregion 28 in region 0 (write '1' to clear') NoAccess 1 Read access(es) occurred in this subregion X RW SR28 Subregion 28 in region 0 (write '1' to clear') NoAccess 1 Read access occurred in this subregion X RW SR29 Subregion 29 in region 0 (write '1' to clear') NoAccess 1 Read access occurred in this subregion X RW SR29 Subregion 29 in region 0 (write '1' to clear') NoAccess 1 Read access occurred in this subregion X RW SR29 Subregion 29 in region 0 (write '1' to clear') NoAccess 1 Read access occurred in this subregion X RW SR29 Subregion 29 in region 0 (write '1' to clear') NoAccess 1 Read access occurred in this subregion X RW SR29 Subregion 29 in region 0 (write '1' to clear') NoAccess 1 Read access occurred in this subregion X RW SR29 Subregion 29 in region 0 (write '1' to clear') NoAccess 1 Read access occurred in this subregion X RW SR29 Subregion 29 in region 0 (write '1' to clear') NoAccess 1 Read access occurred in this subregion X RW SR29 Subregion 20 in region 0 (write '1' to clear')	W	RW	SR22							Sı	ubregion 22	in re	gion	0 (w	rite	'1' t	o cl	ear)									
NoAccess No No read access occurred in this subregion				NoAccess	0					Ν	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Y RW SR24 SR24 SR25 Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 0 No read access occurred in this subregion Access 0 Noaccess occurred in this subregion Access 1 Read access(es) occurred in this subregion				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	breg	gion									
Access 1 Read access(es) occurred in this subregion Y RW SR24 Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion X RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 2 Read access(es) occurred in this subregion Access 3 Read access(es) occurred in this subregion Access 4 Read access(es) occurred in this subregion Access 5 Read access(es) occurred in this subregion Access 6 Read access(es) o	Χ	RW	SR23							Sı	ubregion 23	in re	gion	0 (w	rite	'1' t	o cl	ear)									
Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Z RW SR25 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access occurred in this subregion (write '1' to clear)				NoAccess	0					N	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Example 2 RW SR25 RW SR25 RW SR25 RW SR26 RW SR26 RW SR26 RW SR26 RW SR27 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Bracess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access occurred in this subregion (write '1' to clear)				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	bre	gion									
Access 1 Read access(es) occurred in this subregion Z RW SR25 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion No read access(es) occurred in this subregion No read access occurred in this subregion No Read access(es) occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion	Υ	RW	SR24							Sı	ubregion 24	in re	gion	0 (w	rite	'1' t	o cl	ear)									
Subregion 25 in region 0 (write '1' to clear) NoAccess 0				NoAccess	0					N	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	ore	gion									
Access 1 Read access(es) occurred in this subregion READ SR26 READ SR26 READ SR27 READ SR27 READ SR28 READ SR29 RE	Z	RW	SR25							Sı	ubregion 25	in re	gion	0 (w	rite	'1' t	o cl	ear)									
Subregion 26 in region 0 (write '1' to clear) NoAccess NoAccess No No read access occurred in this subregion Access Read access(es) occurred in this subregion NoAccess NoAccess NoAccess NoAccess NoAccess Read access(es) occurred in this subregion No read access occurred in this subregion Read access occurred in this subregion Read access(es) occurred in this subregion Read access(es) occurred in this subregion NoAccess NoAccess NoAccess NoAccess Read access(es) occurred in this subregion Read access(es) occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion				NoAccess	0					N	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion By SR27 Subregion 27 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Correct RW SR28 Subregion 28 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Mo RW SR29 Subregion 29 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Subregion 20 (write '1' to clear) No read access occurred in this subregion Access 1 Subregion 30 in region 0 (write '1' to clear)				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	bre	gion									
Access 1 Read access(es) occurred in this subregion By SR27 Subregion 27 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 28 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion MoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion Subregion 29 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion Access 1 Subregion 30 in region 0 (write '1' to clear)	а	RW	SR26							Sı	bregion 26	in re	gion	0 (w	rite	'1' t	o cl	ear)									
Subregion 27 in region 0 (write '1' to clear) NoAccess NoAccess Read access(es) occurred in this subregion Coaccess NoAccess NoAccess NoAccess NoAccess NoAccess NoAccess NoAccess NoAccess NoAccess No Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess NoAccess NoAccess Read access(es) occurred in this subregion No read access occurred in this subregion				NoAccess	0					N	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion SERVITED SERVITED SUBREGION 28 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion SUBREGION 29 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access occurred in this subregion Access 1 Read access occurred in this subregion Subregion 29 in region 0 (write '1' to clear) NoAccess 0 Subregion 30 in region 0 (write '1' to clear)				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	ore	gion									
Access 1 Read access(es) occurred in this subregion C RW SR28 Subregion 28 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 29 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access occurred in this subregion Read access occurred in this subregion Subregion 29 in region 0 (write '1' to clear) No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 30 in region 0 (write '1' to clear)	b	RW	SR27							Sı	ubregion 27	in re	gion	0 (w	rite	'1' t	o cl	ear)									
Subregion 28 in region 0 (write '1' to clear) NoAccess NoAccess Read access(es) occurred in this subregion Read access(es) occurred in this subregion Subregion 29 in region 0 (write '1' to clear) NoAccess NoAccess NoAccess Read access(es) occurred in this subregion Read access occurred in this subregion Subregion 29 in region 0 (write '1' to clear) NoAccess Read access occurred in this subregion Subregion 30 in region 0 (write '1' to clear)				NoAccess	0					N	o read acces	ss oc	curre	d in	this	sub	reg	ion									
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Bubregion 29 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access occurred in this subregion Read access (es) occurred in this subregion Subregion 30 in region 0 (write '1' to clear)				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	ore	gion									
Access 1 Read access(es) occurred in this subregion Subregion 29 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion Subregion 30 in region 0 (write '1' to clear)	С	RW	SR28								_		-														
Subregion 29 in region 0 (write '1' to clear) No Access O No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 30 in region 0 (write '1' to clear)																	_										
No Access 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion E RW SR30 Subregion 30 in region 0 (write '1' to clear)				Access	1						•																
Access 1 Read access(es) occurred in this subregion e RW SR30 Subregion 30 in region 0 (write '1' to clear)	d	RW	SR29								_		-														
e RW SR30 Subregion 30 in region 0 (write '1' to clear)																	_										
				Access	1																						
	е	RW	SR30		_						_		-														
				NoAccess .	0												_										
Access 1 Read access(es) occurred in this subregion				Access	1																						
f RW SR31 Subregion 0 (write '1' to clear)	t	RW	SR31								_		-														
NoAccess 0 No read access occurred in this subregion																	_										
Access 1 Read access(es) occurred in this subregion				Access	1					Re	ead access(e	es) o	ccurre	ed ir	thi	s sul	ore	gion									

45.1.9 PERREGION[1].SUBSTATWA

Address offset: 0x408

Source of event/interrupt in region 1, write access detected while corresponding subregion was enabled for watching

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	7 16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	. 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	V	U -	Г :	S R	Q	Р	0	N N	1 L	K	J	1	Н	G	F	Ε	D (C E	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	alue							De	scrip	otio	n																	
Α	RW	SR0										Sub	reg	ion	0 in	re	gion	1 (\	vrit	e '1'	to c	ear)									
			NoAccess	0								No	writ	te a	cces	ss o	ccui	red	in t	his s	ubr	gio	n									
			Access	1								Wr	ite a	cce	ss(e	es) (occu	rred	l in	this	subr	egi	n									



Rit r	numbe	or .		31 30	29 28	3 27	26.2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	iumbe	-1							X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0	0000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value					Description
В		SR1							Subregion 1 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
С	RW	SR2		_					Subregion 2 in region 1 (write '1' to clear)
Ū		5112	NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
D	R\M	SR3	7100033	•					Subregion 3 in region 1 (write '1' to clear)
	11.00	31(3	NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
E	R\//	SR4	Access	_					Subregion 4 in region 1 (write '1' to clear)
_	11.00	3114	NoAccess	0					No write access occurred in this subregion
			Access	1					
С	D\A/	SR5	Access	1					Write access(es) occurred in this subregion Subregion 5 in region 1 (write 11 to clear)
	11.00	31.3	NoAccess	0					Subregion 5 in region 1 (write '1' to clear) No write access occurred in this subregion
									· ·
_	D\A/	SR6	Access	1					Write access(es) occurred in this subregion
G	KVV	SKO	NaAssass	0					Subregion 6 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
	DVA	CD7	Access	1					Write access(es) occurred in this subregion
Н	KVV	SR7	N-A	0					Subregion 7 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
	DIA	cno.	Access	1					Write access(es) occurred in this subregion
1	RW	SR8		•					Subregion 8 in region 1 (write '1' to clear)
			NoAccess .	0					No write access occurred in this subregion
	5111		Access	1					Write access(es) occurred in this subregion
J	RW	SR9							Subregion 9 in region 1 (write '1' to clear)
			NoAccess .	0					No write access occurred in this subregion
.,			Access	1					Write access(es) occurred in this subregion
K	RW	SR10		•					Subregion 10 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
	5111		Access	1					Write access(es) occurred in this subregion
L	RW	SR11							Subregion 11 in region 1 (write '1' to clear)
			NoAccess .	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
M	RW	SR12		•					Subregion 12 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
	D) 4 /	5043	Access	1					Write access(es) occurred in this subregion
N	RW	SR13	N. A	•					Subregion 13 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
	DIA	CD4.4	Access	1					Write access(es) occurred in this subregion
0	RW	SR14		•					Subregion 14 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
_	5111		Access	1					Write access(es) occurred in this subregion
Р	KW	SR15		•					Subregion 15 in region 1 (write '1' to clear)
			NoAccess .	0					No write access occurred in this subregion
	D	CD4.C	Access	1					Write access(es) occurred in this subregion
Q	RW	SR16		•					Subregion 16 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
_	5 1	5047	Access	1					Write access(es) occurred in this subregion
R	RW	SR17							Subregion 17 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
S	RW	SR18							Subregion 18 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Т	RW	SR19							Subregion 19 in region 1 (write '1' to clear)



Bit r	numbei	r		31 30	29	28	27	26	25	24	2:	3 22 21 20	0 19	18 1	7 1	16 1	15 1	14	13 1	2 :	11 1	0 9	8	7	6	5	4	3	2 1	. 0
Id												. w v u																		
	et 0x00	000000										000																		
Id	RW		Value Id	Value								escription																		
			NoAccess	0								o write acc		occu	rre	d ir	n th	is :	subr	egi	on									
			Access	1								rite access								-										
U	RW	SR20	7100035	-								ubregion 2								_										
Ū		51125	NoAccess	0								o write aco		-		•														
			Access	1								rite access								_										
V	R\M	SR21	7100033	•								ubregion 2																		
٧	11.00	SILET	NoAccess	0								o write acc		-																
			Access	1								rite access								-										
W	RW	SP22	Access	1								ubregion 2								_										
vv	NVV	3822	NoAccess	0								o write acc		-		•														
																				-										
V	DIA	CD22	Access	1								rite acces																		
X	KVV	SR23	AL A	•								ubregion 2		-																
			NoAccess	0								o write aco								-										
.,			Access	1								rite access								_										
Υ	RW	SR24		_								ubregion 2		-		•														
			NoAccess	0								o write aco								-										
_			Access	1								rite acces								_										
Z	RW	SR25										ubregion 2		Ŭ		•					,									
			NoAccess	0								o write acc								Ŭ										
			Access	1								rite access								_										
а	RW	SR26										ubregion 2		-		•														
			NoAccess	0								o write acc								-										
			Access	1								rite acces								_										
b	RW	SR27										ubregion 2		•		•														
			NoAccess	0							N	o write acc	cess	occu	rre	d ir	n th	is :	subr	egi	on									
			Access	1							W	rite acces	s(es)	occı	ırr	ed i	in th	his	sub	reg	ion									
С	RW	SR28									Sı	ubregion 2	28 in 1	egic	n :	1 (v	vrite	e '1	l' to	cle	ar)									
			NoAccess	0							N	o write acc	cess	occu	rre	d ir	n th	is :	subr	egi	on									
			Access	1							W	rite acces	s(es)	occı	ırr	ed i	in tl	his	sub	reg	ion									
d	RW	SR29									Sı	ubregion 2	29 in 1	regio	n :	1 (v	vrite	e '1	l' to	cle	ar)									
			NoAccess	0							N	o write acc	cess	occu	rre	ıi b	n th	is :	subr	egi	on									
			Access	1							W	rite access	s(es)	occı	ırr	ed i	in th	his	sub	reg	ion									
е	RW	SR30									Sı	ubregion 3	30 in 1	regio	n :	1 (v	vrite	e '1	l' to	cle	ar)									
			NoAccess	0							N	o write acc	cess	occu	rre	d ir	n th	is :	subr	egi	on									
			Access	1							W	rite access	s(es)	occı	ırr	ed i	in th	his	sub	reg	ion									
f	RW	SR31									Sı	ubregion 3	31 in 1	egic	n :	1 (v	vrite	e '1	l' to	cle	ar)									
			NoAccess	0							N	o write acc	cess	occu	rre	d ir	n th	is :	subr	egi	on									
			Access	1							W	rite acces	s(es)	occı	ırr	ed i	in th	his	sub	reg	ion									

45.1.10 PERREGION[1].SUBSTATRA

Address offset: 0x40C

Source of event/interrupt in region 1, read access detected while corresponding subregion was enabled for watching

Bit n	umbe	er		31	30	29	28	27	26 2	25 :	24 2	23 2	22 2	1 20	19	18	17	16	15	14	13 1	2 1	1 1	0 9	8	7	6	5	4	3 2	2 :	1 0
Id				f	е	d	С	b	a i	Z	Υ	X '	W١	/ U	Т	S	R	Q	Р	О	N I	M I	_ k	J	-1	Н	G	F	Е	D (C E	ВА
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tion																		
Α	RW	SR0									9	Sub	regi	on 0	inı	regi	on 1	. (w	rite	'1'	to c	lear	·)									
			NoAccess	0							1	No i	ead	l acc	ess	occ	urre	d i	n th	is s	ubre	gio	n									
			Access	1							F	Rea	d ac	cess	(es) oc	curr	ed	in th	nis s	subr	egio	n									
В	RW	SR1									9	Sub	regi	on 1	in i	regi	on 1	(w	rite	'1'	to c	lear)									
			NoAccess	0							1	No i	ead	l acc	ess	occ	urre	d i	n th	is s	ubre	gio	n									
			Access	1							F	Rea	d ac	cess	(es) oc	curr	ed	in th	nis s	subr	egio	on									



Bit r	number			31 30	29 28	27 26	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00	000000		0 0	0 0	0 0	0 0	
Id	RW F	Field	Value Id	Value				Description
С	RW S	SR2						Subregion 2 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
D	RW S	SR3						Subregion 3 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Ε	RW S	SR4						Subregion 4 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
F	RW S	SR5						Subregion 5 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
G	RW S	SR6						Subregion 6 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Н	RW S	SR7						Subregion 7 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
I	RW S	SR8						Subregion 8 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
J	RW S	SR9						Subregion 9 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
K	RW S	SR10						Subregion 10 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
L	RW S	SR11						Subregion 11 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
М	RW S	SR12						Subregion 12 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
N	RW S	SR13						Subregion 13 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
0	RW S	SR14						Subregion 14 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Р	RW S	SR15						Subregion 15 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Q	RW S	SR16						Subregion 16 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
R	RW S	SR17						Subregion 17 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
S	RW S	SR18						Subregion 18 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Т	RW S	SR19						Subregion 19 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
U	RW S	SR20						Subregion 20 in region 1 (write '1' to clear)
-	•							_ , ,



Bitı	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	set 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
٧	RW SR21		Subregion 21 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
W	RW SR22		Subregion 22 in region 1 (write '1' to clear)
		NoAccess	O No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Χ	RW SR23		Subregion 23 in region 1 (write '1' to clear)
		NoAccess	O No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Υ	RW SR24		Subregion 24 in region 1 (write '1' to clear)
		NoAccess	O No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Z	RW SR25		Subregion 25 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
а	RW SR26		Subregion 26 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
b	RW SR27		Subregion 27 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
С	RW SR28		Subregion 28 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
d	RW SR29		Subregion 29 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
е	RW SR30		Subregion 30 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
f	RW SR31		Subregion 31 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion

45.1.11 REGIONEN

Address offset: 0x510

Enable/disable regions watch

Bit r	iumbe	er		31	30 2	9 2	8 27	7 26	25	24	23	22	21 2	0 1	19 1	18 1	.7 1	.6	L5 :	14 :	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id							L	K	J	1																Н	G	F	Ε	D C	В	Α
Res	et 0x0	0000000		0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	lue						Des	scri	ptio	n																		
Α	RW	RGN0WA									Ena	able	/dis	abl	e w	rite	aco	ces	s w	atc	h in	regi	ion[0]								
			Disable	0							Disa	able	e wr	ite	acc	ess	wa	tch	in	this	reg	ion										
			Enable	1							Ena	able	wri	te a	ассе	ess	wat	ch	in t	his	reg	ion										
В	RW	RGNORA									Ena	able	/dis	abl	e re	ad	acc	ess	W	atch	in	regio	on[C]								
			Disable	0							Disa	able	e rea	nd a	ассе	ss ı	wat	ch	in t	his	reg	ion										
			Enable	1							Ena	able	rea	d a	cce	ss v	/atc	ch i	n tl	his ı	regi	on										
С	RW	RGN1WA									Ena	able	/dis	abl	e w	rite	aco	ces	s w	atc	h in	regi	on[1]								
			Disable	0							Disa	able	e wr	ite	acc	ess	wa	tch	in	this	reg	ion										
			Enable	1							Ena	able	wri	te a	ассе	ess	wat	ch	in t	his	reg	ion										
D	RW	RGN1RA									Ena	able	/dis	abl	e re	ad	acc	ess	Wa	atch	in	regio	on[1	.]								



Bitı	numbe	er		31	30	29 2	28 2	7 26	5 25	24	23	3 22	21 2	20	19 1	.8 1	7 1	5 1	5 14	13	12	11 :	10 9	9 1	8 7	' (5 5	4	3	2	1	0
Id							L	. K	J	1															F	1 (3 F	Е	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						De	escri	iptio	n																		
			Disable	0							Di	isabl	le rea	ad a	acce	ss v	vato	h ir	thi	s re	gior	ı										
			Enable	1							En	nable	e rea	ıd a	cce	ss v	atc	h in	thi	s reg	ion											
Е	RW	RGN2WA									En	nable	e/dis	ab	le w	rite	acc	ess	wa	ch i	n re	gior	[2]									
			Disable	0							Di	isabl	le wr	ite	acc	ess	wat	ch i	n th	is re	gio	n										
			Enable	1							En	nable	e wri	ite	acce	ss ı	vato	h ii	th	is re	gior	ı										
F	RW	RGN2RA									En	nable	e/dis	ab	le re	ad	ассе	ess '	vat	ch ir	re	gion	[2]									
			Disable	0							Di	isabl	le rea	ad a	acce	ss v	vato	h ir	thi	s re	gior	1										
			Enable	1							En	nable	e rea	ıd a	cce	ss v	atc	h in	thi	s reg	ion											
G	RW	RGN3WA									En	nable	e/dis	ab	le w	rite	acc	ess	wa	ch i	n re	gior	1[3]									
			Disable	0							Di	isabl	le wr	ite	acc	ess	wat	ch i	n th	is re	gio	n										
			Enable	1							En	nable	e wri	ite	acce	ss ı	vato	h ii	th	is re	gior	ı										
Н	RW	RGN3RA									En	nable	e/dis	ab	le re	ad	ассе	ess '	vat	ch ir	re	gion	[3]									
			Disable	0							Di	isabl	le rea	ad a	acce	ss v	vato	h ir	thi	s re	gior	1										
			Enable	1							En	nable	e rea	ıd a	cce	ss v	atc	h in	thi	s reg	ion											
1	RW	PRGNOWA									En	nable	e/dis	ab	le w	rite	acc	ess	wa	ch i	n Pf	REGI	ON	[0]								
			Disable	0							Di	isabl	le wr	ite	acc	ess	wat	ch i	n th	is P	REG	ION										
			Enable	1							En	nable	e wri	ite	acce	ss ı	vato	h ii	th	is PF	EG	ON										
J	RW	PRGNORA									En	nable	e/dis	ab	le re	ad	ассе	ess '	vat	ch ir	PR	EGI	ON[0]								
			Disable	0							Di	isabl	le rea	ad a	acce	ss v	vato	h ir	thi	s PF	EGI	ON										
			Enable	1							En	nable	e rea	ıd a	cce	ss v	atc	h in	thi	s PR	EGI	NC										
K	RW	PRGN1WA									En	nable	e/dis	ab	le w	rite	acc	ess	wa	ch i	n Pf	REGI	ON	[1]								
			Disable	0							Di	isabl	le wr	ite	acc	ess	wat	ch i	n th	is P	REG	ION										
			Enable	1							En	nable	e wri	ite	acce	ess 1	vato	h ii	th	is PF	EG	ON										
L	RW	PRGN1RA									En	nable	e/dis	ab	le re	ad	ассе	ess '	vat	ch ir	PR	EGI]NC	1]								
			Disable	0							Di	isabl	le rea	ad a	acce	SS \	vato	h ir	th	s PF	EGI	ON										
			Enable	1							En	nable	e rea	ıd a	cce	ss v	atc	h in	thi	s PR	EGI	NC										

45.1.12 REGIONENSET

Address offset: 0x514 Enable regions watch

Bit	numbe	r		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K J I	H G F E D C B A
Res	et 0x00	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	RGN0WA			Enable write access watch in region[0]
			Set	1	Enable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
В	RW	RGNORA			Enable read access watch in region[0]
			Set	1	Enable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
С	RW	RGN1WA			Enable write access watch in region[1]
			Set	1	Enable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
D	RW	RGN1RA			Enable read access watch in region[1]
			Set	1	Enable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
Е	RW	RGN2WA			Enable write access watch in region[2]
			Set	1	Enable write access watch in this region
			Disabled	0	Write access watch in this region is disabled



Bit	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K J	I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Enabled	1	Write access watch in this region is enabled
F	RW RGN2RA			Enable read access watch in region[2]
		Set	1	Enable read access watch in this region
		Disabled	0	Read access watch in this region is disabled
		Enabled	1	Read access watch in this region is enabled
G	RW RGN3WA			Enable write access watch in region[3]
		Set	1	Enable write access watch in this region
		Disabled	0	Write access watch in this region is disabled
		Enabled	1	Write access watch in this region is enabled
Н	RW RGN3RA			Enable read access watch in region[3]
		Set	1	Enable read access watch in this region
		Disabled	0	Read access watch in this region is disabled
		Enabled	1	Read access watch in this region is enabled
1	RW PRGNOWA			Enable write access watch in PREGION[0]
		Set	1	Enable write access watch in this PREGION
		Disabled	0	Write access watch in this PREGION is disabled
		Enabled	1	Write access watch in this PREGION is enabled
J	RW PRGNORA			Enable read access watch in PREGION[0]
		Set	1	Enable read access watch in this PREGION
		Disabled	0	Read access watch in this PREGION is disabled
		Enabled	1	Read access watch in this PREGION is enabled
K	RW PRGN1WA			Enable write access watch in PREGION[1]
		Set	1	Enable write access watch in this PREGION
		Disabled	0	Write access watch in this PREGION is disabled
		Enabled	1	Write access watch in this PREGION is enabled
L	RW PRGN1RA			Enable read access watch in PREGION[1]
		Set	1	Enable read access watch in this PREGION
		Disabled	0	Read access watch in this PREGION is disabled
		Enabled	1	Read access watch in this PREGION is enabled

45.1.13 REGIONENCLR

Address offset: 0x518 Disable regions watch

Bit	number			31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K J I	HGFEDCBA
Res	et 0x00000	0000		0 0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Fiel	ld	Value Id	Value	Description
Α	RW RGI	N0WA			Disable write access watch in region[0]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
В	RW RGN	NORA			Disable read access watch in region[0]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
С	RW RGN	N1WA			Disable write access watch in region[1]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
D	RW RGN	N1RA			Disable read access watch in region[1]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled



Bit	numbe	er		31 30 2	9 28 2	7 26 :	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					l	L K	JI	HGFEDCBA
Res	et 0x0	0000000		0 0 0	0 0 0	0 0	0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value				Description
Ε	RW	RGN2WA						Disable write access watch in region[2]
			Clear	1				Disable write access watch in this region
			Disabled	0				Write access watch in this region is disabled
			Enabled	1				Write access watch in this region is enabled
F	RW	RGN2RA						Disable read access watch in region[2]
			Clear	1				Disable read access watch in this region
			Disabled	0				Read access watch in this region is disabled
			Enabled	1				Read access watch in this region is enabled
G	RW	RGN3WA						Disable write access watch in region[3]
			Clear	1				Disable write access watch in this region
			Disabled	0				Write access watch in this region is disabled
			Enabled	1				Write access watch in this region is enabled
Н	RW	RGN3RA						Disable read access watch in region[3]
			Clear	1				Disable read access watch in this region
			Disabled	0				Read access watch in this region is disabled
			Enabled	1				Read access watch in this region is enabled
1	RW	PRGN0WA						Disable write access watch in PREGION[0]
			Clear	1				Disable write access watch in this PREGION
			Disabled	0				Write access watch in this PREGION is disabled
			Enabled	1				Write access watch in this PREGION is enabled
J	RW	PRGNORA						Disable read access watch in PREGION[0]
			Clear	1				Disable read access watch in this PREGION
			Disabled	0				Read access watch in this PREGION is disabled
			Enabled	1				Read access watch in this PREGION is enabled
K	RW	PRGN1WA						Disable write access watch in PREGION[1]
			Clear	1				Disable write access watch in this PREGION
			Disabled	0				Write access watch in this PREGION is disabled
			Enabled	1				Write access watch in this PREGION is enabled
L	RW	PRGN1RA						Disable read access watch in PREGION[1]
			Clear	1				Disable read access watch in this PREGION
			Disabled	0				Read access watch in this PREGION is disabled
			Enabled	1				Read access watch in this PREGION is enabled

45.1.14 REGION[0].START

Address offset: 0x600 Start address for region 0

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW START		Start address for region

45.1.15 REGION[0].END

Address offset: 0x604 End address of region 0

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value Description
A RW END	End address of region.



45.1.16 REGION[1].START

Address offset: 0x610 Start address for region 1

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	Д Д	A	Α	Α	Α	Α	Α	Α	A	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	START										Sta	rt a	ddr	ess	for	re	gior	1														

45.1.17 REGION[1].END

Address offset: 0x614 End address of region 1

Bit numbe	r		31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	L9 1	L8 1	17 1	16	15 :	14	13 1	12 1	1 1	0 9	8	7	6	5	4	3	2	1 0	l
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A	Α	Α	Α	Α.	Α.	A A	A	. A	Α	Α	Α	Α	Α	A	А А	l
Reset 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	l
Id RW	Field	Value Id	Va	lue							Des	crip	otio	n																			l
A RW	END										End	l ad	dre	ss o	f re	gio	n.																ì

45.1.18 REGION[2].START

Address offset: 0x620 Start address for region 2

Bit r	numbe	er		31	30	29	28	27	' 26	25	24	23	22	21	20	19	18 :	17 1	16 1	L5 1	4 1	3 1	2 11	. 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A .	Δ ,	Α Δ	A	Α	Α	Α	Α	Α	Α	Α	A A	4 A	AA
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	START										Sta	rt a	ddr	ess	for	reg	ion	1														

45.1.19 REGION[2].END

Address offset: 0x624 End address of region 2

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW END		End address of region.

45.1.20 REGION[3].START

Address offset: 0x630 Start address for region 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW START		Start address for region

45.1.21 REGION[3].END

Address offset: 0x634 End address of region 3



Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20	19 :	18 :	17 :	16	15 3	14	13 :	12 :	11 1	.0 9	9	8 7	7	6 5	5 4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	Δ.	A A	Δ,	4 4	A A	Α	Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 ()	0 (0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																		
Α	RW	END										Enc	l ad	dre	ss c	of re	egic	n.															

45.1.22 PREGION[0].START

Address offset: 0x6C0

Reserved for future use

Bit r	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	А А
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Value Id	Va	lue							De	scri	pti	on																				
	_											_			,	٠.																		

A R START Reserved for future use

45.1.23 PREGION[0].END

Address offset: 0x6C4

Reserved for future use

Bitı	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	Α Α	4 <i>A</i>	Α Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	λ Δ	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	END										Res	erve	ed f	or f	utu	re u	se															

45.1.24 PREGION[0].SUBS

Address offset: 0x6C8 Subregions of region 0

Bitı	numbe	er		31 30	29	28 2	7 26	25	24 2	23 :	22 2	21 2	0 1	9 18	3 17	16	15 1	14 1	13 12	2 11	10	9	8	7 (5 5	4	3	2 1	١ 0
Id				f e	d	c l	о а	Z	Υ	Χ	W١	V	U T	S	R	Q	Р	0	N M	1 L	K	J	1 1	4 (3 F	Ε	D	C E	3 A
Res	et 0x0	0000000		0 0	0	0 (0 0	0	0	0	0 (0	0 0	0	0	0	0	0	0 0	0	0	0	0) (0	0	0	0 () 0
Id	RW	Field	Value Id	Value	9				ı	Des	scrip	tio	n																
Α	RW	SR0							ı	Incl	lude	or	excl	ude	sub	reg	on () in	regi	on									
			Exclude	0						Exc	lude	•																	
			Include	1					ı	Incl	lude																		
В	RW	SR1							- 1	Incl	lude	or	excl	ude	sub	reg	on :	l in	regi	on									
			Exclude	0					1	Exc	lude	:																	
			Include	1					ı	Incl	lude																		
С	RW	SR2							ı	Incl	lude	or	excl	ude	sub	reg	on 2	2 in	regi	on									
			Exclude	0					1	Exc	lude	:																	
			Include	1					ı	Incl	lude																		
D	RW	SR3							- 1	Incl	lude	or	excl	ude	sub	reg	on 3	3 in	regi	on									
			Exclude	0						Exc	lude	:																	
			Include	1					ı	Incl	lude																		
Е	RW	SR4							ı	Incl	lude	or	excl	ude	sub	reg	on 4	1 in	regi	on									
			Exclude	0					1	Exc	lude	:																	
			Include	1					ı	Incl	lude																		
F	RW	SR5							- 1	Incl	lude	or	excl	ude	sub	reg	on 5	5 in	regi	on									
			Exclude	0					1	Exc	lude	:																	
			Include	1					ı	Incl	lude																		
G	RW	SR6							ı	Incl	lude	or	excl	ude	sub	reg	on 6	in	regi	on									
			Exclude	0					1	Exc	lude	:																	
			Include	1					ı	Incl	lude																		



Bit n	umbe	er		31 30	29 28	27	26.2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0	0000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
Н	RW	SR7							Include or exclude subregion 7 in region
			Exclude	0					Exclude
			Include	1					Include
I	RW	SR8							Include or exclude subregion 8 in region
			Exclude	0					Exclude
			Include	1					Include
J	RW	SR9							Include or exclude subregion 9 in region
			Exclude	0					Exclude
			Include	1					Include
K	RW	SR10							Include or exclude subregion 10 in region
			Exclude	0					Exclude
			Include	1					Include
L	RW	SR11							Include or exclude subregion 11 in region
			Exclude	0					Exclude
			Include	1					Include
М	RW	SR12							Include or exclude subregion 12 in region
			Exclude	0					Exclude
			Include	1					Include
N	RW	SR13		_					Include or exclude subregion 13 in region
			Exclude	0					Exclude
	5111		Include	1					Include
0	RW	SR14	5 1 1						Include or exclude subregion 14 in region
			Exclude	0					Exclude
Р	DIA	CD1F	Include	1					Include
P	KVV	SR15	Evoludo	0					Include or exclude subregion 15 in region Exclude
			Exclude Include	1					Include
Q	R\M	SR16	include	1					Include or exclude subregion 16 in region
Q	11.00	31(10	Exclude	0					Exclude
			Include	1					Include
R	RW	SR17							Include or exclude subregion 17 in region
			Exclude	0					Exclude
			Include	1					Include
S	RW	SR18							Include or exclude subregion 18 in region
			Exclude	0					Exclude
			Include	1					Include
Т	RW	SR19							Include or exclude subregion 19 in region
			Exclude	0					Exclude
			Include	1					Include
U	RW	SR20							Include or exclude subregion 20 in region
			Exclude	0					Exclude
			Include	1					Include
V	RW	SR21							Include or exclude subregion 21 in region
			Exclude	0					Exclude
			Include	1					Include
W	RW	SR22							Include or exclude subregion 22 in region
			Exclude	0					Exclude
			Include	1					Include
Х	RW	SR23							Include or exclude subregion 23 in region
			Exclude	0					Exclude
			Include	1					Include
Υ	RW	SR24							Include or exclude subregion 24 in region
			Exclude	0					Exclude
			Include	1					Include
Z	RW	SR25							Include or exclude subregion 25 in region



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
Exclude	0 Exclude
Include	1 Include
a RW SR26	Include or exclude subregion 26 in region
Exclude	0 Exclude
Include	1 Include
b RW SR27	Include or exclude subregion 27 in region
Exclude	0 Exclude
Include	1 Include
c RW SR28	Include or exclude subregion 28 in region
Exclude	0 Exclude
Include	1 Include
d RW SR29	Include or exclude subregion 29 in region
Exclude	0 Exclude
Include	1 Include
e RW SR30	Include or exclude subregion 30 in region
Exclude	0 Exclude
Include	1 Include
f RW SR31	Include or exclude subregion 31 in region
Exclude	0 Exclude
Include	1 Include

45.1.25 PREGION[1].START

Address offset: 0x6D0

Reserved for future use

Bitı	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	R	START										Res	erv	/ed	for	fut	ure	use	9															

45.1.26 PREGION[1].END

Address offset: 0x6D4

Reserved for future use

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	R	END										Res	serv	ved	for	fut	ure	use	9															

45.1.27 PREGION[1].SUBS

Address offset: 0x6D8 Subregions of region 1

Bit r	numb	er		31	. 30	29	28	3 2	7 26	5 2	5 2	24 2	23 2	22 2	21 2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	.3 1	.2 1	11 1	0 9	9	8 7	6	5	4	3	2	1	0
Id				f	е	d	С	b	а	Z	· \	Y	X١	۸١	Vι	JI	Г :	S F	2	Q F) () I	1 /	VI	LI	Κ.	J	I F	G	F	Ε	D	С	В	Α
Res	et 0x	00000000		0	0	0	0	0	0	0) (0	0	0 (0 (0 () (0 () () () ()	0	0	0 () ()	0 0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue	•							Des	crip	tio	n																			
Α	RW	SR0										ı	ncli	ıde	or	excl	lud	e su	bre	gio	n 0	in	reg	ion											7
			Exclude	0								E	xcl	ude	•																				



Bit n	umbe	er		31 30	29 28	27 2	6 25 :	24 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z	Υ :	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Rese	et 0x0	0000000		0 0	0 0	0 0	0	0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value					Description
			Include	1				I	Include
В	RW	SR1						I	Include or exclude subregion 1 in region
			Exclude	0				E	Exclude
			Include	1				I	Include
С	RW	SR2						I	Include or exclude subregion 2 in region
			Exclude	0				E	Exclude
			Include	1				li	Include
D	RW	SR3						li	Include or exclude subregion 3 in region
			Exclude	0				E	Exclude
			Include	1				I	Include
E	RW	SR4						I	Include or exclude subregion 4 in region
			Exclude	0				E	Exclude
			Include	1				I	Include
F	RW	SR5							Include or exclude subregion 5 in region
			Exclude	0					Exclude
			Include	1					Include
G	RW	SR6							Include or exclude subregion 6 in region
			Exclude	0					Exclude
			Include	1					Include
Н	RW	SR7							Include or exclude subregion 7 in region
			Exclude	0					Exclude
	5111		Include	1					Include
ı	RW	SR8							Include or exclude subregion 8 in region
			Exclude	0					Exclude
	DIM	500	Include	1					Include
J	KW	SR9	Fredrick	0					Include or exclude subregion 9 in region
			Exclude	0					Exclude Include
V	D\A/	CB10	Include	1					
K	NVV	SR10	Exclude	0					Include or exclude subregion 10 in region Exclude
			Include	1					Include
L	R\M	SR11	iliciade	1					Include or exclude subregion 11 in region
-	11.00	SKII	Exclude	0					Exclude
			Include	1					Include
М	RW	SR12	molade	-					Include or exclude subregion 12 in region
		0.122	Exclude	0					Exclude
			Include	1					Include
N	RW	SR13							Include or exclude subregion 13 in region
			Exclude	0					Exclude
			Include	1				li	Include
0	RW	SR14							Include or exclude subregion 14 in region
			Exclude	0					Exclude
			Include	1					Include
Р	RW	SR15							Include or exclude subregion 15 in region
			Exclude	0					Exclude
			Include	1					Include
Q	RW	SR16							Include or exclude subregion 16 in region
			Exclude	0					Exclude
			Include	1				li	Include
R	RW	SR17						- I	Include or exclude subregion 17 in region
			Exclude	0				E	Exclude
			Include	1				I	Include
S	RW	SR18						I	Include or exclude subregion 18 in region
			Exclude	0				E	Exclude
			Include	1				I	Include



Bit	numb	er		31 30	29 :	28 2	7 26	25 24	1 2	23 22 2	1 2	20 1	9 1	8 1	7 1	16	15	14	13 :	12	11 :	.0	9 8	3 7	6	5	4	3	2	1 0	ĺ
Id				f e	d	c ł	о а	Z Y		x w v	V	U 1	Г	S	R	Q	Р	О	N	М	L	K .	J	Н	G	F	Ε	D	С	ВА	l
Res	et 0x0	0000000		0 0	0	0 (0 0	0 0	(0 0 (0	0 ()	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	Value					C	Descrip	tio	n																			١
Т	RW	SR19							li	nclude	or	excl	lud	e sı	ıbr	eg	on	19 i	n re	egio	n										ĺ
			Exclude	0					E	xclude	!																				
			Include	1					li	nclude																					
U	RW	SR20							li	nclude	or	excl	lud	e sı	ıbr	eg	on	2 0 i	n re	egio	n										
			Exclude	0					E	xclude	!																				
			Include	1					li	nclude																					
V	RW	SR21							li	nclude	or	excl	lud	e sı	ıbr	eg	on	21 i	n re	egio	n										
			Exclude	0					Е	xclude	!																				
			Include	1						nclude																					
W	RW	SR22								nclude		excl	lud	e sı	ıbr	eg	on	22 i	n re	egio	n										
			Exclude	0						xclude																					
			Include	1						nclude																					
Х	RW	SR23		_						nclude		excl	lud	e sı	ıbr	eg	on	23 i	n re	egio	n										
			Exclude	0						xclude																					
.,	DIA	5024	Include	1						nclude								- ·													
Υ	RW	SR24	5 1 1	•						nclude · · ·		excl	lud	e sı	ıbr	eg	on	24	n re	egio	n										
			Exclude	0						xclude																					
Z	D\A/	SR25	Include	1						nclude		ovel	اسما		.h.	~~		25:													
2	KVV	3R23	Exclude	0						nclude xclude		exci	luu	e si	וטנ	eg	OH	25	1116	gu)[]										
			Include	1						nclude																					
а	RW	SR26	meduce	-						nclude		excl	lud	e si	ıhr	ρø	on	26 i	n re	οσiα	n										
u		SKEO	Exclude	0						xclude		CACI	uu	C 30		-Б	011			-6"											
			Include	1						nclude																					
b	RW	SR27								nclude		excl	lud	e sı	ıbr	eg	on	27 i	n re	egio	n										
			Exclude	0						xclude						-0															
			Include	1					h	nclude																					
С	RW	SR28							h	nclude	or	excl	lud	e sı	ıbr	eg	on	28 i	n re	egio	n										
			Exclude	0					Е	xclude																					
			Include	1					h	nclude																					
d	RW	SR29							li	nclude	or	excl	lud	e sı	ıbr	eg	on	2 9 i	n re	egio	n										
			Exclude	0					Е	xclude	!																				
			Include	1					h	nclude																					
е	RW	SR30							li	nclude	or	excl	lud	e sı	ıbr	eg	on	30	n re	egio	n										
			Exclude	0					Е	xclude	!																				
			Include	1					h	nclude																					
f	RW	SR31							h	nclude	or	excl	lud	e sı	ıbr	eg	on	31 i	n re	egio	n										
			Exclude	0					E	xclude																					
			Include	1					li	nclude																					



46 EGU — Event generator unit

The Event generator unit (EGU) provides support for inter-layer signaling. This means support for atomic triggering of both CPU execution and hardware tasks from both firmware (by CPU) and hardware (by PPI). This feature can, for instance, be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's ISR execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- · Enables SW triggering of interrupts
- 6 EGU instances separate interrupt vectors
- Up to 16 separate event flags per interrupt for multiplexing

The EGU implements a set of tasks which can individually be triggered to generate the corresponding event, i.e., the corresponding event for TASKS_TRIGGER[n] is EVENTS_TRIGGERED[n].

Table 109: EGU configuration

EGU instance	Number of event flags
0-5	16

46.1 Registers

Table 110: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40014000	EGU	EGU0	Event Generator Unit 0	
0x40015000	EGU	EGU1	Event Generator Unit 1	
0x40016000	EGU	EGU2	Event Generator Unit 2	
0x40017000	EGU	EGU3	Event Generator Unit 3	
0x40018000	EGU	EGU4	Event Generator Unit 4	
0x40019000	EGU	EGU5	Event Generator Unit 5	

Table 111: Register Overview

Register	Offset	Description
_		
TASKS_TRIGGER[0]	0x000	Trigger 0 for triggering the corresponding TRIGGERED[0] event
TASKS_TRIGGER[1]	0x004	Trigger 1 for triggering the corresponding TRIGGERED[1] event
TASKS_TRIGGER[2]	0x008	Trigger 2 for triggering the corresponding TRIGGERED[2] event
TASKS_TRIGGER[3]	0x00C	Trigger 3 for triggering the corresponding TRIGGERED[3] event
TASKS_TRIGGER[4]	0x010	Trigger 4 for triggering the corresponding TRIGGERED[4] event
TASKS_TRIGGER[5]	0x014	Trigger 5 for triggering the corresponding TRIGGERED[5] event
TASKS_TRIGGER[6]	0x018	Trigger 6 for triggering the corresponding TRIGGERED[6] event
TASKS_TRIGGER[7]	0x01C	Trigger 7 for triggering the corresponding TRIGGERED[7] event
TASKS_TRIGGER[8]	0x020	Trigger 8 for triggering the corresponding TRIGGERED[8] event
TASKS_TRIGGER[9]	0x024	Trigger 9 for triggering the corresponding TRIGGERED[9] event
TASKS_TRIGGER[10]	0x028	Trigger 10 for triggering the corresponding TRIGGERED[10] event
TASKS_TRIGGER[11]	0x02C	Trigger 11 for triggering the corresponding TRIGGERED[11] event
TASKS_TRIGGER[12]	0x030	Trigger 12 for triggering the corresponding TRIGGERED[12] event
TASKS_TRIGGER[13]	0x034	Trigger 13 for triggering the corresponding TRIGGERED[13] event
TASKS_TRIGGER[14]	0x038	Trigger 14 for triggering the corresponding TRIGGERED[14] event
TASKS_TRIGGER[15]	0x03C	Trigger 15 for triggering the corresponding TRIGGERED[15] event
EVENTS_TRIGGERED[0]	0x100	Event number 0 generated by triggering the corresponding TRIGGER[0] task
EVENTS_TRIGGERED[1]	0x104	Event number 1 generated by triggering the corresponding TRIGGER[1] task
EVENTS_TRIGGERED[2]	0x108	Event number 2 generated by triggering the corresponding TRIGGER[2] task
EVENTS_TRIGGERED[3]	0x10C	Event number 3 generated by triggering the corresponding TRIGGER[3] task
EVENTS_TRIGGERED[4]	0x110	Event number 4 generated by triggering the corresponding TRIGGER[4] task



Register	Offset	Description
EVENTS_TRIGGERE	D[5] 0x114	Event number 5 generated by triggering the corresponding TRIGGER[5] task
EVENTS_TRIGGERE	D[6] 0x118	Event number 6 generated by triggering the corresponding TRIGGER[6] task
EVENTS_TRIGGERE	D[7] 0x11C	Event number 7 generated by triggering the corresponding TRIGGER[7] task
EVENTS_TRIGGERE	D[8] 0x120	Event number 8 generated by triggering the corresponding TRIGGER[8] task
EVENTS_TRIGGERE	D[9] 0x124	Event number 9 generated by triggering the corresponding TRIGGER[9] task
EVENTS_TRIGGERE	D[10] 0x128	Event number 10 generated by triggering the corresponding TRIGGER[10] task
EVENTS_TRIGGERE	D[11] 0x12C	Event number 11 generated by triggering the corresponding TRIGGER[11] task
EVENTS_TRIGGERE	D[12] 0x130	Event number 12 generated by triggering the corresponding TRIGGER[12] task
EVENTS_TRIGGERE	D[13] 0x134	Event number 13 generated by triggering the corresponding TRIGGER[13] task
EVENTS_TRIGGERE	D[14] 0x138	Event number 14 generated by triggering the corresponding TRIGGER[14] task
EVENTS_TRIGGERE	D[15] 0x13C	Event number 15 generated by triggering the corresponding TRIGGER[15] task
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

46.1.1 INTEN

Address offset: 0x300 Enable or disable interrupt

			·	21 20 20 20 27 26 25 24	1 22 22 21 20 10 10 17 16 17 14 12 12 11 10 0 0 7 6 7 4 2 2 4 0
Id	numbe	er		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 PONMLKJIHGFEDCBA
	o+ 0v0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	
A		TRIGGERED0	value lu	value	Description Enable or disable interrupt for TRIGGERED[0] event
	11.00	TRIGGEREDO			, , , , , , , , , , , , , , , , , , , ,
					See EVENTS_TRIGGERED[0]
			Disabled	0	Disable
_			Enabled	1	Enable
В	RW	TRIGGERED1			Enable or disable interrupt for TRIGGERED[1] event
					See EVENTS_TRIGGERED[1]
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	TRIGGERED2			Enable or disable interrupt for TRIGGERED[2] event
					See EVENTS_TRIGGERED[2]
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	TRIGGERED3			Enable or disable interrupt for TRIGGERED[3] event
					See EVENTS_TRIGGERED[3]
			Disabled	0	Disable
			Enabled	1	Enable
E	RW	TRIGGERED4			Enable or disable interrupt for TRIGGERED[4] event
					See EVENTS TRIGGERED[4]
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	TRIGGERED5	2.102.00	-	Enable or disable interrupt for TRIGGERED[5] event
			8: 11.1		See EVENTS_TRIGGERED[5]
			Disabled	0	Disable Enable
G	D\A/	TRIGGERED6	Enabled	1	Enable or disable interrupt for TRIGGERED[6] event
G	NVV	TRIGGEREDO			chable of disable interrupt for Trilogeneo(o) event
					See EVENTS_TRIGGERED[6]
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	TRIGGERED7			Enable or disable interrupt for TRIGGERED[7] event
					See EVENTS_TRIGGERED[7]
			Disabled	0	Disable



Bit r	numbe	er		31 30	29 2	28 2	7 26	25 2	4 2	3 22 21	1 2	0 19	18	3 17	16	5 15	14	4 1	13 1	2 1	1 1	0 9) 8	7	6	5 5	4	3	2	1	0
Id																Р	C)	N N	1	L K	(J	ı	Н	C	i F	Ε	D	С	В	Α
Res	et 0x0	0000000		0 0	0	0 0	0	0 0	0 0	0 0	0	0	0	0	0	0	0)	0 0) (0 0	0	0	0	c	0	0	0	0	0	0
Id	RW	Field	Value Id	Value					D	escript	tion	1																			
			Enabled	1					Er	nable																					
I	RW	TRIGGERED8							Er	nable o	or d	isab	le i	nte	rru	pt f	or '	TR	IGGI	ERI	D[8] ev	ven	t							
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[8]															
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
J	RW	TRIGGERED9							Er	nable o	or d	isab	le i	nte	rru	pt f	or '	TR	IGGI	ERE	D[9] ev	ven	t							
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[9]															
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
K	RW	TRIGGERED10							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGI	ERI	D[1	.0] 6	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[10]															
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
L	RW	TRIGGERED11							Er	nable o	or d	isab	le i	nte	rru	pt f	or '	TR	IGGI	ERI	D[1	.1] 6	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[11]	,														
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
M	RW	TRIGGERED12							Er	nable o	or d	isab	le i	nte	rru	pt f	or '	TR	IGGI	ERI	D[1	2] 6	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[12]															
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
N	RW	TRIGGERED13							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGI	ERI	D[1	.3] 6	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[13]	,														
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
0	RW	TRIGGERED14							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGI	ERI	D[1	4] 6	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[14]	,														
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
Р	RW	TRIGGERED15							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGI	ERI	D[1	.5] €	eve	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[15]															
			Disabled	0						isable																					
			Enabled	1					Er	nable																					

46.1.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	umbe	r		31	30 2	29	28	27	26 2	25 2	24 2	3 22	21	20	19 1	.8 1	7 1	6 1	5 1	4 1	3 12	11	10	9	8	7	6 5	4	3	2	1 0
Id																		F) (O N	I M	L	K	J	L	+ •	G F	Ε	D	С	ВА
Rese	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0 () () (0	0	0	0	0	0	0	0	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						0	escr	iptic	n																	
Α	RW	TRIGGERED0									٧	Vrite	'1' t	o E	nab	e in	ter	rup	t fo	r TF	IIGG	ERE	D[0] ev	ent						
											S	ee <i>E</i>	VEN	TS_	TRIC	GE	REL	0[0]													
			Set	1							Е	nabl	e																		
			Disabled	0							F	lead:	Disa	able	d																
			Enabled	1							F	lead:	Ena	ble	d																
В	RW	TRIGGERED1									٧	Vrite	'1' t	o E	nab	e in	ter	rup	t fo	r TF	RIGG	ERE	D[1] ev	ent						
											S	ee <i>E</i>	VEN	TS_	TRIC	GE	REL	[1]													
			Set	1							E	nabl	е																		



Bit r	number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 C
Id				P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW Field	Value Id	Value	Description
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW TRIGGERED2			Write '1' to Enable interrupt for TRIGGERED[2] event
				See EVENTS_TRIGGERED[2]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW TRIGGERED3			Write '1' to Enable interrupt for TRIGGERED[3] event
				See EVENTS_TRIGGERED[3]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW TRIGGERED4			Write '1' to Enable interrupt for TRIGGERED[4] event
		Cat	1	See EVENTS_TRIGGERED[4]
		Set Disabled	1	Enable Read: Disabled
		Enabled	1	Read: Enabled
F	RW TRIGGERED5	Enabled	1	Write '1' to Enable interrupt for TRIGGERED[5] event
'	NW TRIGGEREDS			Write 1 to thable interrupt for infludent D[5] event
				See EVENTS_TRIGGERED[5]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW TRIGGERED6			Write '1' to Enable interrupt for TRIGGERED[6] event
				See EVENTS_TRIGGERED[6]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW TRIGGERED7			Write '1' to Enable interrupt for TRIGGERED[7] event
				See EVENTS_TRIGGERED[7]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
ı	RW TRIGGERED8			Write '1' to Enable interrupt for TRIGGERED[8] event
				See EVENTS_TRIGGERED[8]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW TRIGGERED9			Write '1' to Enable interrupt for TRIGGERED[9] event
				, in the second
		C-t	1	See EVENTS_TRIGGERED[9] Enable
		Set	1	
		Disabled Enabled	0 1	Read: Disabled Read: Enabled
K	RW TRIGGERED10	Епаріец	1	Write '1' to Enable interrupt for TRIGGERED[10] event
IX.	WAS IMIGGEREDIO			
				See EVENTS_TRIGGERED[10]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW TRIGGERED11			Write '1' to Enable interrupt for TRIGGERED[11] event
				See EVENTS_TRIGGERED[11]
		Set	1	Enable
		Disabled	0	Read: Disabled



Bit r	numbe	er		31 30 29 28 27 26	5 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id						PONMLKJIHGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value		Description
			Enabled	1		Read: Enabled
М	RW	TRIGGERED12				Write '1' to Enable interrupt for TRIGGERED[12] event
						See EVENTS TRIGGERED[12]
			Set	1		Enable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
N	RW	TRIGGERED13				Write '1' to Enable interrupt for TRIGGERED[13] event
						See EVENTS TRIGGERED[13]
			Set	1		Enable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
0	R\M	TRIGGERED14	Lilableu	1		Write '1' to Enable interrupt for TRIGGERED[14] event
O	11.00	MIGGENEDIA				,
						See EVENTS_TRIGGERED[14]
			Set	1		Enable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
Р	RW	TRIGGERED15				Write '1' to Enable interrupt for TRIGGERED[15] event
						See EVENTS_TRIGGERED[15]
			Set	1		Enable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled

46.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit n	umbe	r		31 3	0 29	9 28	27 2	26 2	25 24	4 23	3 2	2 21	1 20	0 19	18	17	16	15	14	13	12 1	.1 10	9	8	7	6	5	4	3 2	1	0
Id																		Р	О	N	М	L K	J	1	Н	G	F	Е	D C	В	Α
Rese	t 0x0	0000000		0 (0 0	0	0	0 (0 0	0) (0 0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	e					D	esc	cript	ion																		
Α	RW	TRIGGERED0								W	۷rit	e '1'	to	Disa	able	int	errı	upt	for	TRI	GGE	RED	[0]	evei	nt						
										Se	ee L	EVEI	NTS	TR	IIGO	SERE	:D[01													
			Clear	1							isal			_			•	•													
			Disabled	0						Re	ead	d: Di	sab	led																	
			Enabled	1						Re	ead	d: En	nabl	led																	
В	RW	TRIGGERED1								W	Vrit	e '1'	to	Disa	able	int	errı	upt	for	TRI	GGE	RED	[1]	evei	nt						
										Se	ee L	EVEI	NTS	TR	IIGO	SERE	D[:	1]													
			Clear	1							isal			_			i														
			Disabled	0						Re	ead	d: Di	sab	led																	
			Enabled	1						Re	ead	d: En	nabl	led																	
С	RW	TRIGGERED2								W	۷rit	e '1'	to	Disa	able	int	errı	upt	for	TRI	GGE	RED	[2]	evei	nt						
										Se	ee L	EVEI	NTS	TR	IGO	SERE	D[.	2]													
			Clear	1							isal																				
			Disabled	0						Re	ead	d: Di	sab	led																	
			Enabled	1						Re	ead	d: En	nabl	led																	
D	RW	TRIGGERED3								W	Vrit	e '1'	to	Disa	able	int	errı	upt	for	TRI	GGE	RED	[3]	evei	nt						
										Se	ee L	EVEI	NTS	TR	IIGO	SERE	D[.	31													
			Clear	1						Di	isal	ble		_																	
			Disabled	0						Re	ead	d: Di	sab	led																	
			Enabled	1						Re	ead	d: En	nabl	led																	
Е	RW	TRIGGERED4								W	Vrit	e '1'	to	Disa	able	int	errı	upt	for	TRI	GGE	RED	[4]	evei	nt						



Bit r	numbe	er		31 30	29	28 2	7 26	25 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									PONMLKJIHGFEDCBA
		0000000			0	0 (0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value					Description
			Clear	1					See EVENTS_TRIGGERED[4] Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
F	RW	TRIGGERED5							Write '1' to Disable interrupt for TRIGGERED[5] event
			Clear	1					See EVENTS_TRIGGERED[5] Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
G	RW	TRIGGERED6							Write '1' to Disable interrupt for TRIGGERED[6] event
									See EVENTS_TRIGGERED[6]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
Н	RW	TRIGGERED7							Write '1' to Disable interrupt for TRIGGERED[7] event
									See EVENTS TRIGGERED[7]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
1	RW	TRIGGERED8							Write '1' to Disable interrupt for TRIGGERED[8] event
									SOO EVENTS TRICCEDEDIO
			Clear	1					See EVENTS_TRIGGERED[8] Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
J	RW	TRIGGERED9							Write '1' to Disable interrupt for TRIGGERED[9] event
									See EVENTS_TRIGGERED[9]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
K	RW	TRIGGERED10							Write '1' to Disable interrupt for TRIGGERED[10] event
									See EVENTS_TRIGGERED[10]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
L	RW	TRIGGERED11							Write '1' to Disable interrupt for TRIGGERED[11] event
									See EVENTS_TRIGGERED[11]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
М	RW	TRIGGERED12							Write '1' to Disable interrupt for TRIGGERED[12] event
									See EVENTS_TRIGGERED[12]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
N	RW	TRIGGERED13							Write '1' to Disable interrupt for TRIGGERED[13] event
									See EVENTS_TRIGGERED[13]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
0	RW	TRIGGERED14							Write '1' to Disable interrupt for TRIGGERED[14] event
									See EVENTS_TRIGGERED[14]



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			PONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
P RW TRIGGERED15			Write '1' to Disable interrupt for TRIGGERED[15] event
			See EVENTS_TRIGGERED[15]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

46.2 Electrical Specification

46.2.1 EGU Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{EGU,EVT}	Latency between setting an EGU event flag and the system		1		cycles
	setting an interrupt				



47 PWM — Pulse width modulation

The PWM module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

Three PWM modules can provide up to 12 PWM channels with individual frequency control in groups of up to four channels. Furthermore, a built-in decoder and EasyDMA capabilities make it possible to manipulate the PWM duty cycles without CPU intervention. Arbitrary duty-cycle sequences are read from Data RAM and can be chained to implement ping-pong buffering or repeated into complex loops.

Listed here are the main features of one PWM module:

- Fixed PWM base frequency with programmable clock divider
- Up to four PWM channels with individual polarity and duty-cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty-cycle arrays (sequences) defined in Data RAM
- · Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA
- · Change of polarity, duty-cycle, and base frequency possibly on every PWM period
- · Data RAM sequences can be repeated or connected into loops

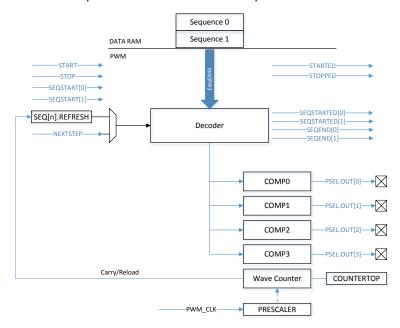


Figure 140: PWM Module

47.1 Wave counter

The wave counter is responsible for generating the pulses at a duty-cycle that depends on the compare values, and at a frequency that depends on COUNTERTOP.

There is one common 15-bit counter with four compare channels. Thus, all four channels will share the same period (PWM frequency), but can have individual duty-cycle and polarity. The polarity is set by the value read from RAM (see *Figure 143: Decoder memory access modes* on page 494), while the MODE register controls if the counter counts up, or up and down. The timer top value is controlled by the COUNTERTOP register. This register value in conjunction with the selected PRESCALER of the PWM_CLK will result in a given PWM period. A COUNTERTOP value smaller than the compare setting will result in a state where no PWM edges are generated. Respectively, OUT[n] is held high, given that the polarity is set to FallingEdge. All the compare registers are internal and can only be configured through the decoder presented later.

COUNTERTOP can be safely written at any time. It will get sampled following a START task. If DECODER.LOAD is anything else than WaveForm, it will also get sampled following a STARTSEQ[n] task,



and when loading a new value from RAM during a sequence playback. If DECODER.LOAD=WaveForm, the register value is ignored, and taken from RAM instead (see *Decoder with EasyDMA* on page 494 below).

Figure 141: PWM up counter example - FallingEdge polarity on page 492 shows the counter operating in up (MODE=PWM_MODE_Up) mode with three PWM channels with the same frequency but different duty cycle. The counter is automatically reset to zero when COUNTERTOP is reached and OUT[n] will invert. OUT[n] is held low if the compare value is 0 and held high respectively if set to COUNTERTOP given that the polarity is set to FallingEdge. Running in up counter mode will result in pulse widths that are edge-aligned. See the code example below:

```
uint16 t pwm seq[4] = {PWM CH0 DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
PWM CH3 DUTY);
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                        (PWM PSEL OUT CONNECT Connected <<
                                                  PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                        (PWM PSEL OUT CONNECT Connected <<
                                                 PWM_PSEL_OUT_CONNECT_Pos);
                      = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
NRF PWM0->ENABLE
NRF PWM0->MODE
                      = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->PRESCALER = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                  PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
NRF PWM0->LOOP
                    = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF PWM0->DECODER
                   = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos)
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF PWM0->SEQ[0].PTR = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(pwm seq) / sizeof(uint16_t)) < < 
                                                 PWM SEQ CNT CNT Pos);
NRF_PWM0 \rightarrow SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

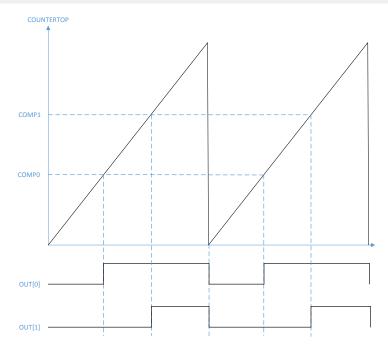


Figure 141: PWM up counter example - FallingEdge polarity

In up counting mode, the following formula can be used to compute PWM period and step size:

```
PWM period: T_{PWM}(Up) = T_{PWM} CLK * COUNTERTOP
```

Step width/Resolution: $T_{\text{steps}} = T_{\text{PWM_CLK}}$



Figure 142: PWM up-and-down counter example on page 493 shows the counter operating in up and down mode with (MODE=PWM_MODE_UpAndDown) two PWM channels with the same frequency but different duty cycle and output polarity. The counter starts decrementing to zero when COUNTERTOP is reached and will invert the OUT[n] when compare value is hit for the second time. This results in a set of pulses that are center- aligned.

```
uint16 t pwm seq[4] = {PWM CHO DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
 PWM CH3 DUTY);
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |</pre>
                                                                      (PWM PSEL OUT CONNECT Connected <<
                                                                                                                                              PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                                                                      (PWM PSEL OUT CONNECT Connected <<
                                                                                                                                             PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                                                               = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                                                               = (PWM MODE UPDOWN UpAndDown << PWM MODE UPDOWN Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                                                                                                             PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
                                                               = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF
          PWM0->LOOP
NRF PWM0->DECODER
                                                          = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos)
                                                               (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF_PWM0->SEQ[0].PTR = ((uint32_t)(pwm_seq) << PWM_SEQ PTR PTR Pos);
NRF_PWM0 - SEQ[0].CNT = ((sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(uint16_t)) < col
                                                                                                                                             PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0 \rightarrow SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

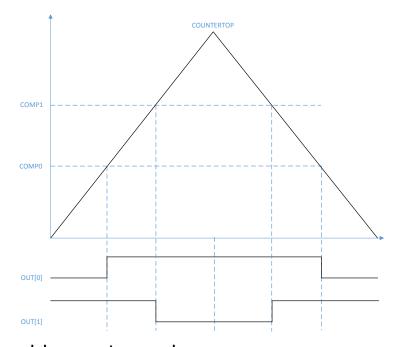


Figure 142: PWM up-and-down counter example

In up-and-down counting modes, the following formula can be used to compute PWM period and step size:

```
T_{PWM}(Up And Down) = T_{PWM} CLK * 2 * COUNTERTOP
```

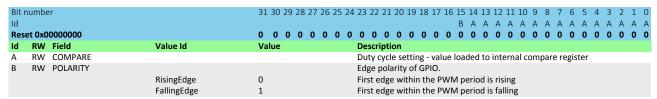
Step width/Resolution: $T_{steps} = T_{PWM CLK} * 2$



47.2 Decoder with EasyDMA

The decoder uses EasyDMA to take PWM parameters stored in Data RAM by ways of EasyDMA and updates the internal compare registers of the wave counter based on the mode of operation.

The mentioned PWM parameters are organized into a sequence containing at least one half word (16 bit). Its most significant bit[15] denotes the polarity of the OUT[n] while bit[14:0] is the 15-bit compare value. See below for further details of these RAM defined registers.



The DECODER register controls how the RAM content is interpreted and loaded to the internal compare registers. The LOAD field can be used to control if the RAM values are loaded to all compare channels - or alternatively to update a group or all channels with individual values. *Figure 143: Decoder memory access modes* on page 494 illustrates how the parameters stored in RAM are organized and routed to the various compare channels in the different modes.

A special mode of operation is available when DECODER.LOAD is set to WaveForm. In this mode, up to three PWM channels can be enabled - OUT[0] to OUT[2]. In RAM, four values are loaded at a time: the first, second and third location are used to load the values, and the fourth RAM location is used to load the COUNTERTOP register. This way one can have up to three PWM channels with a frequency base that changes on a per PWM period basis. This mode of operation is useful for arbitrary wave form generation in applications such as LED lighting.

The register SEQ[n].REFRESH=N (one per sequence n=0 or 1) will instruct a new RAM stored pulse width value on every (N+1)th PWM period. Setting the register to zero will result in a new duty cycle update every PWM period as long as the minimum PWM period is observed.

Note that registers SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored when DECODER.MODE=NextStep . The next value is loaded upon receiving every NEXTSTEP task.

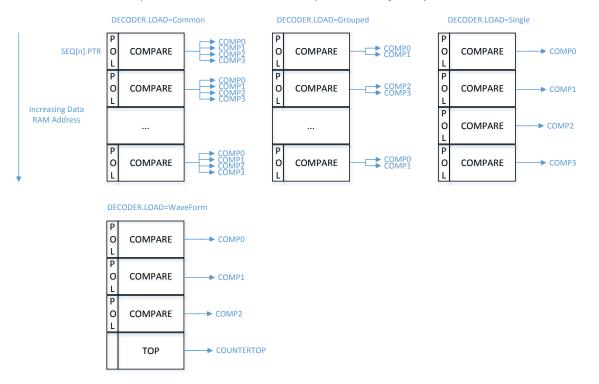


Figure 143: Decoder memory access modes



SEQ[n].PTR is the pointer used to fetch COMPARE values from RAM. If the SEQ[n].PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 20 for more information about the different memory regions.

After the SEQ[n].PTR is set to the desired RAM location, the SEQ[n].CNT register must be set to the number of 16-bit half words in the sequence. It is important to observe that the Grouped and Single modes require one half word per group or one half word per channel respectively, and thus increases RAM size occupation. If PWM generation was not running yet at that point, sending the SEQSTART[n] task will load the first value from RAM, then start the PWM generation. A SEQSTARTED[n] event is generated as soon as the EasyDMA has read the first PWM parameter from RAM and the wave counter has started executing it. When LOOP.CNT=0, sequence n=0 or 1 is played back once. After the last value in the sequence has been loaded and started executing, a SEQEND[n] event is generated. The PWM generation will then continue with the last loaded value. See *Figure 144: Simple sequence example* on page 496 for an example of such simple playback.

To completely stop the PWM generation and force the associated pins to a defined state, a STOP task can be fired at any time. A STOPPED event is generated when the PWM generation has stopped at the end of currently running PWM period, and the pins go into their idle state as defined in GPIO->OUT. PWM generation can then only be restarted through a SEQSTART[n] task. SEQSTART[n] will resume PWM generation after having loaded the first value from the RAM buffer defined in the SEQ[n].PTR register.

The table below provides indication of when specific registers get sampled by the hardware. Care should be taken when updating these registers to avoid values to be applied earlier than expected.

Table 112: When to safely update PWM registers

Register	Taken into account by hardware	Recommended (safe) update
SEQ[n].PTR	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[n].CNT	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[0].ENDDELAY	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the	When no more value from sequence [0] gets loaded from RAM (indicated by the SEQEND[0] event)
	PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].ENDDELAY	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the	When no more value from sequence [1] gets loaded from RAM (indicated by the SEQEND[1] event)
	PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
SEQ[0].REFRESH	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].REFRESH	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
COUNTERTOP	In DECODER.LOAD=WaveForm: this register is ignored.	Before starting PWM generation through a SEQSTART[n] task
	In all other LOAD modes: at the end of current PWM period (indicated by the PWMPERIODEND event)	After a STOP task has been issued, and the STOPPED event has been received.
MODE	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
DECODER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PRESCALER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
LOOP	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PSEL.OUT[n]	Immediately	Before enabling the PWM instance through the ENABLE register

Important: SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored at the end of a complex sequence, indicated by a LOOPSDONE event. The reason for this is that the last value loaded from RAM is maintained until further action from software (restarting a new sequence, or stopping PWM generation).



Figure 144: Simple sequence example on page 496 depicts the source code used for configuration and timing details in a sequence where only sequence 0 is used and only run once with a new PWM duty cycle for each period.

```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM_PSEL_OUT_PIN_Pos)
                           (PWM PSEL OUT CONNECT Connected <<
                                                      PWM PSEL OUT CONNECT Pos);
NRF_PWM0->ENABLE
                        = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                        = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                      PWM PRESCALER PRESCALER Pos);
NRF_PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec NRF_PWM0->LOOP = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF PWM0->DECODER
                      = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos)
                        (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(seq0 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(seq0 ram) / sizeof(\overline{uint16 t})) < \overline{<})
                                                      PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 0;
NRF PWM0->SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

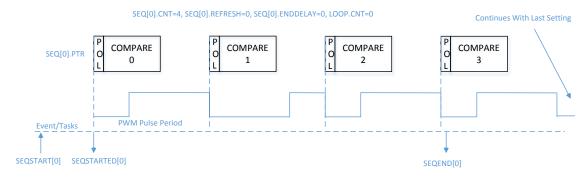


Figure 144: Simple sequence example

A more complex example is shown in *Figure 145: Example using two sequences* on page 497, where LOOP.CNT>0. In this case, an automated playback takes place, consisting of SEQ[0], delay 0, SEQ[1], delay 1, then again SEQ[0], etc. The user can choose to start a complex playback with SEQ[0] or SEQ[1] through sending the SEQSTART[0] or SEQSTART[1] task.

The complex playback always ends with delay 1.

The two sequences 0 and 1 are defined with address of values tables in Data RAM (pointed by SEQ[n].PTR) and respective buffer size (SEQ[n].CNT). The rate at which a new value is loaded is defined individually for each sequence by SEQ[n].REFRESH . The chaining of sequence 1 following sequence 0 is implicit, the LOOP.CNT register allows the chaining of sequence 1 to sequence 0 for a determined number of times. In other words, it allows to repeat a complex sequence a number of times in a fully automated way.

In the example below, sequence 0 is defined with SEQ[0].REFRESH set to one - that means that a new PWM duty cycle is pushed every second PWM period. This complex sequence is started with the SEQSTART[0] task, so SEQ[0] is played first. Since SEQ[0].ENDDELAY=1 there will be one PWM period delay between last period on sequence 0 and the first period on sequence 1. Since SEQ[1].ENDDELAY=0 there is no delay 1, so SEQ[0] would be started immediately after the end of SEQ[1]. However, as LOOP.CNT is one, the playback stops after having played only once SEQ[1], and both SEQEND[1] and LOOPSDONE are generated (their order is not guaranteed in this case).



```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                       (PWM PSEL OUT CONNECT Connected <<
                                              PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                    = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_
                    = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
   PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                              PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
                   = (1 \ll PWM LOOP CNT Pos);
NRF PWM0->LOOP
NRF PWM0->DECODER
                 = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos) |
                    (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(seq0 ram) << PWM SEQ PTR PTR Pos);
PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 1;
NRF PWM0->SEQ[0].ENDDELAY = 1;
NRF PWM0->SEQ[1].PTR = ((uint32 t)(seq1 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[1].CNT = ((sizeof(seq1 ram) / sizeof(uint16 t)) <<
                                              PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[1].REFRESH = 0;
NRF PWM0->SEQ[1].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

SEQ[0].CNT=2, SEQ[1].CNT=3, SEQ[0].REFRESH=1, SEQ[1].REFRESH=0, SEQ[0].ENDDELAY=1, SEQ[1].ENDDELAY=0, LOOP.CNT=1

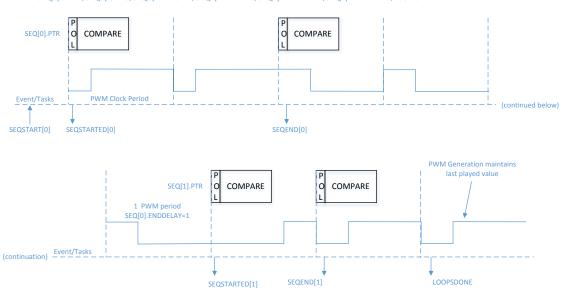


Figure 145: Example using two sequences

The decoder can also be configured to asynchronously load a new PWM duty cycle. If the DECODER.MODE register is set to NextStep - then the NEXTSTEP task will cause an update of the internal compare registers on the next PWM period.

The figures below provide an overview of each part of an arbitrary sequence, in various modes (LOOP.CNT=0 and LOOP.CNT>0). In particular are represented:

- Initial and final duty cycle on the PWM output(s)
- Chaining of SEQ[0] and SEQ[1] if LOOP.CNT>0
- · Influence of registers on the sequence
- Events fired during a sequence
- DMA activity (loading of next value and applying it to the output(s))

Note that the single-shot example applies also to SEQ[1], only SEQ[0] is represented for simplicity.



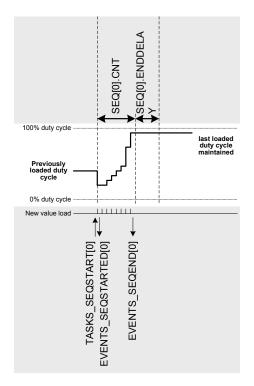


Figure 146: Single shot (LOOP.CNT=0)

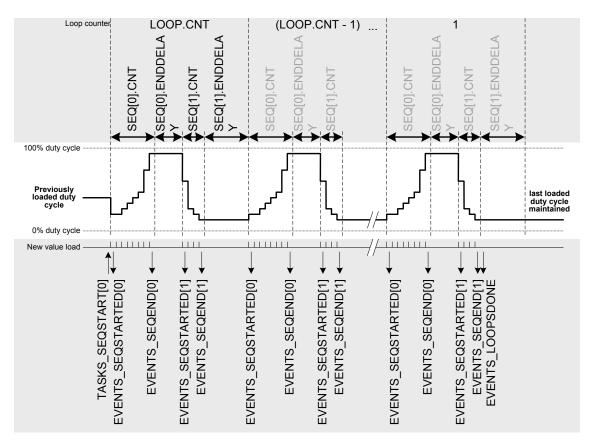


Figure 147: Complex sequence (LOOP.CNT>0) starting with SEQ[0]



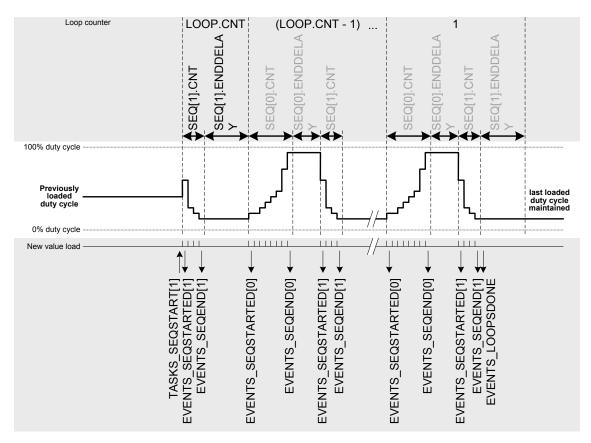


Figure 148: Complex sequence (LOOP.CNT>0) starting with SEQ[1]

Note that if a sequence is in use in a simple or complex sequence, it must have a length of SEQ[n].CNT > 0.

47.3 Limitations

The previous compare value will be repeated if the PWM period is selected to be shorter than the time it takes for the EasyDMA to fetch from RAM and update the internal compare registers.

This is to ensure a glitch-free operation even if very short PWM periods are chosen.

47.4 Pin configuration

The OUT[n] (n=0..3) signals associated to each channel of the PWM module are mapped to physical pins according to the configuration specified in the respective PSEL.OUT[n] registers. If a PSEL.OUT[n].CONNECT is set to Disconnected, the associated PWM module signal will not be connected to any physical pins.

The PSEL.OUT[n] registers and their configurations are only used as long as the PWM module is enabled and PWM generation is active (wave counter started), and retained only as long as the device is in System ON mode, see *POWER* chapter for more information about power modes.

To ensure correct behaviour in the PWM module, the pins used by the PWM module must be configured in the GPIO peripheral as described in *Table 113: Recommended GPIO configuration before starting PWM generation* on page 500 before enabling the PWM module. The pins' idle state is defined by the OUT registers in the GPIO module. This is to ensure that the pins used by the PWM module are driven correctly, if PWM generation is stopped through a STOP task, the PWM module itself is temporarily disabled, or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected IOs as long as the PWM module is supposed to be connected to an external PWM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.



Table 113: Recommended GPIO configuration before starting PWM generation

PWM signal	PWM pin	Direction	Output value	Comment
OUT[n]	As specified in PSEL.OUT[n]	Output	0	Idle state defined in GPIO->OUT
	(n=0, 3)			

47.5 Registers

Table 114: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x4001C000	PWM	PWM0	Pulse Width Modulation Unit 0		
0x40021000	PWM	PWM1	Pulse Width Modulation Unit 1		
0x40022000	PWM	PWM2	Pulse Width Modulation Unit 2		

Table 115: Register Overview

Register	Offset	Description
TASKS_STOP	0x004	Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence
		playback
TASKS_SEQSTART[0]	0x008	Loads the first PWM value on all enabled channels from sequence 0, and starts playing that
		sequence at the rate defined in SEQ[0]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_SEQSTART[1]	0x00C	Loads the first PWM value on all enabled channels from sequence 1, and starts playing that
		sequence at the rate defined in SEQ[1]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_NEXTSTEP	0x010	Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep.
		Does not cause PWM generation to start it was not running.
EVENTS_STOPPED	0x104	Response to STOP task, emitted when PWM pulses are no longer generated
EVENTS_SEQSTARTED[0	0] 0x108	First PWM period started on sequence 0
EVENTS_SEQSTARTED[1	1] 0x10C	First PWM period started on sequence 1
EVENTS_SEQEND[0]	0x110	Emitted at end of every sequence 0, when last value from RAM has been applied to wave counter
EVENTS_SEQEND[1]	0x114	Emitted at end of every sequence 1, when last value from RAM has been applied to wave counter
EVENTS_PWMPERIODE	N 0x118	Emitted at the end of each PWM period
EVENTS_LOOPSDONE	0x11C	Concatenated sequences have been played the amount of times defined in LOOP.CNT
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PWM module enable register
MODE	0x504	Selects operating mode of the wave counter
COUNTERTOP	0x508	Value up to which the pulse generator counter counts
PRESCALER	0x50C	Configuration for PWM_CLK
DECODER	0x510	Configuration of the decoder
LOOP	0x514	Amount of playback of a loop
SEQ[0].PTR	0x520	Beginning address in Data RAM of sequence A
SEQ[0].CNT	0x524	Amount of values (duty cycles) in sequence A
SEQ[0].REFRESH	0x528	Amount of additional PWM periods between samples loaded to compare register (load every CNT+1
		PWM periods)
SEQ[0].ENDDELAY	0x52C	Time added after the sequence
SEQ[1].PTR	0x540	Beginning address in Data RAM of sequence A
SEQ[1].CNT	0x544	Amount of values (duty cycles) in sequence A
SEQ[1].REFRESH	0x548	Amount of additional PWM periods between samples loaded to compare register (load every CNT+1
		PWM periods)
SEQ[1].ENDDELAY	0x54C	Time added after the sequence
PSEL.OUT[0]	0x560	Output pin select for PWM channel 0
PSEL.OUT[1]	0x564	Output pin select for PWM channel 1
PSEL.OUT[2]	0x568	Output pin select for PWM channel 2
PSEL.OUT[3]	0x56C	Output pin select for PWM channel 3



47.5.1 SHORTS

Address offset: 0x200 Shortcut register

Bit r	numbe	er		31	30	29	28 2	7 2	6 2	5 24	1 23	3 2	22 21	1 2	0 19	18	3 17	' 16	5 15	14	13	12	11	10	9	8 .	7 (5 5	4	3	2	1 0
Id																													Ε	D	С	ВА
Res	et 0x0	0000000		0	0	0	0 (0 (0 0	0	0) (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	es	cript	tion	1																	
Α	RW	SEQENDO_STOP									Sł	hoi	rtcut	t be	etwe	en	SEC	QEN	ID[C] ev	ent	an	d S	ГОР	tas	k						
											Se	ee	EVE	NTS	S_SE	QE	ND	[0]	and	TA	KS	_ST	OP									
			Disabled	0							Di	isa	ble	sho	rtcu	it																
			Enabled	1							Er	nal	ble s	hoi	rtcu	t																
В	RW	SEQEND1_STOP									Sł	hoi	rtcut	t be	etwe	en	SEC	QEN	ID[1] e	ent	an	d S	ГОР	tas	k						
											Se	ee	EVE	NTS	S_SE	QE	ND	[1]	and	TA:	KS	_ST	OP									
			Disabled	0							Di	isa	ble	sho	ortcu	it																
			Enabled	1							Er	nal	ble s	hoi	rtcu	t																
С	RW	LOOPSDONE_SEQSTARTO									Sł	hoi	rtcut	t be	etwe	en	LO	OPS	DO	NE	eve	nt a	ınd	SEQ	STA	ART[0] t	ask				
											Se	ee	EVE	NTS	S_LC	OOF	SDO	ONI	an	d T	4 <i>5K</i>	s_s	EQ.	STAI	RT[0]						
			Disabled	0							Di	isa	ble	sho	rtcu	it																
			Enabled	1							Er	nal	ble s	hoi	rtcu	t																
D	RW	LOOPSDONE_SEQSTART1									Sł	hoi	rtcut	t be	etwe	en	LO	OPS	DO	NE	eve	nt a	ınd	SEQ	STA	ART[1] t	ask				
											Se	ee	EVE	NTS	S_LC	OOF	SDO	ONI	an	d <i>T.</i>	4 <i>SK</i>	s_s	EQ.	STAI	RT[.	1]						
			Disabled	0							Di	isa	ble s	sho	rtcu	it																
			Enabled	1							Er	nal	ble s	hoi	rtcu	t																
Е	RW	LOOPSDONE_STOP									Sł	hoı	rtcut	t be	etwe	en	LO	OPS	DO	NE	eve	nt a	ınd	STO	P t	ask						
											Se	ee	EVE	NTS	S_LC	OOF	SDO	ONI	an	d T	4 <i>5K</i>	s_s	ΤΟΙ	D								
			Disabled	0							Di	isa	ble s	sho	rtcu	it																
			Enabled	1							Er	nal	ble s	hoi	rtcu	t																

47.5.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	numbe	er		31 3	30 29	28	27 :	26 2	5 24	23	22	21 2	0 1	9 18	3 17	16	15	14 1	.3 12	11	10	9	8 7	7 6	5	4	3	2 1	1 0
Id																							F	1 G	F	Ε	D	C E	3
Res	et 0x0	0000000		0	0 0	0	0	0 0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0	0 (0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Valu	ıe					Des	scrip	otio	n																
В	RW	STOPPED								Ena	able	or c	lisal	ble i	nter	rup	t for	ST	OPPE	D ev	/ent								
										۲.,	. FV	CNIT	.c. c.	TOD	חרח														
			a	_								ENT.	3_3	IUP	PED														
			Disabled	0						Disa																			
			Enabled	1						Ena	able																		
С	RW	SEQSTARTED0								Ena	able	or c	disab	ble i	nter	rup	t for	SE	QSTA	RTE	D[0]	ev	ent						
										See	e EV	ENT.	s si	EQS	TAR	TED	[0]												
			Disabled	0						Disa			_	-			,												
			Enabled	1						Ena																			
D	RW	SEQSTARTED1	Lilubica	-									lical	hlo i	ntor	run	t for	. CE/	QSTA	DTE	D[1]	ا مر	ont						
D	NVV	SEQSTANTEDI								LIId	ibie	OI C	ıısaı	oie i	iitei	rup	LIUI	3E	J317	INIE	ווט	ev	ent						
										See	e EV	ENT.	S_SI	EQS	TAR	TED	[1]												
			Disabled	0						Disa	able	ē																	
			Enabled	1						Ena	able																		
Ε	RW	SEQEND0								Ena	able	or c	disal	ble i	nter	rup	t for	SE	QENI	0[0]	eve	nt							
														-0-	NO.	01													
												ENT.	5_51	EQE	ND[UJ													
			Disabled	0						Disa																			
			Enabled	1						Ena	able																		
F	RW	SEQEND1								Ena	able	or c	disab	ble i	nter	rup	t for	SE	QENI	0[1]	eve	nt							



Bit	numbe	er		31	30 29	9 2	8 27	7 26	5 25	24	23 2	22 2	21 20	0 19	9 18	17	16	15	14 :	13 :	12 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																									Н	G	F	Ε	D	С	В
Res	et 0x0	0000000		0	0 0) (0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						Des	crip	otion																		
											See	EVI	ENTS	_SE	QEI	VD[1]														
			Disabled	0							Disa	ble	2																		
			Enabled	1							Ena	ble																			
G	RW	PWMPERIODEND									Ena	ble	or di	isab	ole ir	nter	rup	t fo	r PV	VM	PER	IODE	ND	eve	nt						
											See	EVI	ENTS	_ <i>P</i> I	WM	PER	IOD	ENI	D												
			Disabled	0							Disa	ble	9																		
			Enabled	1							Ena	ble																			
Н	RW	LOOPSDONE									Ena	ble	or di	isab	ole ir	nter	rup	t fo	r LO	OP	SDC	NE e	ven	t							
											See	EVI	ENTS		OOP.	SDC	NE														
			Disabled	0							Disa	ble	9																		
			Enabled	1							Ena	ble																			

47.5.3 INTENSET

Address offset: 0x304

Enable interrupt

Endoio intorrapt			
Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			H G F E D C B
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
B RW STOPPED			Write '1' to Enable interrupt for STOPPED event
			See EVENTS_STOPPED
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW SEQSTARTEDO			Write '1' to Enable interrupt for SEQSTARTED[0] event
			See EVENTS_SEQSTARTED[0]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW SEQSTARTED1			Write '1' to Enable interrupt for SEQSTARTED[1] event
			See EVENTS_SEQSTARTED[1]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW SEQENDO			Write '1' to Enable interrupt for SEQEND[0] event
			See EVENTS_SEQEND[0]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW SEQEND1			Write '1' to Enable interrupt for SEQEND[1] event
			See EVENTS_SEQEND[1]
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
G RW PWMPERIODEND			Write '1' to Enable interrupt for PWMPERIODEND event
			See EVENTS_PWMPERIODEND
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
H RW LOOPSDONE			Write '1' to Enable interrupt for LOOPSDONE event



Bit number		31 30 29 28 27 2	6 25 24	1 23 2	2 21	20 19	18	17 1	.6 15	14	13 1	2 11	10	9 8	7	6	5	4	3 2	2 1	0
Id															Н	G	F	Ε	D (В	
Reset 0x00000000		0 0 0 0 0	0 0 0	0	0 0	0 0	0	0	0 0	0	0 (0	0	0 0	0	0	0	0	0 (0	0
ld RW Field	Value Id	Value		Des	criptio	on															
				See	EVEN	TS_LC	OOPS	DON	IE												_
	Set	1		Enal	ble																
	Disabled	0		Read	d: Disa	abled															
	Enabled	1		Read	d: Ena	bled															

47.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	iidiiibe	-1		31 30 23 20 27 20 23	H G F E D C B
	et 0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
В		STOPPED			Write '1' to Disable interrupt for STOPPED event
					See EVENTS_STOPPED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	SEQSTARTED0			Write '1' to Disable interrupt for SEQSTARTED[0] event
					See EVENTS_SEQSTARTED[0]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	SEQSTARTED1			Write '1' to Disable interrupt for SEQSTARTED[1] event
					See EVENTS_SEQSTARTED[1]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Е	RW	SEQEND0			Write '1' to Disable interrupt for SEQEND[0] event
					See EVENTS_SEQEND[0]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	SEQEND1			Write '1' to Disable interrupt for SEQEND[1] event
					See EVENTS_SEQEND[1]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	PWMPERIODEND			Write '1' to Disable interrupt for PWMPERIODEND event
					See EVENTS_PWMPERIODEND
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	LOOPSDONE			Write '1' to Disable interrupt for LOOPSDONE event
					See EVENTS_LOOPSDONE
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

47.5.5 ENABLE

Address offset: 0x500



PWM module enable register

Bit	num	nbei	·		31 30	29	28	27	26	25	24	23	22	21	20	19	18 1	.7 1	16 1	15 3	L4 1	.3 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																																	Α
Res	et 0)x00	000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0 0
Id	R۱	w	Field	Value Id	Value	:						De	scri	ptic	on																		
Α	R۱	W	ENABLE									Ena	able	or	disa	able	PV	/M	mo	du	e												
				Disabled	0							Dis	able	ed																			
				Enabled	1							Ena	able	•																			

47.5.6 MODE

Address offset: 0x504

Selects operating mode of the wave counter

Bit r	iumbe	r		31 30	29	28	27	26 2	25 2	24 2	23 2	2 2	1 20	19	18	17	16	15	14 1	13 1	2 11	10	9	8	7	6	5	4	3 2	2 1	0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value	•						Desc	ript	tion																		
Α	RW	UPDOWN								S	Sele	cts ı	ир о	r up	an	d do	own	as	wav	e co	unt	er m	nod	e							
			Up	0						ι	Јр с	oun	iter	- ed	ge a	aligr	ned	PW	M c	luty	cycl	e									
			UpAndDown	1						ι	Јр а	nd	dow	n c	ount	ter-	- ce	nte	r ali	gne	l PW	M c	luty	су	cle						

47.5.7 COUNTERTOP

Address offset: 0x508

Value up to which the pulse generator counter counts

Bit	numb	er		31 30	29	28 2	7 26	25	24	23 2	22 2	1 20	19	18 :	17 :	16 :	15 1	4 1	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id																		A A	A	Α	Α	Α	Α	Α	Α	Α	A A	A	Α	Α
Res	et 0x0	000003FF		0 0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Value						Des	cript	tion																		
Α	RW	COUNTERTOP		[3327	767]]				Valu	ie up	o to	whi	ch th	ne p	ouls	e ge	ener	ator	coı	unte	er c	oun	ts.	This					
										regi	ster	is ig	nore	ed w	hei	n DI	ECO	DER	.MC	DDE	=Wa	ave	For	n a	nd c	only	,			
										بيامي	a. f.		RAN	A:	IJЬ															

47.5.8 PRESCALER

Address offset: 0x50C

Configuration for PWM_CLK

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		ААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PRESCALER		Pre-scaler of PWM_CLK
	DIV_1	0 Divide by 1 (16MHz)
	DIV_2	1 Divide by 2 (8MHz)
	DIV_4	2 Divide by 4 (4MHz)
	DIV_8	3 Divide by 8 (2MHz)
	DIV_16	4 Divide by 16 (1MHz)
	DIV_32	5 Divide by 32 (500kHz)
	DIV_64	6 Divide by 64 (250kHz)
	DIV_128	7 Divide by 128 (125kHz)

47.5.9 DECODER

Address offset: 0x510

Configuration of the decoder



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW LOAD			How a sequence is read from RAM and spread to the compare
			register
	Common	0	1st half word (16-bit) used in all PWM channels 03
	Grouped	1	1st half word (16-bit) used in channel 01; 2nd word in channel
			23
	Individual	2	1st half word (16-bit) in ch.0; 2nd in ch.1;; 4th in ch.3
	WaveForm	3	1st half word (16-bit) in ch.0; 2nd in ch.1;; 4th in
			COUNTERTOP
B RW MODE			Selects source for advancing the active sequence
	RefreshCount	0	SEQ[n].REFRESH is used to determine loading internal compare
			registers
	NextStep	1	NEXTSTEP task causes a new value to be loaded to internal
			compare registers

47.5.10 LOOP

Address offset: 0x514

Amount of playback of a loop

Bit	number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 1	6 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Id					A A A A A A A A A A A A A	Α
Res	et 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
Id	RW Field	Value Id	Value	Description		
Α	RW CNT			Amount of playback of p	attern cycles	
		Disabled	0	Looping disabled (stop a	t the end of the sequence)	

47.5.11 SEQ[0].PTR

Address offset: 0x520

Beginning address in Data RAM of sequence A

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Beginning address in Data RAM of sequence A

47.5.12 SEQ[0].CNT

Address offset: 0x524

Amount of values (duty cycles) in sequence A

Bitı	numbe	er		3:	1 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 :	l6 1	.5 1	.4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																					Α,	Δ ,	۱ ۸	A A	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0 () (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	2						De	scri	ptic	n																		
Α	RW	CNT										Am	our	nt o	f va	lue	s (d	uty	сус	les) in	seq	uer	ice /	4								
			Disabled	0								Sec	quei	nce	is c	lisal	bled	l, aı	nd s	hal	l no	t b	e st	arte	d as	it i	s er	npt	у				

47.5.13 SEQ[0].REFRESH

Address offset: 0x528

Amount of additional PWM periods between samples loaded to compare register (load every CNT+1 PWM periods)



Bit r	numb	er		31 30	29	28	27	26	25	24	23	22 :	21 2	0 1	9 18	17	16	15	14	13 1	2 1	l 10	9	8	7	6	5	4	3	2 1	. 0
Id											Α	Α	Α /	4 Δ	A A	Α	Α	Α	Α	Α /	4 Α	Α.	Α	Α	Α	Α	Α	Α	Α .	A A	АА
Res	et Ox	0000001		0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0	1
Id	RW	Field	Value Id	Value	:						Des	crip	otio	n																	
Α	RW	CNT									Am	oun	nt of	ado	ditio	nal	PW	Μŗ	erio	ods b	etw	een	san	nple	es lo	oad	ed '	to			,
											con	npa	re re	egist	ter (load	d ev	ery	CN	T+1 I	PWN	∕l pe	rioc	ls)							
			Continuous	0							Upo	date	e eve	ery F	PWN	Л ре	erio	d													

47.5.14 SEQ[0].ENDDELAY

Address offset: 0x52C

Time added after the sequence

Bit n	umb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Rese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α	RW	CNT										Tin	ne a	dd	ed a	afte	r th	ne s	eau	ien	ce i	n P	W١	1 pe	erio	ds									7

47.5.15 SEQ[1].PTR

Address offset: 0x540

Beginning address in Data RAM of sequence A

Bit number	31 30 29	9 28 27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id	A A A	A A A A A A A A	A A A A A A A A	A A A A A A A A
Reset 0x00000000	0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field Value I	d Value	Description		
A RW PTR		Beginning ac	Idress in Data RAM of sequence A	1

47.5.16 SEQ[1].CNT

Address offset: 0x544

Amount of values (duty cycles) in sequence A

Bitı	numb	er		31	. 30	29	28	27 2	6 2	25 2	24 2	23 2	22 2	21 2	20 2	19 1	18 2	17 1	.6 1	L5 1	4 1	13	12	11	10	9	8	7	6	5	4	3 2	2	L 0
Id																					Д	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	A A
Res	et 0x(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tio	n																			
Α	RW	CNT									,	٩m٥	oun	t of	va	lues	s (d	uty	сус	les) in	se	que	nc	e A									
			Disabled	0							9	Seq	uen	ce	is d	isak	olec	l, ar	nd s	hal	Ind	ot k	e s	tar	ted	as	it is	en	npty	/				

47.5.17 SEQ[1].REFRESH

Address offset: 0x548

Amount of additional PWM periods between samples loaded to compare register (load every CNT+1 PWM periods)

Bit	numb	er		31 30	29	28	27	26	25	24	23	22	21	20	19 1	8 1	7 16	5 15	14	13	12 1	1 10	9	8	7	6	5	4	3	2 1	. 0
Id											Α	Α	Α	Α	Α .	A A	A	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	Α	4 Α	AA
Res	et 0x	0000001		0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	1
Id	RW	Field	Value Id	Value							De	scri	ptic	n																	
Α	RW	CNT									Αn	nou	nt o	f ad	lditi	ona	PW	/M p	oerio	ods	betv	veen	san	nple	es lo	oad	ed '	to			
											coı	mpa	are i	egi	ster	(loa	d e	very	CN	T+1	PW	И ре	rio	ds)							
			Continuous	0							Up	dat	e ev	ery	PW	/M p	erio	d													

47.5.18 SEQ[1].ENDDELAY

Address offset: 0x54C

Time added after the sequence



Bit r	iumbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	LO	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	Α	Α.	A ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	CNT										Tin	ne a	dd	ed a	afte	r th	ie s	equ	ien	ce i	n P	٨N	l pe	rioc	ls								

47.5.19 PSEL.OUT[0]

Address offset: 0x560

Output pin select for PWM channel 0

Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

47.5.20 PSEL.OUT[1]

Address offset: 0x564

Output pin select for PWM channel 1

Bitı	numbe	r		31 30 29 28 27 26 2	5 24	23 2	22 2	1 20	19	18 3	17 16	5 15	14 :	13 12	11	10 9	9 8	7	6	5	4	3 2	1	0
Id				С																	Α	А А	A	Α
Res	et OxF	FFFFFF		1 1 1 1 1 1 1	. 1	1	1 1	l 1	1	1	1 1	. 1	1	1 1	1	1	l 1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Value		Des	crip	tion																
Α	RW	PIN		[031]		Pin	num	ber																
С	RW	CONNECT				Con	nect	tion																
			Disconnected	1		Disc	onn	ect																
			Connected	0		Con	nect	t																

47.5.21 PSEL.OUT[2]

Address offset: 0x568

Output pin select for PWM channel 2

Bi	numb	er		31 30 29 28 27 26	25 24	4 23	22 21	20	19	18 1	7 16	15	14 1	3 12	11 10	9	8	7	6	5 4	3	2	1 0
Id				С																Α	Α	Α	A A
Re	set 0x	FFFFFFF		1 1 1 1 1 1	1 1	. 1	1 1	1	1	1 1	. 1	1	1 1	. 1	1 1	1	1	1	1	1 1	1	1	1 1
Id	RW	/ Field	Value Id	Value		De	script	ion															
Α	RW	PIN		[031]		Pin	numl	ber															
С	RW	CONNECT				Cor	nnecti	ion															
			Disconnected	1		Dis	conne	ect															
			Connected	0		Cor	nnect																

47.5.22 PSEL.OUT[3]

Address offset: 0x56C

Output pin select for PWM channel 3

Bit r	numbe	er		31	. 30	29	28	27	26	25 2	24 2	23 2	2 21	20	19	18	17 :	16 1	5 1	4 13	12	11	10 9	9 8	7	6	5	4	3 2	2 1	0
Id				С																								Α	A A	A A	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1 :	1 1	1	1	1 :	L 1	. 1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue						ı	Desc	ript	ion																	
Α	RW	PIN		[0	31]					F	Pin r	uml	ber																	
С	RW	CONNECT									(Conr	ect	ion																	
			Disconnected	1							ı	Disco	onne	ect																	



Bit number	31 30 29 2	28 27 26 25 24 23 22 21 20 :	19 18 17 16 15 14 13 12 11	. 10 9 8 7 6 5 4 3 2 1 0
Id	С			AAAAA
Reset 0xFFFFFFF	1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	l Value	Description		
Connec	ted 0	Connect		

47.6 Electrical Specification

47.6.1 PWM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PWM,16MHz}	PWM run current, Prescaler set to DIV_1 (16 MHz), excluding		200		μΑ
	DMA and GPIO				
I _{PWM,8MHz}	PWM run current, Prescaler set to DIV_2 (8 MHz), excluding		150		μΑ
	DMA and GPIO				
I _{PWM,125kHz}	PWM run current, Prescaler set to DIV_128 (125 kHz), excluding		150		μΑ
	DMA and GPIO				



48 SPI — Serial peripheral interface master

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. This section is added for legacy support for now.

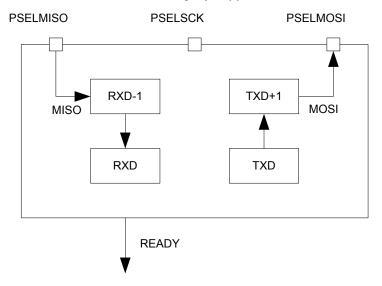


Figure 149: SPI master

RXD-1 and TXD+1 illustrate the double buffered version of RXD and TXD respectively.

48.1 Functional description

The TXD and RXD registers are double-buffered to enable some degree of uninterrupted data flow in and out of the SPI master.

The SPI master does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPI master supports SPI modes 0 through 3.

Table 116: SPI modes

Mode	Clock polarity	Clock phase
	CPOL	СРНА
SPI_MODE	0 (Leading)	0 (Active High)
SPI_MODE	0 (Leading)	1 (Active Low)
SPI_MODE	1 (Trailing)	0 (Active High)
SPI_MODE	1 (Trailing)	1 (Active Low)

48.1.1 SPI master mode pin configuration

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins.

This mapping is according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If a value of 0xFFFFFFFF is specified in any of these registers, the associated SPI master signal is not connected to any physical pin. The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 117: GPIO configuration* on page 510 prior to enabling the SPI. The SCK must always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.



Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 117: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value
SCK	As specified in PSEL.SCK	Output	Same as CONFIG.CPOL
MOSI	As specified in PSEL.MOSI	Output	0
MISO	As specified in PSEL.MISO	Input	Not applicable

48.1.2 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

48.1.3 SPI master transaction sequence

An SPI master transaction is started by writing the first byte, which is to be transmitted by the SPI master, to the TXD register.

Since the transmitter is double buffered, the second byte can be written to the TXD register immediately after the first one. The SPI master will then send these bytes in the order they are written to the TXD register.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 150: SPI master transaction* on page 511. Bytes that are received will be moved to the RXD register where the CPU can extract them by reading the register. The RXD register is double buffered in the same way as the TXD register, and a second byte can therefore be received at the same time as the first byte is being extracted from RXD by the CPU. The SPI master will generate a READY event every time a new byte is moved to the RXD register. The double buffered byte will be moved from RXD-1 to RXD as soon as the first byte is extracted from RXD. The SPI master will stop when there are no more bytes to send in TXD and TXD+1.



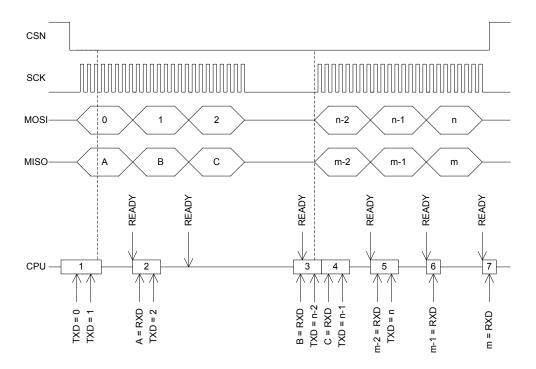


Figure 150: SPI master transaction

The READY event of the third byte transaction is delayed until B is extracted from RXD in occurrence number 3 on the horizontal lifeline. The reason for this is that the third event is generated first when C is moved from RXD-1 to RXD after B is read.

The SPI master will move the incoming byte to the RXD register after a short delay following the SCK clock period of the last bit in the byte. This also means that the READY event will be delayed accordingly, see *Figure 151: SPI master transaction* on page 511. Therefore, it is important that you always clear the READY event, even if the RXD register and the data that is being received is not used.

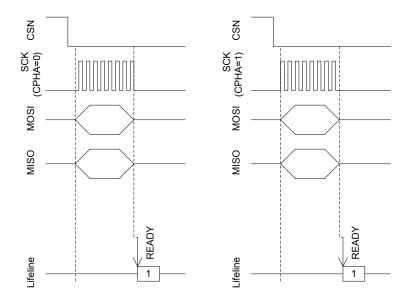


Figure 151: SPI master transaction



48.2 Registers

Table 118: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPI	SPI0	SPI master 0		Deprecated
0x40004000	SPI	SPI1	SPI master 1		Deprecated
0x40023000	SPI	SPI2	SPI master 2.		Deprecated

Table 119: Register Overview

Register	Offset	Description
EVENTS_READY	0x108	TXD byte sent and RXD byte received
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPI
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI
PSEL.MISO	0x510	Pin select for MISO
RXD	0x518	RXD register
TXD	0x51C	TXD register
FREQUENCY	0x524	SPI frequency
CONFIG	0x554	Configuration register

48.2.1 INTENSET

Address offset: 0x304

Enable interrupt

Bitı	numbe	er		31	30 2	29	28	27	26	25	24	23	22	21	20	19	18	3 17	7 16	5 15	5 14	1 13	3 12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																	Α		
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Val	ue							De	escr	ipti	on																				
Α	RW	READY										W	rite	'1'	to I	Ena	ble	int	terr	upt	fo	RE	AD'	Y ev	ent										
												Se	e <i>E</i>	VΕN	ITS_	_RE	AD	Υ																	
			Set	1								En	abl	e																					
			Disabled	0								Re	ad:	Dis	abl	led																			
			Enabled	1								Re	ad:	Ena	able	ed																			

48.2.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	numbe	er		31	30	29	28	27	7 26	5 25	5 24	1 2	3 2	2 2	1 2	0 1	19 1	18	17	16	15	14	- 13	3 1	2 1	1 1	0 9	9 (3 7	7	6	5	4	3	2	1	0
Id																																			Α		
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0) (0) () (0	0	0	0	0	0	0	C) () () () () () (0	0	0	0	0	0	O
Id	RW	Field	Value Id	Va	lue							D	esc	ript	tior	1																					
Α	RW	READY										W	/rit	e '1	' to	Di	sab	le	int	err	upt	fo	r RI	ΑI	OY (eve	nt										
												Se	ee <i>l</i>	EVE	NT.	S_ <i>F</i>	REA	DΥ	,																		
			Clear	1								D	isal	ole																							
			Disabled	0								R	ead	l: Di	isal	ole	d																				
			Enabled	1								R	ead	l: Er	nab	led	ł																				

48.2.3 ENABLE

Address offset: 0x500

Enable SPI



Bitı	numbe	er		31 3	30 29	9 28	3 27	26	25	24	23	22	21	20 1	L9 1	8 1	7 1	5 15	14	13	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																													Α	Α.	А А
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						De	scri	ptic	on																	
Α	RW	ENABLE									Ena	able	e or	disa	ble	SPI															
			Disabled	0							Dis	abl	e SF	Pl																	
			Enabled	1							Ena	able	s SP	I																	

48.2.4 PSEL.SCK

Address offset: 0x508 Pin select for SCK

Bit	nu	ımb	er		31	1 30	29	9 2	8 2	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id					Α	Α	Α	. /	Δ.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	А
Res	set	Oxl	FFFFFFF		1	1	1	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. 1
Id		RW	Field	Value Id	Va	alue	•							De	scri	ptic	on														6 5 4 3 2 1 A A A A A A 1 1 1 1 1 1					
Α		RW	PSELSCK		[0	31	.]							Pin	nu	mb	er c	onf	igu	rati	ion	for	SP	I SC	K si	gna	al	A A . 1 1								
				Disconnected	0х	FFF	FFF	FFF	=					Dis	con	ne	ct																			

48.2.5 PSEL.MOSI

Address offset: 0x50C Pin select for MOSI

Bit r	numb	er		31	1 30	29	28	3 27	7 26	25	24	23	22	21	20 1	19 1	l8 1	7 1	6 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	Α	A .	A A	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	A	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	n																		
Α	RW	PSELMOSI		[0	31	.]						Pin	nu	mbe	er c	onfi	gura	atio	n fo	r SP	I M	OSI	sigr	nal									
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	:t																		

48.2.6 PSEL.MISO

Address offset: 0x510 Pin select for MISO

Bit r	numbe	er		31	. 30	29	28	3 2	7 26	5 2	5 24	1 23	3 2:	2 21	1 2	0 19	18	8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Δ	A	. 4	4 A	. A		A A	. 4	A	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	ı
Res	et OxF	FFFFFF		1	1	1	1	1	. 1	1	1 1	. 1	. 1	1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	l
Id	RW	Field	Value Id	Va	lue							D	esc	ript	ior	١																			
Α	RW	PSELMISO		[0.	31]						Pi	in n	um	bei	cor	nfig	gura	tior	ı fo	r SP	ΙM	ISO	sig (gnal										
			Disconnected	0x	FFF	FFF	FF					Di	isco	onne	ect																				

48.2.7 RXD

Address offset: 0x518

RXD register

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18	17 16 15 14 13 12 11 10 9	9 8 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x0000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A R RXD			RX data received. D	ouble buffered	

48.2.8 TXD

Address offset: 0x51C

TXD register



Bit r	numbe	er		31	30	29	28 2	7 20	5 25	5 24	4 23	3 22	21	20	19	18	17	16	15 :	14 1	.3 1	2 1:	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																										Α	Α	Α	Α	A A	4 Δ	A A
Res	et 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																		
Α	RW	TXD									T)	〈 da	ta to	se	nd.	Do	uble	e bı	ıffe	red												

48.2.9 FREQUENCY

Address offset: 0x524

SPI frequency

Bit number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0x04000000		0 0 0 0 0 1 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
ld RW Field	Value Id	Value	Description
A RW FREQUENCY			SPI master data rate
	K125	0x02000000	125 kbps
	K250	0x04000000	250 kbps
	K500	0x08000000	500 kbps
	M1	0x10000000	1 Mbps
	M2	0x20000000	2 Mbps
	M4	0x40000000	4 Mbps
	M8	0x80000000	8 Mbps

48.2.10 CONFIG

Address offset: 0x554 Configuration register

Bit r	iumbe	r		31	30 2	9 2	8 27	7 26	25	24	23 2	22 2	21 2	0 1	9 18	8 1	7 16	5 15	5 14	1 13	12	11	10	9	8 7	6	5	4	3	2	1 ()
Id																														С	В	l
Rese	et 0x0	0000000		0	0 0) (0 0	0	0	0	0 (0	0 0) (0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (
Id	RW	Field	Value Id	Val	lue						Desc	crip	tion	١																		
Α	RW	ORDER									Bit o	orde	er																			
			MsbFirst	0							Mos	t si	gnifi	icar	nt b	it sl	hifte	ed o	out	first												
			LsbFirst	1							Leas	t si	gnif	icar	nt b	it sl	hifte	ed o	out	first												
В	RW	СРНА									Seria	al c	lock	(SC	CK) p	pha	se															
			Leading	0							Sam	ple	on	lead	ding	g ed	lge (of c	loc	k, sh	ift s	eria	al da	ta (on ti	aili	ng					
											edge	е																				
			Trailing	1							Sam	ple	on	trai	ling	ed	ge c	of c	lock	k, sh	ift s	eria	l da	ta c	n le	adi	ng					
											edge	е																				
С	RW	CPOL									Seria	al c	lock	(SC	CK) p	pola	arity	,														
			ActiveHigh	0							Activ	ve l	nigh																			
			ActiveLow	1							Activ	ve I	ow																			

48.3 Electrical Specification

48.3.1 SPI master interface

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPI}	Bit rates for SPI ³⁹			8 ⁴⁰	Mbps
I _{SPI,2Mbps}	Run current for SPI, 2 Mbps			50	μΑ
I _{SPI,8Mbps}	Run current for SPI, 8 Mbps			50	μΑ
I _{SPI,IDLE}	Idle current for SPI (STARTed, no CSN activity)		<1		μΑ

Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.



Symbol	Description	Min.	Тур.	Max.	Units
t _{SPI,START,LP}	Time from writing TXD register to transmission started, low		t _{SPI,STAR}	г,сі	μs
	power mode		+		
			t _{START_H}	FIN	
t _{SPI,START,CL}	Time from writing TXD register to transmission started, constant		1		μs
	latency mode				

48.3.2 Serial Peripheral Interface (SPI) Master timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPI,CSCK,8Mbps}	SCK period at 8Mbps		125		ns
t _{SPI,CSCK,4Mbps}	SCK period at 4Mbps		250		ns
t _{SPI,CSCK,2Mbps}	SCK period at 2Mbps		500		ns
t _{SPI,RSCK,LD}	SCK rise time, low drive ^a			t _{RF,25pF}	
t _{SPI,RSCK,HD}	SCK rise time, high drive ^a			t _{HRF,25pF}	
t _{SPI,FSCK,LD}	SCK fall time, low drive ^a			t _{RF,25pF}	
t _{SPI,FSCK,HD}	SCK fall time, high drive ^a			t _{HRF,25pF}	
t _{SPI,WHSCK}	SCK high time ^a	(0.5*t _{CS}	ск]		
		– t _{RSCK}			
t _{SPI,WLSCK}	SCK low time ^a	(0.5*t _{CS}	ск)		
		– t _{FSCK}			
t _{SPI,SUMI}	MISO to CLK edge setup time	19			ns
t _{SPI,HMI}	CLK edge to MISO hold time	18			ns
t _{SPI,VMO}	CLK edge to MOSI valid			59	ns
t _{SPI.HMO}	MOSI hold time after CLK edge	20			ns

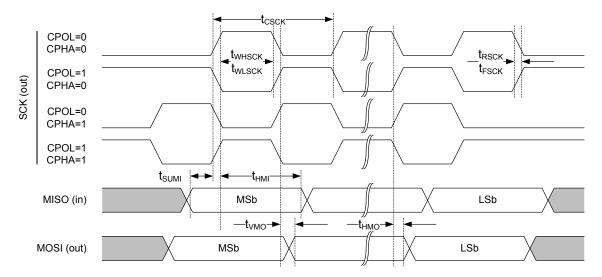


Figure 152: SPI master timing diagram

 $^{^{\}rm a}~{\rm At}~25{\rm pF}$ load, including GPIO capacitance, see GPIO spec.



49 TWI — I²C compatible two-wire interface

The TWI master is compatible with I²C operating at 100 kHz and 400 kHz.

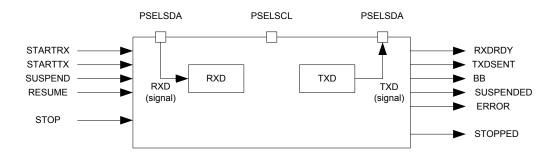


Figure 153: TWI master's main features

49.1 Functional description

This TWI master is not compatible with CBUS. The TWI transmitter and receiver are single buffered.

See, Figure 153: TWI master's main features on page 516.

A TWI setup comprising one master and three slaves is illustrated in *Figure 154: A typical TWI setup comprising one master and three slaves* on page 516. This TWI master is only able to operate as the only master on the TWI bus.

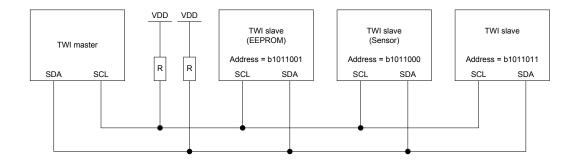


Figure 154: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

49.2 Master mode pin configuration

The different signals SCL and SDA associated with the TWI master are mapped to physical pins according to the configuration specified in the PSELSCL and PSELSDA registers respectively.

If a value of 0xFFFFFFF is specified in any of these registers, the associated TWI master signal is not connected to any physical pin. The PSELSCL and PSELSDA registers and their configurations are only used



as long as the TWI master is enabled, and retained only as long as the device is in ON mode. PSELSCL and PSELSDA must only be configured when the TWI is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 120: GPIO configuration* on page 517.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 120: GPIO configuration

TWI master signal	TWI master pin	Direction	Drive strength	Output value
SCL	As specified in PSELSCL	Input	SOD1	Not applicable
SDA	As specified in PSELSDA	Input	SOD1	Not applicable

49.3 Shared resources

The TWI shares registers and other resources with other peripherals that have the same ID as the TWI.

Therefore, you must disable all peripherals that have the same ID as the TWI before the TWI can be configured and used. Disabling a peripheral that has the same ID as the TWI will not reset any of the registers that are shared with the TWI. It is therefore important to configure all relevant TWI registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 21 shows which peripherals have the same ID as the TWI.

49.4 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes that are written to the TXD register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave. A TXDSENT event will be generated each time the TWI master has clocked out a TXD byte, and the associated ACK/NACK bit has been clocked in from the slave.

The TWI master transmitter is single buffered, and a second byte can only be written to the TXD register after the previous byte has been clocked out and the ACK/NACK bit clocked in, that is, after the TXDSENT event has been generated.

If the CPU is prevented from writing to TXD when the TWI master is ready to clock out a byte, the TWI master will stretch the clock until the CPU has written a byte to the TXD register.

A typical TWI master write sequence is illustrated in *Figure 155: The TWI master writing data to a slave* on page 518. Occurrence 3 in the figure illustrates delayed processing of the TXDSENT event associated with TXD byte 1. In this scenario the TWI master will stretch the clock to prevent writing erroneous data to the slave.



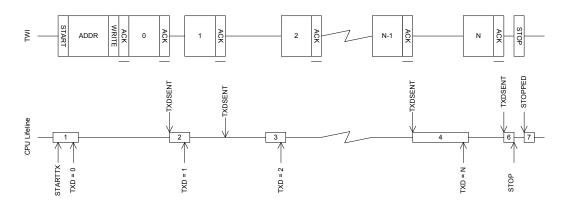


Figure 155: The TWI master writing data to a slave

The TWI master write sequence is stopped when the STOP task is triggered whereupon the TWI master will generate a stop condition on the TWI bus.

49.5 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1).

The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

The TWI master will generate a RXDRDY event every time a new byte is received in the RXD register.

After receiving a byte, the TWI master will delay sending the ACK/NACK bit by stretching the clock until the CPU has extracted the received byte, that is, by reading the RXD register.

The TWI master read sequence is stopped by triggering the STOP task. This task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the stop condition.

A typical TWI master read sequence is illustrated in *Figure 156: The TWI master reading data from a slave* on page 519. Occurrence 3 in this figure illustrates delayed processing of the RXDRDY event associated with RXD byte B. In this scenario the TWI master will stretch the clock to prevent the slave from overwriting the contents of the RXD register.



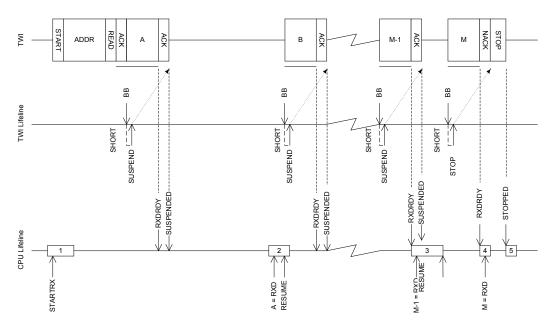


Figure 156: The TWI master reading data from a slave

49.6 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes one byte to the slave followed by reading M bytes from the slave. Any combination and number of transmit and receive sequences can be combined in this fashion. Only one shortcut to STOP can be enabled at any given time.

The figure below illustrates a repeated start sequence where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between.

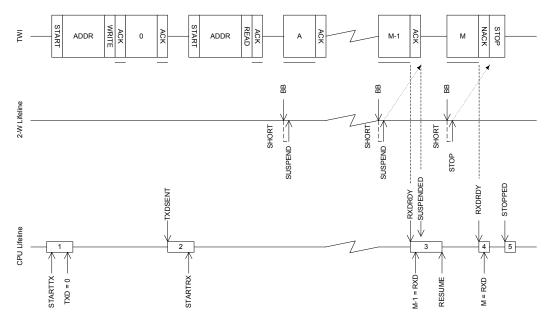


Figure 157: A repeated start sequence, where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between

To generate a repeated start after a read sequence, a second start task must be triggered instead of the STOP task, that is, STARTRX or STARTTX. This start task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the repeated start condition.



49.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

49.8 Registers

Table 121: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	TWI	TWI0	Two-wire interface master 0		Deprecated
0x40004000	TWI	TWI1	Two-wire interface master 1		Deprecated

Table 122: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_RXDREADY	0x108	TWI RXD byte received
EVENTS_TXDSENT	0x11C	TWI TXD byte sent
EVENTS_ERROR	0x124	TWI error
EVENTS_BB	0x138	TWI byte boundary, generated before each byte that is sent or received
EVENTS_SUSPENDED	0x148	TWI entered the suspended state
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWI
PSELSCL	0x508	Pin select for SCL
PSELSDA	0x50C	Pin select for SDA
RXD	0x518	RXD register
TXD	0x51C	TXD register
FREQUENCY	0x524	TWI frequency
ADDRESS	0x588	Address used in the TWI transfer

49.8.1 SHORTS

Shortcut register

Address offset: 0x200

Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Id ВА Reset 0x00000000 ld RW Field Value Id Value Description RW BB_SUSPEND Shortcut between BB event and SUSPEND task See EVENTS_BB and TASKS_SUSPEND Disabled 0 Disable shortcut Enabled 1 **Enable shortcut** B RW BB_STOP Shortcut between BB event and STOP task



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_BB and TASKS_STOP
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

49.8.2 INTENSET

Address offset: 0x304

Enable interrupt

Enable interrupt																									
Bit number		31 30	29 2	8 27	26 2	25 24	23	3 22 21 2	0 19 :	18	17 :	16	15	14	13 1	2 1	.1 10	9	8	7	6	5 4	1 3	2	1 (
Id										F				Ε				D		С				В	Α
Reset 0x00000000		0 0	0 (0	0	0 0	0	0 0 0	0	0	0	0	0	0	0 ()	0 0	0	0	0	0	0 (0	0	0 (
Id RW Field	Value Id	Value					De	escription)																
A RW STOPPED							W	rite '1' to	Enab	le i	nte	rru	pt f	or S	TOP	PE	D ev	ent							
							Se	e <i>EVENT</i>	STO)PP	ED														
	Set	1					En	able																	
	Disabled	0					Re	ad: Disak	led																
	Enabled	1					Re	ad: Enab	led																
B RW RXDREADY							W	rite '1' to	Enab	le i	nte	rru	pt f	or F	RXDF	REA	DY e	ven	t						
							Se	e <i>EVENT</i> S	S RXI	ORF	ΔΩ\	,													
	Set	1						iable																	
	Disabled	0						ad: Disak	oled																
	Enabled	1						ad: Enab																	
C RW TXDSENT							W	rite '1' to	Enab	le i	nte	rruj	ot f	or 1	XDS	ΕN	T ev	ent							
							۲.	o EVENT	TVE)CE	NIT														
	Set	1						e <i>EVENT</i> : iable	_	JSE	IVI														
	Disabled	0						ad: Disak	hal																
	Enabled	1						ad: Enab																	
D RW ERROR	2.100.00	-						rite '1' to		le i	nte	rrui	ot fo	or E	RRC)R e	even	t							
								e <i>EVENT</i>	S_ERR	ROR	?														
	Set	1						able																	
	Disabled	0						ead: Disak																	
E RW BB	Enabled	1						ad: Enab rite '1' to		ıla i	nto	· · · · ·	at f	or E	DD O	,on									
E RVV DD							VV	iite I to	LIIAU	ne i	me	iiu	pt II	ם וט	ים פנ	/eii	ι								
								e EVENTS	_ <i>BB</i>																
	Set	1						iable																	
	Disabled	0						ad: Disak																	
	Enabled	1						ad: Enab						_											
F RW SUSPENDED							W	rite '1' to	Enab	ie i	nte	rru	pt fo	or S	USP	ΈN	DED	eve	nt						
							Se	e <i>EVENT</i>	s_sus	PE	NDE	D													
	Set	1					En	able																	
	Disabled	0					Re	ead: Disab	oled																
	Enabled	1					Re	ad: Enab	led																

49.8.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	numb	er		31 30	29 2	8 27	26 2	5 24	23	22 21	20 1	.9 1	8 17	16	15 1	.4 13	12	11 1	0 9	8	7	6	5 4	4 3	2	1 (
Id												F				E			D		С				В	Α
Res	et 0x0	0000000		0 0	0 (0 0	0 (0 0	0	0 0	0 (0 (0	0	0	0 0	0	0 (0	0	0	0	0 (0 0	0	0 (
Id	RW	Field	Value Id	Value	!				De	escripti	on															
Α	RW	STOPPED							Wı	rite '1'	to Dis	sabl	e int	erru	pt f	or ST	OPF	ED e	ven	t						
									Se	e <i>EVEN</i>	ITS_S	TOF	PED													
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	t														
			Enabled	1					Re	ad: Ena	abled															
В	RW	RXDREADY							Wı	rite '1'	to Dis	sabl	e int	erru	pt f	or RX	DRE	ADY	eve	nt						
									Se	e <i>EVEN</i>	ITS_R	XDI	READ	ŊΥ												
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	t														
			Enabled	1					Re	ad: Ena	abled															
С	RW	TXDSENT							Wı	rite '1'	to Dis	sabl	e int	erru	pt f	or TX	DSE	NT e	vent	t						
									Se	e <i>EVEN</i>	ITS_T	XDS	ENT													
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	t														
			Enabled	1					Re	ad: Ena	abled															
D	RW	ERROR							Wı	rite '1'	to Dis	sabl	e int	erru	pt f	or EF	ROF	R eve	nt							
									Se	e <i>EVEN</i>	ITS_E	RRC	OR													
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	t														
			Enabled	1					Re	ad: Ena	abled															
E	RW	ВВ							Wı	rite '1'	to Dis	sabl	e int	erru	pt f	or BE	eve	ent								
									Se	e <i>EVEN</i>	ITS_B	ВВ														
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	t														
			Enabled	1					Re	ad: Ena	abled															
F	RW	SUSPENDED							Wı	rite '1'	to Dis	sabl	e int	erru	pt f	or SL	ISPE	NDE	D ev	ent						
									Se	e <i>EVEN</i>	ITS_S	USF	PEND	ED												
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	t														
			Enabled	1					Re	ad: Ena	abled															

49.8.4 ERRORSRC

Address offset: 0x4C4

Error source

Rit r	numbe	ar.		21	30	20	20 2	7 .	26.1)5 2	04	23 22	21	20	10	10	17	16	15	1/1	12	12	11	10	Q	Q	7	6	5	1	2 2	1	0
	iuiiibe	:1		31	30 .	23	20 2	٠, .	20 2	<u> </u>	24.	ZJ ZZ	. 21	20	13	10	1/	10	13	14	13	12	11	10	9	0	<i>'</i>	U	J	7	<i>3</i> 2	. 1	٥
Id																															(: В	
Rese	et 0x0	0000000		0	0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						- 1	Descr	ipti	on																			
Α	RW	OVERRUN									(Overr	un	erro	or																		
											,	A nev	v by	te v	vas	rec	eiv	ed l	oef	ore	pre	vio	us b	yte	go	t re	ad	by					
											:	softw	are	fro	m tl	he I	RXE	re	gist	er. (Pre	vio	us (lata	a is	lost	t)						
			NotPresent	0							-	Read:	no	ove	erru	n o	ccu	red															
			Present	1							ı	Read	ove	erru	ın o	ccu	rec																
В	RW	ANACK									1	NACK	rec	eive	ed a	fte	r se	ndi	ng	the	ado	dres	ss (v	vrit	e '1	' to	cle	ear)					
			NotPresent	0							- 1	Read:	err	or r	not	pre	sen	t															
			Present	1							1	Read:	err	or p	ores	ent	t																
С	RW	DNACK									-	NACK	rec	eive	ed a	fte	r se	ndi	ng	a da	ita	byt	e (v	rite	e '1	' to	cle	ar)					
			NotPresent	0							-	Read:	err	or r	not	pre	sen	t															
			Present	1							ı	Read:	err	or p	ores	ent	t																



49.8.5 ENABLE

Address offset: 0x500

Enable TWI

Bitı	numb	oer			33	1 30	29	28	3 27	26	5 25	24	23	22	21	20	19 :	18 3	17 1	16 1	.5 1	4 1	3 1	2 11	10	9	8	7	6	5	4	3	2 1	L 0
Id																																Α.	A A	АА
Res	et 0x	000	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	/ F	Field	Value Id	V	alue	2						De	scri	ptic	n																		
Α	RW	/ E	ENABLE										En	able	or	disa	ble	TV	/I															
				Disabled	0								Dis	sable	e TV	٧I																		
				Enabled	5								En	able	TV	V١																		

49.8.6 PSELSCL

Address offset: 0x508 Pin select for SCL

Bitı	numb	er		31	. 30	29	28	8 2	7 26	25	24	23	22	21 :	20 1	L9 1	8 1	7 10	5 15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	. 4	A A	Α	Α	Α	Α	Α	Α	A A	А Д	. Α	Α	Α	Α	Α	A A	A A	. A	Α	Α	Α	Α	Α	A ,	А А
Res	et Oxl	FFFFFFF		1	1	1	1	. 1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1 1	l 1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptio	n																	
Α	RW	PSELSCL		[0	31	.]						Pir	nuı	mbe	er co	onfi	gura	tio	n fo	r TV	VI S	CL si	gna									
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t																	

49.8.7 PSELSDA

Address offset: 0x50C Pin select for SDA

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	9 18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	А А	Α	Α	Α	Α	Α	Α.	4 Δ	A	Α	Α	Α	Α	Α	Α	A A	4 Α	A A
Res	et 0xl	FFFFFF		1	1	1	1	1	1	1	1	1	1	1 1	l 1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 1	l 1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	1																	
Α	RW	PSELSDA		[0]	.31]							Pin	nun	nbei	r cor	nfig	urat	ion	for	TW	'I SD	A sia	gnal									
																							J									

49.8.8 RXD

Address offset: 0x518

RXD register

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13	12 11 10 9 8	7 6 5	4 3 2	1 0
Id						A A A	. A A A .	А А
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0	0 0 0	0 0
Id RW Field	Value Id	Value	Description					
A R RXD			RXD register					

49.8.9 TXD

Address offset: 0x51C

TXD register

Bit r	numbe	r		31	30	29	28	27 2	26 2	25 2	24 :	23 2	22 2	21 2	0 1	9 1	8 1	7 1	6 1	5 14	4 13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id																											Α	Α	Α	Α	Α /	Δ ,	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0 0) (0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tio	n																		
Α	RW	TXD									-	TXD	reg	giste	er																		



49.8.10 FREQUENCY

Address offset: 0x524

TWI frequency

Bitı	numbe	r		31	1 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14 :	l3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A 4	Δ Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	4000000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																			
Α	RW	FREQUENCY										ΤV	/I m	aste	er c	locl	k fr	equ	en	су														_
			K100	0x	(019	980	000)				10	0 kb	ps																				
			K250	0x	(040	000	000)				25	0 kb	ps																				
			K400	0x	066	580	000)				40	0 kb	ps	(act	tual	rat	e 4	10.	256	kbį	os)												

49.8.11 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	7 16 15 14 13 12 11 1	10 9 8 7 6	5 4 3 2 1 0
Id					А	A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	000000	0 0 0 0 0	0 0 0 0 0 0
ld RW Field	Value Id	Value	Description			
A RW ADDRESS			Address used in the T	WI transfer		

49.9 Electrical Specification

49.9.1 TWI interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWI}	Bit rates for TWI ⁴¹	100		400	kbps
I _{TWI,100kbps}	Run current for TWI, 100 kbps		50		μΑ
I _{TWI,400kbps}	Run current for TWI, 400 kbps		50		μΑ
t _{TWI,START,LP}	Time from STARTRX/STARTTX task to transmission started, Low		t _{TWI,STAI}	RT,C	μs
	power mode		+		
			t _{START_H}	FIN	
t _{TWI,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1.5		μs
	Constant latency mode				

49.9.2 Two Wire Interface (TWI) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWI,SCL,100kbps}	SCL clock frequency, 100 kbps		100		kHz
f _{TWI,SCL,250kbps}	SCL clock frequency, 250 kbps		250		kHz
f _{TWI,SCL,400kbps}	SCL clock frequency, 400 kbps		400		kHz
t _{TWI,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWI,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWI,HD_STA,100kbps}	TWI master hold time for START and repeated START condition,	10000			ns
	100 kbps				
t _{TWI,HD_STA,250kbps}	TWI master hold time for START and repeated START condition,	4000			ns
	250kbps				
t _{TWI,HD_STA,400kbps}	TWI master hold time for START and repeated START condition,	2500			ns
	400 kbps				
t _{TWI,SU_STO,100kbps}	TWI master setup time from SCL high to STOP condition, 100	5000			ns
	kbps				

Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWI,SU_STO,250kbps}	TWI master setup time from SCL high to STOP condition, 250	2000			ns
	kbps				
t _{TWI,SU_STO,400kbps}	TWI master setup time from SCL high to STOP condition, 400	1250			ns
	kbps				
t _{TWI,BUF,100kbps}	TWI master bus free time between STOP and START conditions,	5800			ns
	100 kbps				
t _{TWI,BUF,250kbps}	TWI master bus free time between STOP and START conditions,	2700			ns
	250 kbps				
t _{TWI,BUF,400kbps}	TWI master bus free time between STOP and START conditions,	2100			ns
	400 kbps				

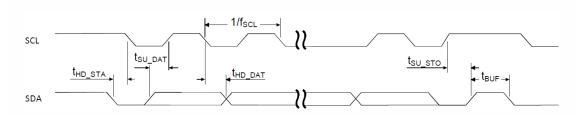


Figure 158: TWI timing diagram, 1 byte transaction



50 UART — Universal asynchronous receiver/ transmitter

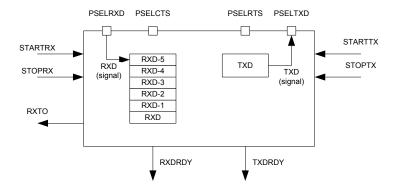


Figure 159: UART configuration

50.1 Functional description

Listed here are the main features of UART.

The UART implements support for the following features:

- Full-duplex operation
- · Automatic flow control
- Parity checking and generation for the 9th data bit

As illustrated in *Figure 159: UART configuration* on page 526, the UART uses the TXD and RXD registers directly to transmit and receive data. The UART uses one stop bit.

50.2 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UART are mapped to physical pins according to the configuration specified in the PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers respectively.

If a value of 0xFFFFFFFF is specified in any of these registers, the associated UART signal will not be connected to any physical pin. The PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers and their configurations are only used as long as the UART is enabled, and retained only for the duration the device is in ON mode. PSELRXD, PSELCTS, PSELRTS and PSELTXD must only be configured when the UART is disabled.

To secure correct signal levels on the pins by the UART when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Pin configuration* on page 526.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 123: GPIO configuration

UART pin	Direction	Output value
RXD	Input	Not applicable
CTS	Input	Not applicable
RTS	Output	1
TXD	Output	1



50.3 Shared resources

The UART shares registers and other resources with other peripherals that have the same ID as the UART.

Therefore, you must disable all peripherals that have the same ID as the UART before the UART can be configured and used. Disabling a peripheral that has the same ID as the UART will not reset any of the registers that are shared with the UART. It is therefore important to configure all relevant UART registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 21 for details on peripherals and their IDs.

50.4 Transmission

A UART transmission sequence is started by triggering the STARTTX task.

Bytes are transmitted by writing to the TXD register. When a byte has been successfully transmitted the UART will generate a TXDRDY event after which a new byte can be written to the TXD register. A UART transmission sequence is stopped immediately by triggering the STOPTX task.

If flow control is enabled a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 160: UART transmission* on page 527. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended. For more information, see *Suspending the UART* on page 528.

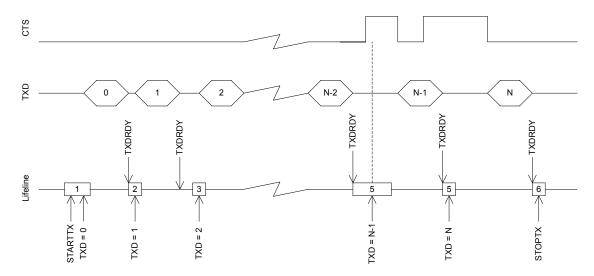


Figure 160: UART transmission

50.5 Reception

A UART reception sequence is started by triggering the STARTRX task.

The UART receiver chain implements a FIFO capable of storing six incoming RXD bytes before data is overwritten. Bytes are extracted from this FIFO by reading the RXD register. When a byte is extracted from the FIFO a new byte pending in the FIFO will be moved to the RXD register. The UART will generate an RXDRDY event every time a new byte is moved to the RXD register.

When flow control is enabled, the UART will deactivate the RTS signal when there is only space for four more bytes in the receiver FIFO. The counterpart transmitter is therefore able to send up to four bytes after the RTS signal is deactivated before data is being overwritten. To prevent overwriting data in the FIFO, the counterpart UART transmitter must therefore make sure to stop transmitting data within four bytes after the RTS line is deactivated.



The RTS signal will first be activated again when the FIFO has been emptied, that is, when all bytes in the FIFO have been read by the CPU, see *Figure 161: UART reception* on page 528.

The RTS signal will also be deactivated when the receiver is stopped through the STOPRX task as illustrated in *Figure 161: UART reception* on page 528. The UART is able to receive four to five additional bytes if they are sent in succession immediately after the RTS signal has been deactivated. This is possible because the UART is, even after the STOPRX task is triggered, able to receive bytes for an extended period of time dependent on the configured baud rate. The UART will generate a receiver timeout event (RXTO) when this period has elapsed.

To prevent loss of incoming data the RXD register must only be read one time following every RXDRDY event.

To secure that the CPU can detect all incoming RXDRDY events through the RXDRDY event register, the RXDRDY event register must be cleared before the RXD register is read. The reason for this is that the UART is allowed to write a new byte to the RXD register, and therefore can also generate a new event, immediately after the RXD register is read (emptied) by the CPU.

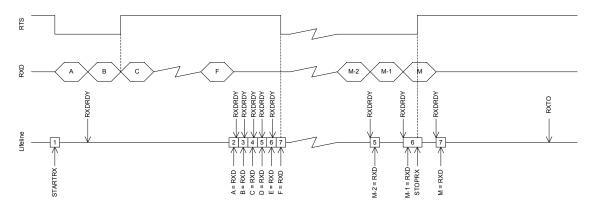


Figure 161: UART reception

As indicated in occurrence 2 in the figure, the RXDRDY event associated with byte B is generated first after byte A has been extracted from RXD.

50.6 Suspending the UART

The UART can be suspended by triggering the SUSPEND task.

SUSPEND will affect both the UART receiver and the UART transmitter, i.e. the transmitter will stop transmitting and the receiver will stop receiving. UART transmission and reception can be resumed, after being suspended, by triggering STARTTX and STARTRX respectively.

Following a SUSPEND task, an ongoing TXD byte transmission will be completed before the UART is suspended.

When the SUSPEND task is triggered, the UART receiver will behave in the same way as it does when the STOPRX task is triggered.

50.7 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.



50.8 Using the UART without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

50.9 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

50.10 Registers

Table 124: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40002000	UART	UART0	Universal Asynchronous Receiver/		Deprecated
			Transmitter		

Table 125: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_SUSPEND	0x01C	Suspend UART
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSELRTS	0x508	Pin select for RTS
PSELTXD	0x50C	Pin select for TXD
PSELCTS	0x510	Pin select for CTS
PSELRXD	0x514	Pin select for RXD
RXD	0x518	RXD register
TXD	0x51C	TXD register
BAUDRATE	0x524	Baud rate
CONFIG	0x56C	Configuration of parity and hardware flow control

50.10.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number	31 30 2	29 28 27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2	1 0
Id				ВА	
Reset 0x00000000	0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0
Id RW Field Valu	e Id Value	Description			

A RW CTS_STARTRX

Shortcut between CTS event and STARTRX task



Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ВА
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_CTS and TASKS_STARTRX
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut
B RW NCTS_STOPRX			Shortcut between NCTS event and STOPRX task
			See EVENTS_NCTS and TASKS_STOPRX
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

50.10.2 INTENSET

Address offset: 0x304 Enable interrupt

Enable Interrupt			
Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			F E D C B
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW CTS			Write '1' to Enable interrupt for CTS event
			See EVENTS_CTS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW NCTS			Write '1' to Enable interrupt for NCTS event
			See EVENTS_NCTS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW RXDRDY			Write '1' to Enable interrupt for RXDRDY event
	Č-1	4	See EVENTS_RXDRDY
	Set Disabled	1 0	Enable Read: Disabled
	Enabled	1	Read: Enabled
D RW TXDRDY	Lilabled	1	Write '1' to Enable interrupt for TXDRDY event
D KW INDIDI			
			See EVENTS_TXDRDY
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW ERROR			Write '1' to Enable interrupt for ERROR event
			See EVENTS_ERROR
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW RXTO			Write '1' to Enable interrupt for RXTO event
			See EVENTS_RXTO
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

50.10.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	numbe	er		31	30	29	28	27 2	6 2	25 24	4 2	23	22 2	1 2	20	19	18	3 17	1	6 :	15	14	13	12	11	. 10	9	8	7	6	5	4	3	3 2	1	. 0
Id																		F									Ε		D					C	: E	A
Res	et 0x0	0000000		0	0	0	0	0 () (0 0) (0	0 (כ	0	0	0	0	C)	0	0	0	0	0	0	0	0	0	C	0	0) (0	C	0
Id	RW	Field	Value Id	Val	ue						C	Des	scrip	tio	n																					
Α	RW	CTS									٧	۷ri	ite '1	.' t	o D	isa	ble	e in	ter	ru	pt 1	or	CT:	s e	ver	nt										
											S	ee	e EVE	N	rs_	CTS	5																			
			Clear	1							C	Disa	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
В	RW	NCTS									٧	۷ri	ite '1	.' t	o D	isa	ble	e in	ter	ru	pt 1	or	NC	TS	ev	ent										
											S	ee	e EVE	N	rs_	NC	TS																			
			Clear	1							C	Disa	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
С	RW	RXDRDY									٧	۷ri	ite '1	.' t	o D	isa	ble	e in	ter	ru	pt 1	or	RX	DR	DY	eve	ent									
											S	ee	e EVE	N	rs_	RX	DR	DΥ																		
			Clear	1							C	Disa	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
D	RW	TXDRDY									٧	۷ri	ite '1	.' t	o D	isa	ble	e in	ter	ru	pt 1	or	TXI	DRI	DY	eve	nt									
											S	ee	EVE	N	rs_	TXI	DR	DΥ																		
			Clear	1							C	Disa	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
Ε	RW	ERROR									٧	۷ri	ite '1	.' t	o D	isa	ble	e in	ter	ru	pt 1	or	ERI	RO	R e	ver	it									
											S	ee	e EVE	N	rs_	ERI	۲ <i>O</i>	R																		
			Clear	1								Disa	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
F	RW	RXTO									٧	۷ri	ite '1	.' t	o D	isa	ble	e in	ter	ru	pt 1	or	RX'	ТО	ev	ent										
											S	ee	EVE	N	rs_	RX	то																			
			Clear	1							C	Disa	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				

50.10.4 ERRORSRC

Address offset: 0x480

Error source

Bit	numbe	er		31	30	29	28	27	26	25	24	23 2	22 2	21 2	0 1	.9 1	18 1	L7 1	16 :	15	14 1	L3 1	12 1	1 1	9	8	7	6	5	4	3	2 1	. 0
Id																															D	СВ	8 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue							Des	scrip	tior	า																		
Α	RW	OVERRUN										Ove	erru	n er	ror																		
												A st	tart	bit i	s re	ecei	ive	lw b	hile	th:	e pı	evi	ous	dat	a sti	II lie	es ir	ı RX	D.				
												(Pre	evio	us d	ata	is l	lost	:.)															
			NotPresent	0								Rea	ad: e	rror	r no	ot p	res	ent															
			Present	1								Rea	ad: e	rror	rpr	ese	nt																
В	RW	PARITY										Pari	ity e	erro	r																		
												A ch	hara	ictei	r wi	ith l	bac	l pa	rity	/ is	rec	eive	d, i	f HV	V pa	rity	che	eck i	is				
												ena	ble	d.																			
			NotPresent	0								Rea	ad: e	rror	r no	ot p	res	ent															
			Present	1								Rea	ad: e	rror	pr	ese	nt																
С	RW	FRAMING										Fran	min	g er	ror	occ	curi	red															



Bit	numbe	er		31	. 30	29	28	27	26	25 :	24	23 22	2 21	20	19	18	17	16	15	14 1	13 :	12 1	1 :	10 9	9	8 7	' 6	5	4	3	2	1	0
Id																														D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	llue							Desc	ript	ion																			
												A val	id s	top	bit i	s no	ot d	ete	cte	d on	th	e se	ria	l da	ta i	npu	t af	er a	all				
												bits i	n a	char	ract	er h	ave	be	en	rece	eive	d.											
			NotPresent	0								Read	l: er	ror ı	not	pre	sen	t															
			Present	1								Read	l: er	ror _l	pres	ent																	
D	RW	BREAK										Breal	k co	ndit	ion																		
												The s	seria	al da	ıta i	npı	ıt is	'0'	for	long	ger	tha	n tł	ne le	eng	th c	fa	data	9				
												fram	e. (The	data	a fra	ame	e lei	ngth	is :	10 k	oits	wit	hou	ıt p	arit	/ bit	, ar	ıd				
												11 bi	its w	/ith	pari	ity Ł	oit.)																
			NotPresent	0								Read	l: er	rorı	not	pre	sen	t															
			Present	1								Read	l: er	ror	pres	ent																	
																		t															

50.10.5 ENABLE

Address offset: 0x500

Enable UART

Bit	numbe	r		33	1 30	29	9 2	8 2	7 2	26 :	25	24	23	22	21	20	19	18	3 17	16	5 15	5 1	4 1	3 1	2 1	.1 1	0 9	9 ;	8	7	6	5	4	3 2	1	0
Id																																		4 A	Α	Α
Res	et 0x0	0000000		0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	C	() (0	0 () (0 (0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	V	alu	е							De	scr	ipti	on																				
Α	RW	ENABLE											Ena	abl	e o	dis	ab	le l	JAF	Т																
			Disabled	0									Dis	ab	le L	IAR	Т																			
			Enabled	4									Ena	abl	e U	AR	ī																			

50.10.6 PSELRTS

Address offset: 0x508 Pin select for RTS

Bitı	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 18	3 17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	ΑА	A	Α	Α	Α	Α	A	4 4	A	Α	Α	Α	Α	Α	Α	A A	A /	A A
Res	et Oxl	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 :	L 1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	PSELRTS		[0	31]						Pin	nur	nbe	r co	nfig	urat	ion	for	UA	RT R	TS s	igna	I								
			Disconnected	0x	FFF	FFF	FF					Dis	coni	nect	t																	

50.10.7 PSELTXD

Address offset: 0x50C Pin select for TXD

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 18	3 17	16	15	14	13 :	L2 1	11 10	9	8	7	6	5	4 3	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A ,	ДД	A	Α	Α	Α	Α	Α	Α.	А А	Α	Α	Α	Α	Α	A A	A	Α	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 1	1	1	1	1	1	1 1	l 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	PSELTXD		[0	31]							Pin	nun	nbe	r co	nfig	ura	tion	for	UA	RT 1	ΧD	sign	al								_
			Disconnected	0x	FFFI	FFFI	FF					Disc	conr	nect	t																	

50.10.8 PSELCTS

Address offset: 0x510 Pin select for CTS



Bitı	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 18	3 17	16	15	14	13	12 1	.1 10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	ΑА	A	А	Α	Α	Α	Α	A .	4 A	Α	Α	Α	Α	Α	Α	A	A /	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	1	. 1	1	1	1	1	1	1 1	1	1	1	1	1	1	1 :	L 1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	PSELCTS		[0.	31]						Pin	nur	nbe	r co	nfig	urat	tion	for	UA	RT (CTS	sign	al								
			Disconnected	0x	FFF	FFF	FF					Dis	coni	nect	t																	

50.10.9 PSELRXD

Address offset: 0x514 Pin select for RXD

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9	8 7	7 6	5	4	3 2	1 0
Id				A A A A A A A A A A A A A A A A A A A	АА	A A	Α	Α	A A	A A
Res	et 0xF	FFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1	l 1	1	1	1 :	1 1
Id	RW	Field	Value Id	Value Description						
Α	RW	PSELRXD		[031] Pin number configuration for UART RXD signal						
			Disconnected	0xFFFFFFF Disconnect						

50.10.10 RXD

Address offset: 0x518

RXD register

Bitı	numbe	er		31	30 2	9 :	28 2	27 2	6 2	5 2	4 2	3 2	2 21	L 20	19	18	17	16	15	14	13 :	L2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	Α	A	А А
Res	et 0x0	0000000		0	0	0	0	0 () () () (0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion																		
Α	R	RXD									R	X d	ata	rece	eive	d in	pre	evic	us	tran	sfei	s, d	oub	e bı	uffe	red						

50.10.11 TXD

Address offset: 0x51C

TXD register

Bit nu	ımber			31	30 2	29 2	8 27	26 2	25 2	4 23	22	21 2	20 1	.9 18	3 17	16	15 1	4 13	12	11 1	10 9	8	7	6	5	4	3 2	1	0
Id																							Α	Α	Α	Α	А А	Α	Α
Reset	0x000	000000		0	0	0 (0 0	0	0 (0	0	0	0	0 0	0	0	0 (0	0	0	0 0	0	0	0	0	0	0 0	0	0
ld I	RW F	ield	Value Id	Va	lue					De	scri	ptio	n																
Α '	w 1	TXD								TX	dat	a to	be '	trans	ferr	ed													

50.10.12 BAUDRATE

Address offset: 0x524

Baud rate

		31 30 29 28 27		Bit number
A A A A A A A A	A A A A A A A A A A A A A A	AAAAA		ld
0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0		Reset 0x04000000
	Description	Value	Value Id	ld RW Field
	Baud-rate			A RW BAUDRATE
	1200 baud (actual rate: 1205)	0x0004F000	Baud1200	
	2400 baud (actual rate: 2396)	0x0009D000	Baud2400	
	4800 baud (actual rate: 4808)	0x0013B000	Baud4800	
	9600 baud (actual rate: 9598)	0x00275000	Baud9600	
	14400 baud (actual rate: 14414)	0x003B0000	Baud14400	
	19200 baud (actual rate: 19208)	0x004EA000	Baud19200	
	28800 baud (actual rate: 28829)	0x0075F000	Baud28800	
	38400 baud (actual rate: 38462)	0x009D5000	Baud38400	
	57600 baud (actual rate: 57762)	0x00EBF000	Baud57600	
	Baud-rate 1200 baud (actual rate: 1205) 2400 baud (actual rate: 2396) 4800 baud (actual rate: 4808) 9600 baud (actual rate: 9598) 14400 baud (actual rate: 14414) 19200 baud (actual rate: 19208) 28800 baud (actual rate: 28829) 38400 baud (actual rate: 38462)	0x0004F000 0x0009D000 0x0013B000 0x00275000 0x003B0000 0x004EA000 0x0075F000 0x009D5000	Baud1200 Baud2400 Baud4800 Baud9600 Baud14400 Baud19200 Baud28800 Baud38400	ld RW Field



Bit number	31 30 29 28 2	27 26 25 24 :	23 22 21 20	19 18 17	16 1	L5 14	13 12	11 10	9	8 7	6	5 -	4 3	2	1 0
Id	A A A A	A A A A	A A A A	A A A	Α ,	А А	A A	АА	Α	ΑА	A	Α .	4 А	Α	A A
Reset 0x04000000	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0	0	0 0	0 0	0 0	0	0 0	0	0	0 0	0	0 0
Id RW Field Value Id	l Value	l l	Description												
Baud76	0x013A9000	:	76800 baud	(actual ra	te: 76	5923)									
Baud11	5200 0x01D7E000	:	115200 bau	d (actual r	ate: 1	11594	2)								
Baud23	0400 0x03AFB000	:	230400 bau	d (actual r	ate: 2	23188	4)								
Baud25	0000 0x04000000	:	250000 bau	d											
Baud46	0800 0x075F7000	4	460800 bau	d (actual r	ate: 4	47058	8)								
Baud92	1600 0x0EBED000	9	921600 bau	d (actual r	ate: 9	94117	(6)								
Baud1N	0x10000000	:	1Mega baud	l											

50.10.13 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id																																ВВ	Е	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
ld	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	HWFC										Ha	rdw	are	flo	w	con	tro	ı															
			Disabled	0								Dis	abl	ed																				
			Enabled	1								Ena	able	ed																				
В	RW	PARITY										Par	ity																					
			Excluded	0x	0							Exc	lud	le p	arit	y b	it																	
			Included	0x	7							Inc	lud	ера	arit	y b	it																	

50.11 Electrical Specification

50.11.1 UART electrical specification

Symbol	Description	Min.	Тур.	Max.	Units
f _{UART}	Baud rate for UART ⁴² .			1000	kbps
I _{UART1M}	Run current at max baud rate.		55		μΑ
I _{UART115k}	Run current at 115200 bps.		55		μΑ
I _{UART1k2}	Run current at 1200 bps.		55		μΑ
I _{UART,IDLE}	Idle current for UART		1		μΑ
t _{UART,CTSH}	CTS high time	1			μs
t _{UART,START,LP}	Time from STARTRX/STARTTX task to transmission started, low		t _{UART,STAR}	т	μs
	power mode		+		
			t _{START_HFI}	N	
t _{UART,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1		μs
	constant latency mode				

Higher baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.



51 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

51.1 QFN48 6 x 6 mm package

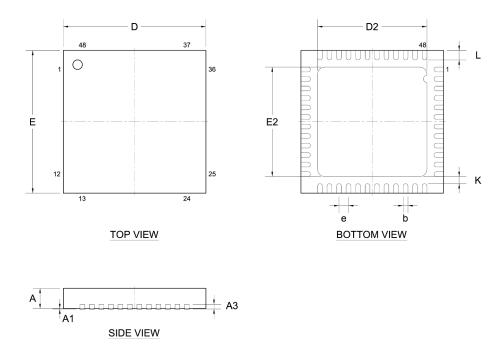


Figure 162: QFN48 6 x 6 mm package

Table 126: QFN48 dimensions in millimeters

Package	Α	A1	А3	b	D, E	D2, E2	е	K	L	
	0.80	0.00		0.15		4.50		0.20	0.35	Min.
QFN48 (6x6)	0.85	0.02	0.2	0.20	6.0	4.60	0.4		0.40	Nom.
	0.90	0.05		0.25		4.70			0.45	Max.



52 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

52.1 IC marking

The nRF52832 IC package is marked like described below.

N	5	2	8	3	2
<p< td=""><td>P></td><td><v< td=""><td>V></td><td><h></h></td><td><p></p></td></v<></td></p<>	P>	<v< td=""><td>V></td><td><h></h></td><td><p></p></td></v<>	V>	<h></h>	<p></p>
<y< td=""><td>Y></td><td><w< td=""><td>W></td><td><l< td=""><td>L></td></l<></td></w<></td></y<>	Y>	<w< td=""><td>W></td><td><l< td=""><td>L></td></l<></td></w<>	W>	<l< td=""><td>L></td></l<>	L>

Figure 163: Package marking

52.2 Box labels

Here are the box labels used for the nRF52832.

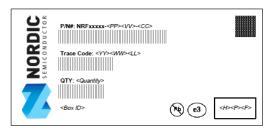


Figure 164: Inner box label



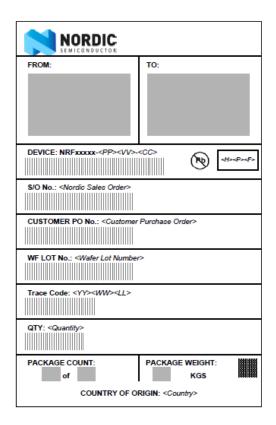


Figure 165: Outer box label

52.3 Order code

Here are the nRF52832 order codes and definitions.

n	R	F	5	2	8	3	2	1	<p< th=""><th>P></th><th><v< th=""><th>V></th><th>-</th><th><c< th=""><th>C></th><th></th></c<></th></v<></th></p<>	P>	<v< th=""><th>V></th><th>-</th><th><c< th=""><th>C></th><th></th></c<></th></v<>	V>	-	<c< th=""><th>C></th><th></th></c<>	C>	
---	---	---	---	---	---	---	---	---	------------------------------------------------------------------------------------------------------------------------------	----	----------------------------------------------------------------------------------------	----	---	----------------------------------------	----	--

Figure 166: Order code

Table 127: Abbreviations

Abbrevitation	Definition and implemented codes
N52/nRF52	nRF52 series product
832	Part code
<pp></pp>	Package variant code
<vv></vv>	Function variant code
<h><p><f></f></p></h>	Build code
	H - Hardware version code
	P - Production configuration code (production site, etc.)
<yy><ww><ll></ll></ww></yy>	F - Firmware version code (only visible on shipping container label) Tracking code
	YY - Year code
	WW - Assembly week number
<cc></cc>	LL - Wafer lot code Container code

52.4 Code ranges and values

Defined here are the nRF52832 code ranges and values.



Table 128: Package variant codes

<pp></pp>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
QF	QFN	6 x 6	48	0.4
CH	WLCSP	2.9 x 3.2	50	0.4

Table 129: Function variant codes

<vv></vv>	Flash (kB)	RAM (kB)
AA	512	64
AB	256	32

Table 130: Hardware version codes

<h></h>	Description
[A Z]	Hardware version/revision identifier (incremental)

Table 131: Production configuration codes

<p></p>	Description
[09]	Production device identifier (incremental)
[A Z]	Engineering device identifier (incremental)

Table 132: Production version codes

<f></f>	Description
[A N, P Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 133: Year codes

<yy></yy>	Description
[1599]	Production year: 2015 to 2099

Table 134: Week codes

Table 135: Lot codes

<ll></ll>	Description	
[AA ZZ]	Wafer production lot identifier	

Table 136: Container codes

<cc></cc>	Description
R7	7" Reel
R	13" Reel
T	Tray

52.5 Product options

Defined here are the nRF52832 product options.

Table 137: nRF IC order codes

Order code	MOQ ⁴³	Comment
nRF52832-QFAA-R7	1000	Availability to be announced.
nRF52832-QFAA-R	3000	
nRF52832-QFAA-T	490	
nRF52832-CHAA-R7	1500	
nRF52832-CHAA-R	7000	
nRF52832-QFAB-R	3000	

Table 138: Development tools order code

Order code	Description
nRF52-DK	nRF52 Development Kit



53 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from www.nordicsemi.com.

53.1 Schematic QFAA QFN48 with internal LDO setup

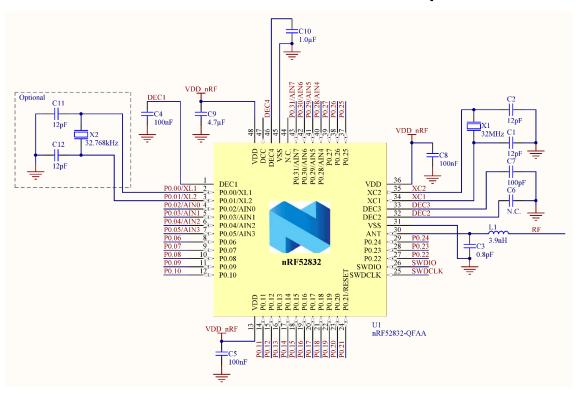


Figure 167: QFAA QFN48 with internal LDO setup

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the nRF52832 on *www.nordicsemi.com*.

Table 139: Bill of material for QFAA QFN48 with internal LDO setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
U1	nRF52832-QFAA	Multi-protocol Bluetooth low energy and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, 9 pF, ±20 ppm	XTAL 3215



53.2 Schematic QFAA QFN48 with DC/DC regulator setup

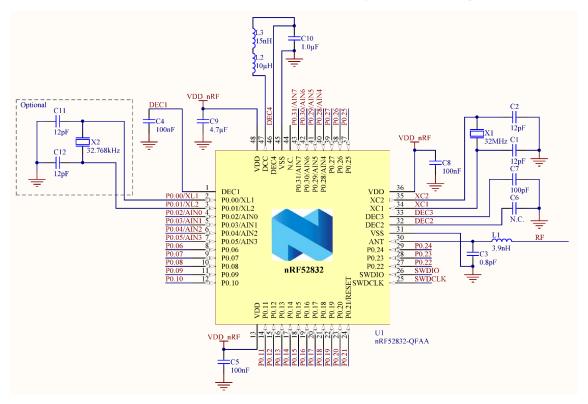


Figure 168: QFAA QFN48 with DC/DC regulator setup

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for nRF52832 on *www.nordicsemi.com*.

Table 140: Bill of material for QFAA QFN48 with DC/DC regulator setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-QFAA	Multi-protocol Bluetooth low energy and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, 9 pF, ±20 ppm	XTAL_3215



53.3 Schematic QFAA QFN48 with DC/DC regulator and NFC setup

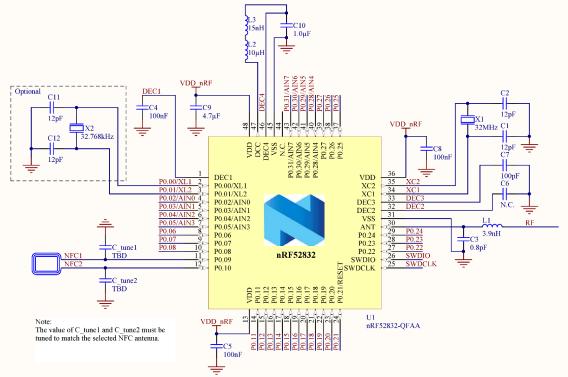


Figure 169: QFAA QFN48 with DC/DC regulator and NFC setup

Important: For PCB reference layouts, see the Reference Layout section on the Downloads tab for nRF52832 on *www.nordicsemi.com*.

Table 141: Bill of material for QFAA QFN48 with DC/DC converter and NFC setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
C _{tune1} , Ctune2	TBD pF	Capacitor, NPO, ±5%	0402
L1	3.9 nH	High frequency chip inductor ±5%	0402
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-QFAA	Multi-protocol Bluetooth low energy and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, 9 pF, ±20 ppm	XTAL_3215

53.4 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality.

A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from *www.nordicsemi.com*.

To ensure optimal performance it is essential that you follow the schematics- and layout references closely. Especially in the case of the antenna matching circuitry (components between device pin ANT and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 ohm single end antenna.



A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna matching circuitry (components between device pin ANT and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the RF pin ANT and the antenna, to match the antenna impedance (normally 50 ohm) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in the recommended QFN48 package reference circuitry from *Schematic QFAA QFN48 with internal LDO setup* on page 539.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Fast switching digital signals should not be routed close to the crystal or the power supply lines. Capacitive loading of fast switching digital output lines should be minimized in order to avoid radio interference.

53.5 PCB layout example

The PCB layout shown below is a reference layout for the QFN package with internal LDO setup.

Important: Pay attention to how the capacitor C3 is grounded. It is not directly connected to the ground plane, but grounded via VSS pin 31. This is done to create additional filtering of harmonic components.

For all available reference layouts, see the Reference Layout section on the Downloads tab for nRF52832 on www.nordicsemi.com.

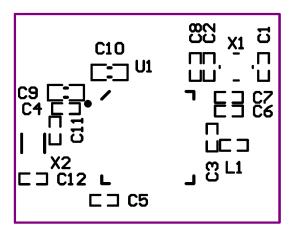


Figure 170: Top silk layer



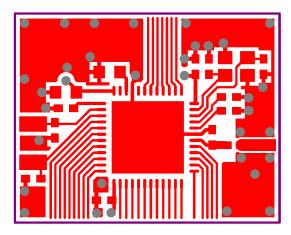


Figure 171: Top layer

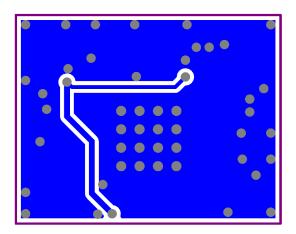


Figure 172: Bottom layer

Important: No components in bottom layer.



54 Liability disclaimer

Liability disclaimer

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