

REV	Description	DATE	BY
A4A	Initial production Release.	11/19/2012	GC
A5	On the initial production release the processors were to be found incorrect as supplied by TI. Parts while marked AM3359 were actually AM3352. This revision uses the correct parts.	1/2/2013	GC
A5A	<ol style="list-style-type: none"> <li>Deleted R29-R44 from the LCD lines.</li> <li>Added 47pf capacitors C156-C173 to LCD data lines to ground.</li> <li>Changed schematic revision to A5A.</li> <li>Changed a few footprints after PCB update for above changes.</li> <li>Added access point for the battery function of the TPS65217C.</li> <li>Added Ferrite beads in series with LED power and 5V power rail of the USB host connector. Required to pass FCC/CE testing due to noise emissions on that pin.</li> <li>Added power button to enable sleep, wakeup, power down and power up features on the system.</li> <li>Added Modification to add 100K ohm resistor to ground to prevent crosstalk when serial cable is not plugged in.</li> </ol>	2/8/2013	GC
A5B	<ol style="list-style-type: none"> <li>Added 100K pull-down on J1 pin 4 to prevent crosstalk when serial cable is not connected into PCB layout.</li> <li>Changed the LED resistors to 4.75K to lower the brightness.</li> </ol>	5/21/2013	GC
A5C	<ol style="list-style-type: none"> <li>Changed R46, R47, R48 to 0 ohms.</li> <li>Changed R45 to 22 Ohms.</li> </ol> <p>Change was made due to production failures on some boards due to differences in impedances.</p>	6/12/2013	GC
A6	<ol style="list-style-type: none"> <li>Moved the enable for the VDD_3V3B regulator to VDD_3V3A rail. Change was made to reduce the delay between the ramp up of the 3.3V rails.</li> <li>Added a AND gate to the SYS_RESETn circuitry. There is a small chance that on power up the nRESETOUT signal on the processor may go high, causing the SYS_RESETn signal to go HI before it should. This change reinforces the reset with the PORZn reset signal.</li> <li>Added optional zero ohm resistor to tie GND_OSC0 to system ground.</li> </ol>	7/25/2013	GC
A6A	<ol style="list-style-type: none"> <li>Added optional zero ohm resistor to tie GND_OSC1 to system ground.</li> <li>Changed C106 to a 1uF capacitor.</li> <li>Changed C24 to a 2.2uF capacitor.</li> <li>Made R8 installed and R9 not installed.</li> </ol>	12/13/2013	GC
B	1.Changed the processor to the AM3588ZC100.	1/20/2014	GC
C	1.Increased the eMMC from 2GB to 4GB.	3/21/2014	GC

**This schematic is \*NOT SUPPORTED\* and DOES NOT constitute a reference design. Only "community" support is allowed via resources at BeagleBoard.org/discuss.**

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2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, UAB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	eMMC FLASH
9	10/100 ETHERNET
10	HDMI FRAMER
11	EXP CONN, uSD

**NOTE: PCB Revision for this board is Rev B6**



Title BeagleBone Black Cover Page

Size Document Number  
 B 450-5500-001

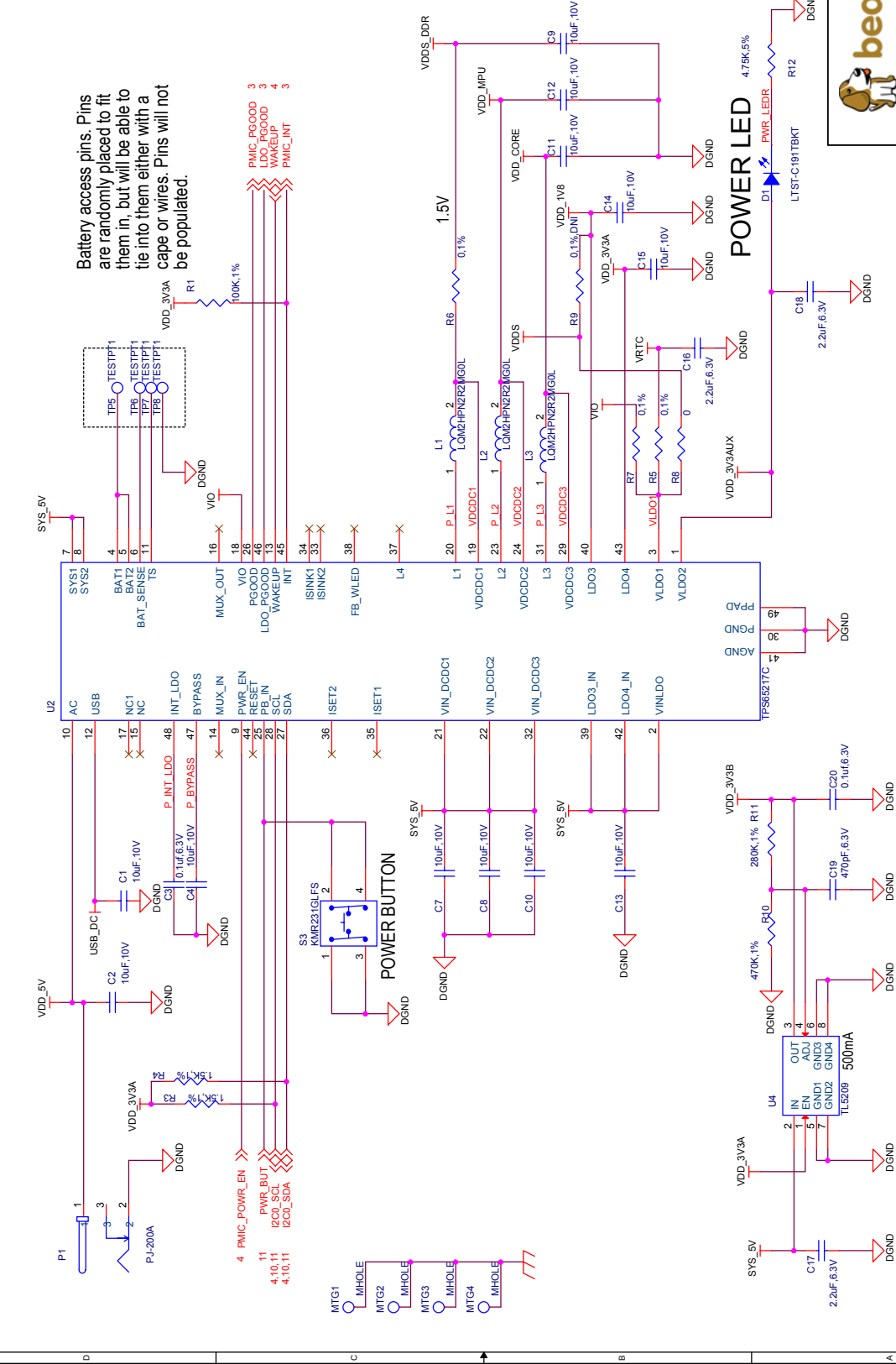
Rev C

Date: Friday, March 21, 2014

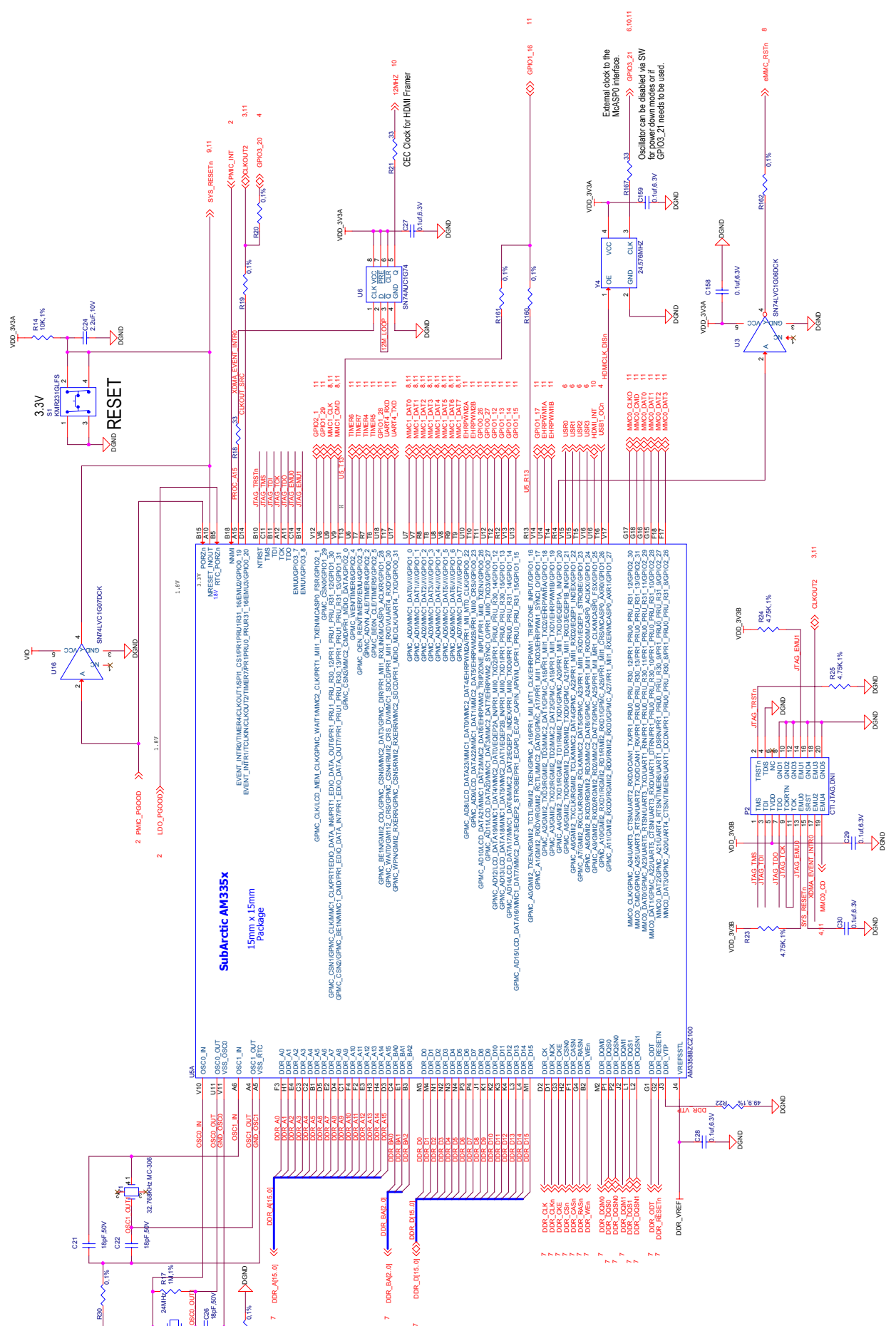
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Battery access pins. Pins are randomly placed to fit them in, but will be able to tie into them either with a cape or wires. Pins will not be populated.



Title		BeagleBone Black Power Management
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**SubArctic AM335x**  
 15mm x 15mm  
 Package

Extends clock to the  
 MicroSDIO interfaces.  
 Oscillator can be disabled via SW  
 for power down modes or if  
 GPIO\_Z1 needs to be used.

CEC Clock for HDMI Framers  
 12MHz

VDD\_3V3B  
 0.1µF 6.3V  
 XOSCI1  
 24.576MHz

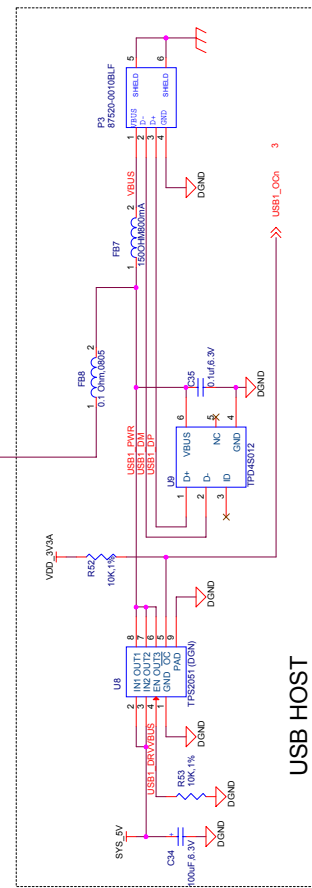
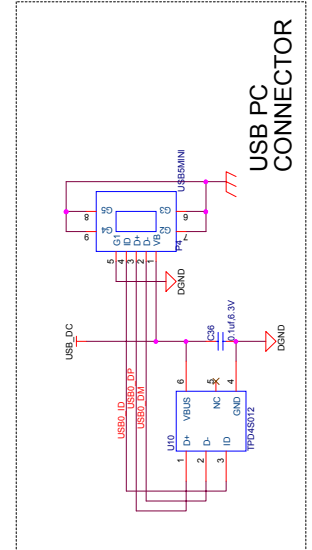
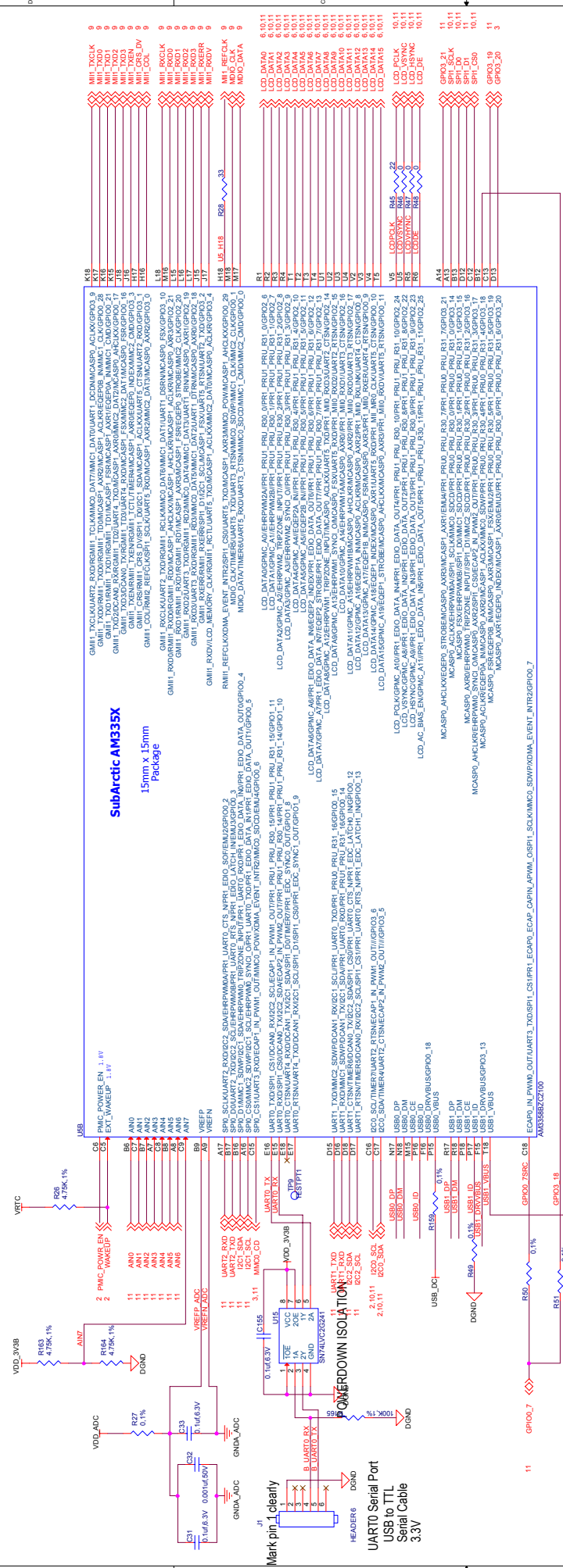
VDD\_3V3B  
 0.1µF 6.3V  
 XOSCI2  
 24.576MHz

VDD\_3V3B  
 0.1µF 6.3V  
 XOSCI3  
 24.576MHz

VDD\_3V3B  
 0.1µF 6.3V  
 XOSCI4  
 24.576MHz

VDD\_3V3B  
 0.1µF 6.3V  
 XOSCI5  
 24.576MHz

**SubArctic-AM335X**  
 15mm x 15mm  
 Package

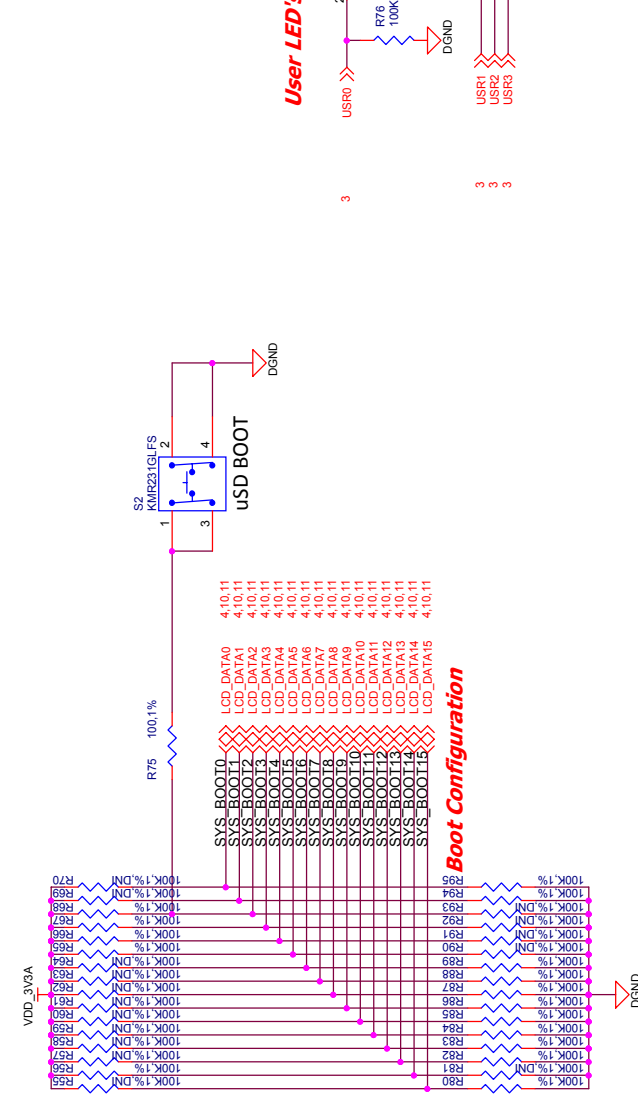
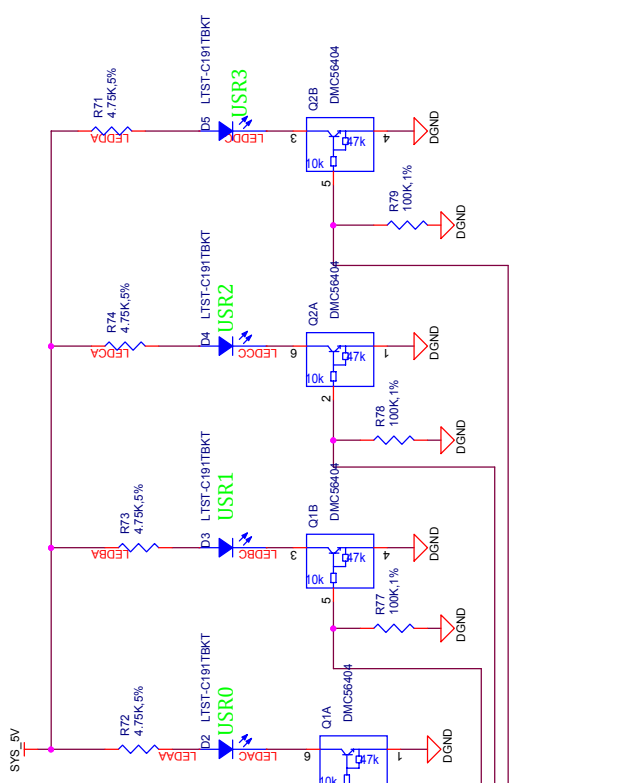


Mark pin 1 clearly  
 USB to TTL  
 Serial Cable  
 3.3V

USB HOST

USB PC CONNECTOR



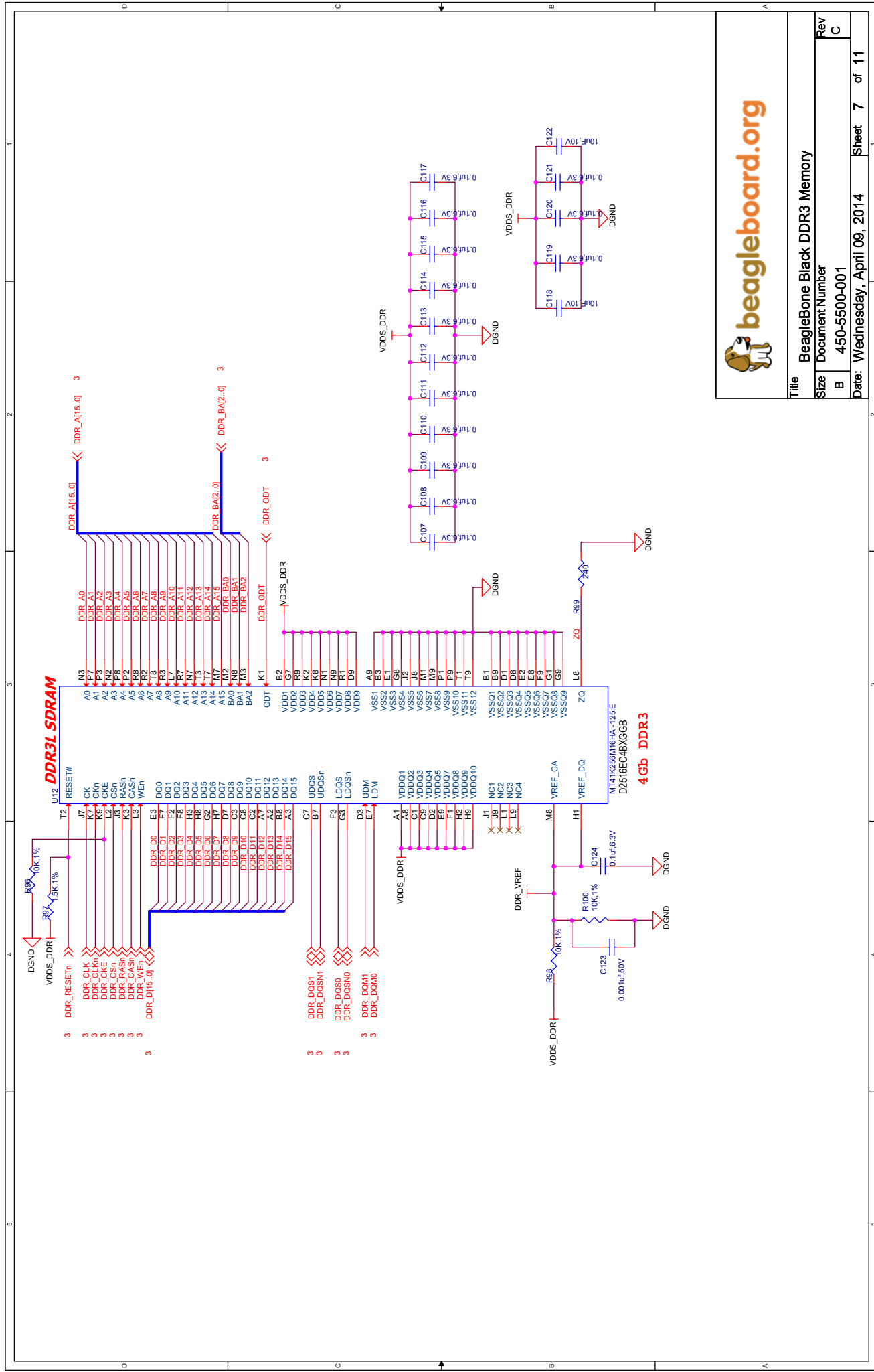


SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC0   UART0   USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	MMC0   SPI0   USB0[5]   UART0



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Title		BeagleBone Black LED, Configuration, and Reset
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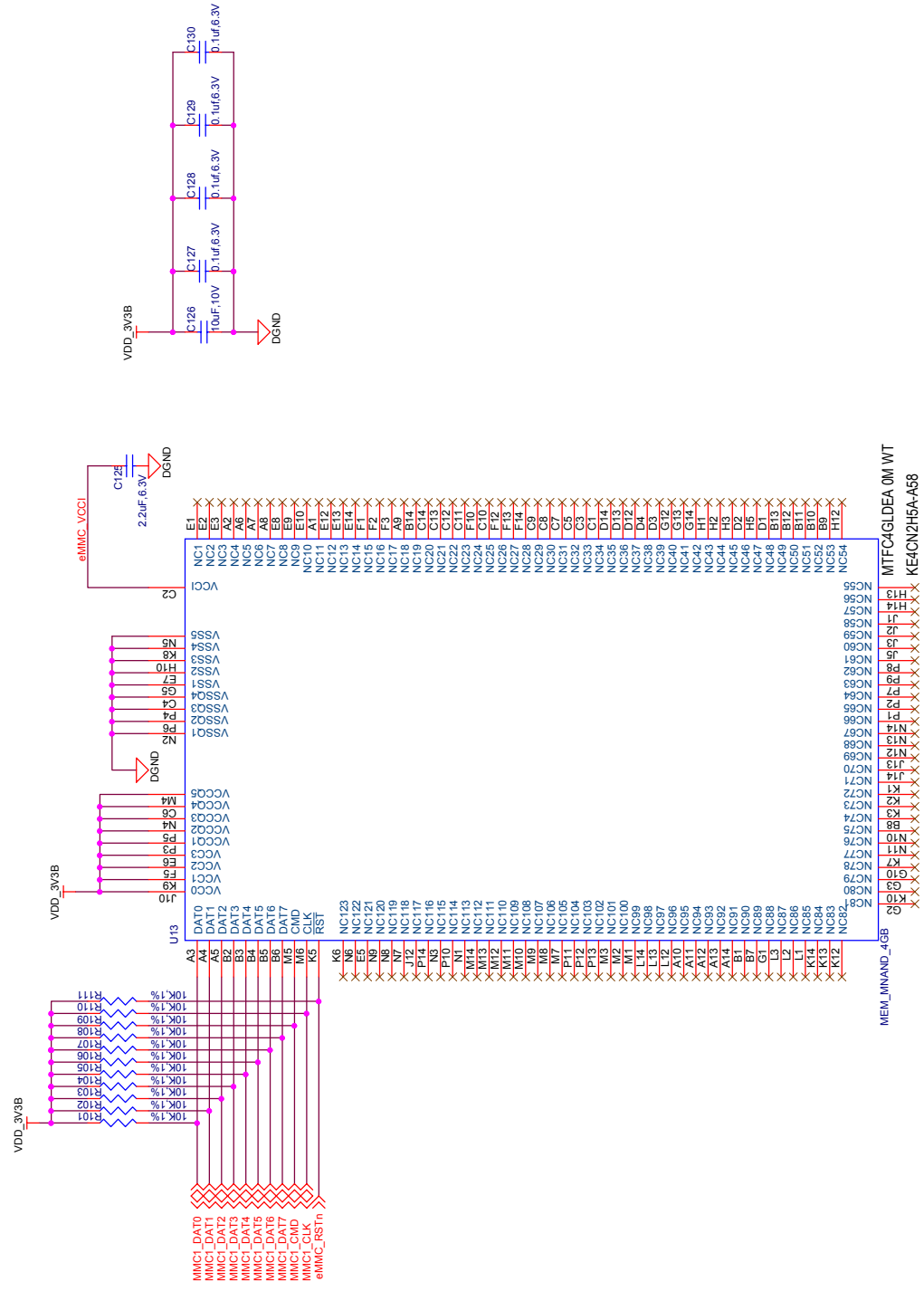
beagleboard.org

Title		BeagleBone Black DDR3 Memory
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Title Beagle BoneBlack 4G eMMC

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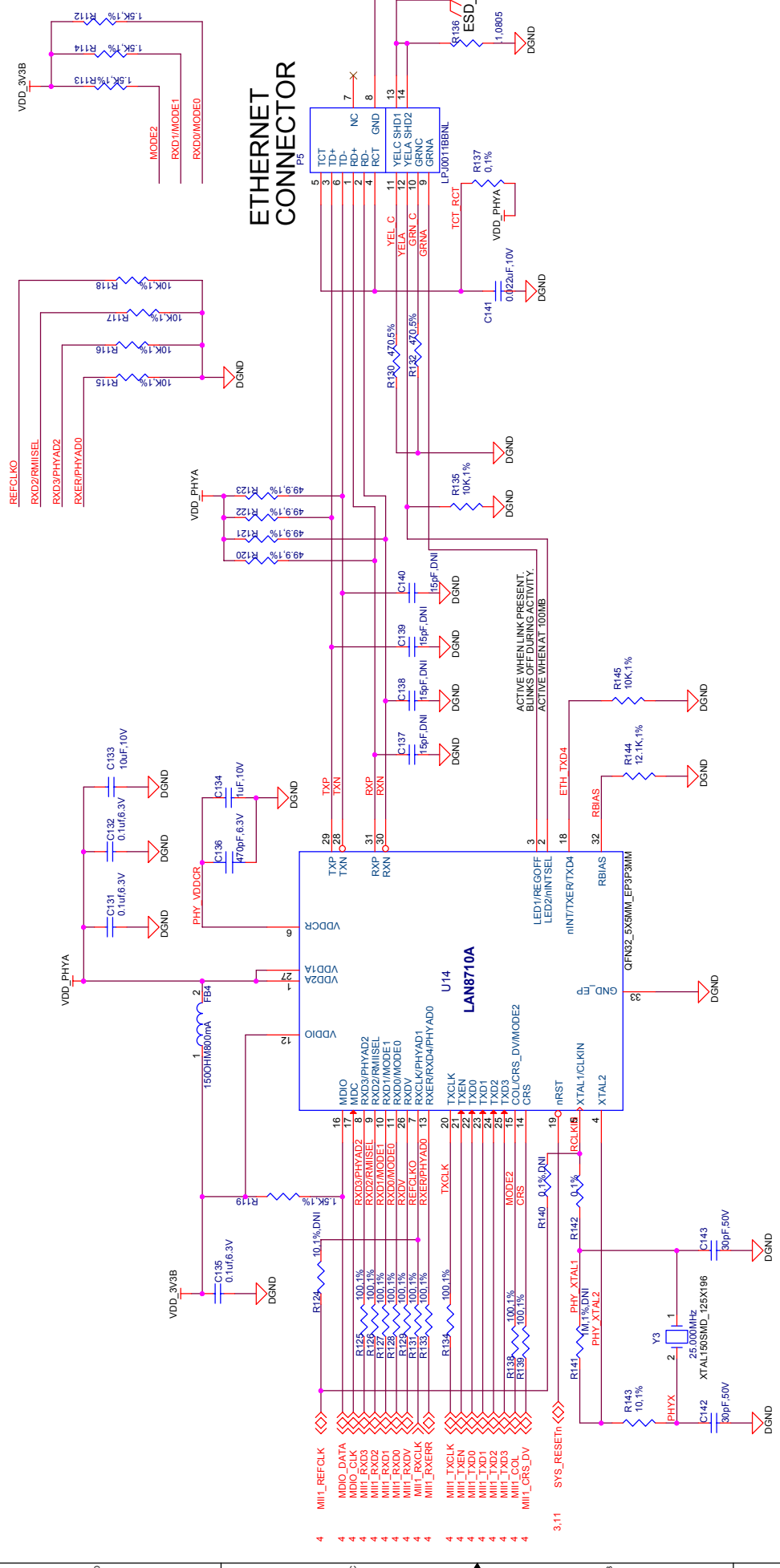


MEM\_MNAND\_4GB  
 NC8  
 G9  
 G8  
 G7  
 G6  
 G5  
 G4  
 G3  
 G2  
 G1  
 G0  
 NC80  
 NC79  
 NC78  
 NC77  
 NC76  
 NC75  
 NC74  
 NC73  
 NC72  
 NC71  
 J14  
 J13  
 J12  
 J11  
 J10  
 J9  
 J8  
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 NC130

MTFC4GLDEA 0M WT  
 KE4CN2H5A-A58

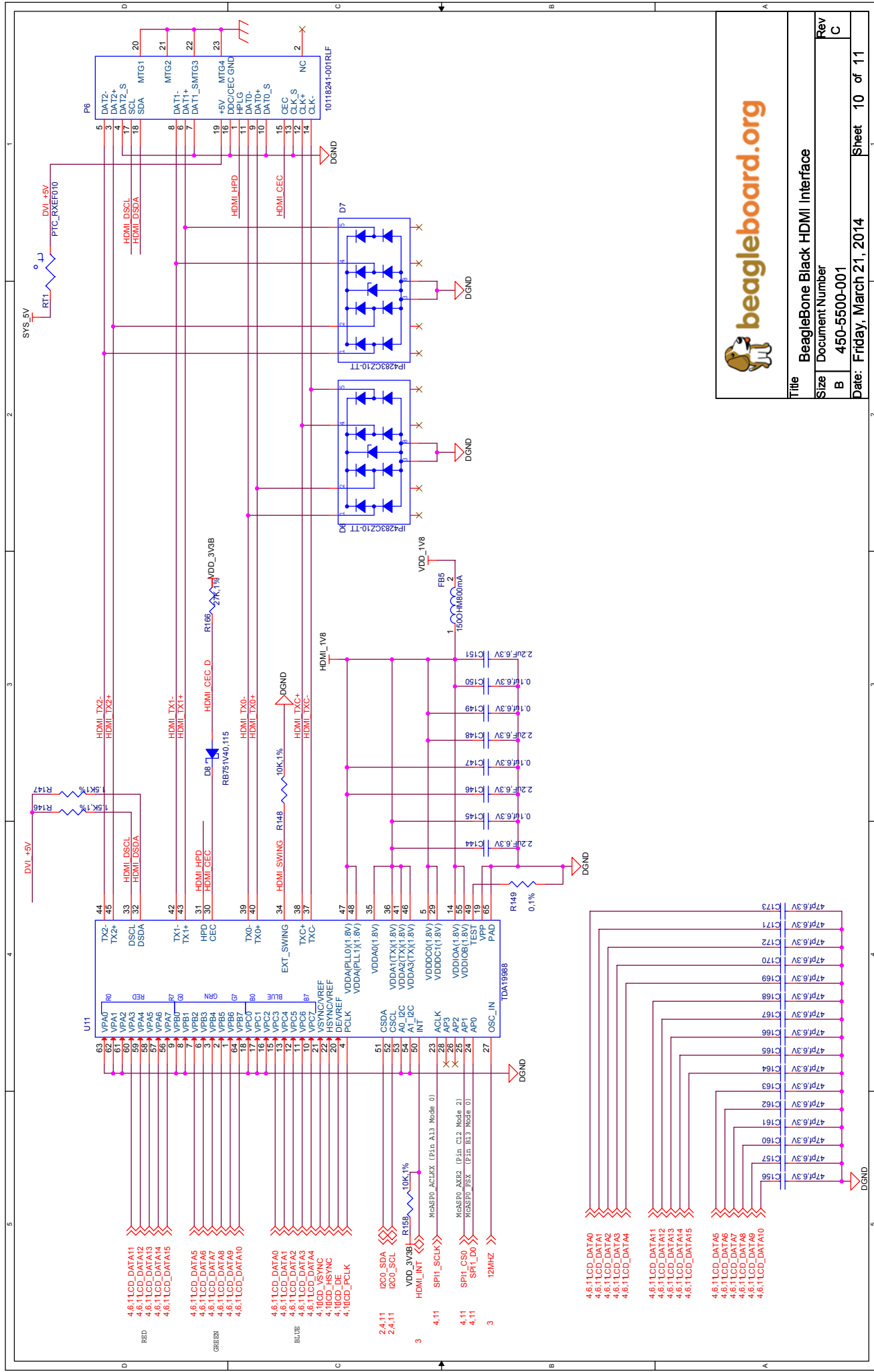




## ETHERNET CONNECTOR



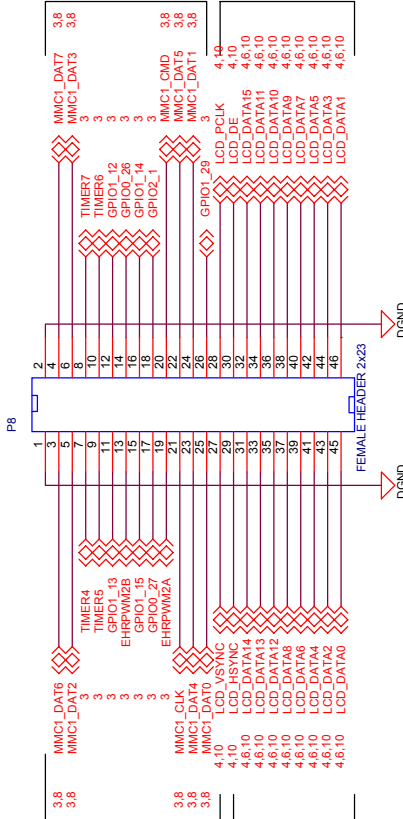
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BeagleBone Black Ethernet		
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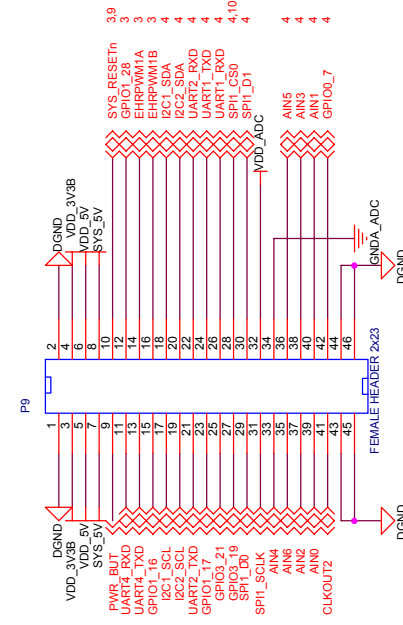
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CAUTION: USED ON BOARD

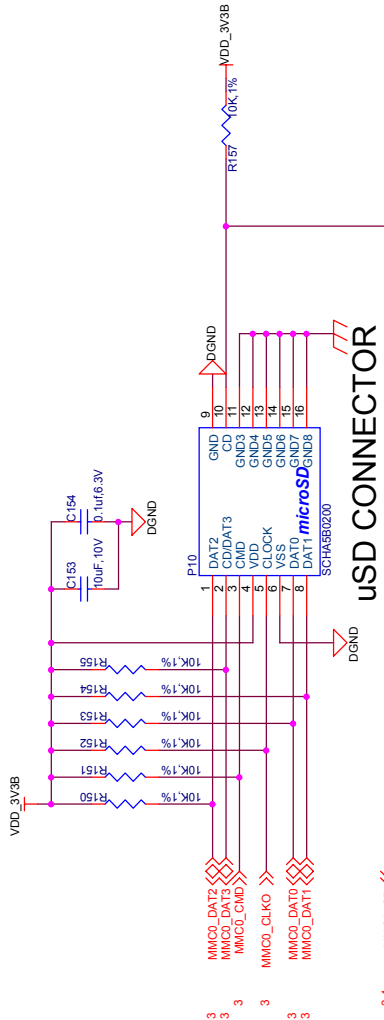


### EXPANSION HEADER

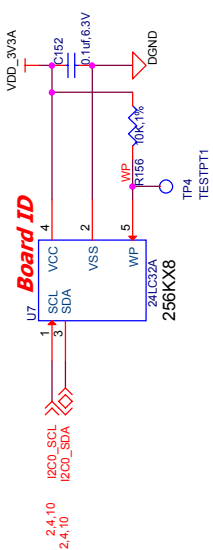
CAUTION: USED ON BOARD



### EXPANSION HEADER



### uSD CONNECTOR



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